AN2258/D
Rev. 0.4, 4/2002

Differences and Additions in the MPC82xx HiP3 and HiP4 Silicon

This document provides information for customers who are migrating from the HiP3-process technology PowerQUICC II™ MPC8260 device(s) to HiP4 silicon. It addresses the important differences, derivatives, and additional features of HiP4 MPC82xx silicon.

IMPORTANT DIFFERENCES

Improvements in voltage and performance are summarized below.

Characteristic	HiP3 MPC8260	HiP4 MPC82xxA
Core Supply Voltage	2.4V – 2.7V	1.7V – 2.1V for devices 233 MHz and below 1.9V – 2.1V for devices 266 MHz and above
Maximum speeds (MHz)	200 (CPU/)166 (CPM) /66 (bus)	300 (CPU) /208 (CPM) /83 (bus)

Customers should refer to the most current device errata and hardware specifications documents available at www.freescale.com/semiconductors.

DERIVATIVES

There are several new derivatives of the PowerQUICC II that may prove to be a better overall solution to customer products. The table below shows the functionality that defines each derivative of the HiP4-enhanced PowerQUICC II family.

HiP4 PowerQUICC II Family Derivatives

Functionality	Derivatives					
	MPC8250A	MPC8255A	MPC8260A	MPC8264A	MPC8265A	MPC8266A
HiP4 enhancements	X	X	X	X	X	X
PCI bridge	X				X	X
Transmission convergence (TC) layer				X		X
Inverse multiplexing for ATM (IMA)				X		X

ADDITIONAL FEATURES

Additional features of the MPC82xxA family are as follows:

- CPM
  - 32-Kbyte dual-port RAM
  - Additional MCC host commands
  - Eight transfer transmission convergence (TC) layers between the TDMs and FCC2 to support inverse multiplexing for ATM capabilities (IMA) (MPC8264A and MPC8266A only)
- CPM multiplexing
  - FCC2 can also be connected to the TC layer (MPC8264A and MPC8266A only)
- TC layer (MPC8264A and MPC8266A only)
  - Each of the 8 TDM channels is routed in hardware to a TC layer block
  - Protocol-specific overhead bits may be discarded or routed to other controllers by the SI
  - Performing ATM TC layer functions (according to ITU-T I.432)
  - Transmit (Tx) updates
  - Cell HEC generation
  - Payload scrambling using self synchronizing scrambler (programmable by the user)
  - Coset generation (programmable by the user)
  - Cell rate by inserting idle/unassigned cells
  - Receive (Rx) updates
  - Cell delineation using bit by bit HEC checking and programmable ALPHA and DELTA parameters for the delineation state machine
  - Payload descrambling using self synchronizing scrambler (programmable by the user)
  - Coset removing (programmable by the user)
  - Filtering idle/unassigned cells (programmable by the user)
  - Performing HEC error detection and single bit error correction (programmable by user)
  - Generating loss of cell delineation status/interrupt (LOC/LCD)
  - Operates with FCC2 (UTOPIA 8)
  - Provides serial loop back mode
  - Cell echo mode is provided
  - Supports both FCC transmit modes
  - External rate mode—Idle cells are generated by the FCC (microcode) to control data rate.
  - Internal rate mode (sub-rate)—FCC transfers only the data cells using the required data rate. The TC layer generates idle/unassigned cells to maintain the line bit rate.
  - Supports TC-layer and PMD-WIRE interface (according to the ATM-Forum af-phy-0063.000)
  - Cell counters for performance monitoring
  - 16-bit counters count
  - HEC error cells
  - HEC single bit error and corrected cells

- Idle/unassigned cells filtered
- Idle/unassigned cells transmitted
- Transmitted ATM cells
- Received ATM cells
- Maskable interrupt is sent to the host when a counter expires
- Overrun (Rx cell FIFO) and underrun (Tx cell FIFO) condition produces maskable interrupt
- May be operated at E1 and DS-1 rates. In addition, xDSL applications at bit rates up to 10 Mbps are supported

- PCI bridge (MPC8250A, MPC8265A, and MPC8266A only)
  - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
  - On-chip arbitration
  - Support for PCI to 60x memory and 60x memory to PCI streaming
  - PCI Host Bridge or Peripheral capabilities
  - Includes 4 DMA channels for the following transfers:
    - PCI-to-60x to 60x-to-PCI
    - 60x-to-PCI to PCI-to-60x
    - PCI-to-60x to PCI-to-60x
    - 60x-to-PCI to 60x-to-PCI
  - Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8265A) required by the PCI standard as well as message and doorbell registers
  - Supports the I 2 O standard
  - Hot-Swap friendly (supports the Hot Swap Specification as defined by PICMG 2.1 R1.0 August 3, 1998)
  - Support for 66 MHz, 3.3 V specification
  - 32-bit data bus
  - 60x-PCI bus core logic which uses a buffer pool to allocate buffers for each port
  - Makes use of the local bus signals to avoid need for additional pins

ADDITIONAL DIFFERENCES

Pin Termination: AE11, U5, AF25, and V4

HiP3 Silicon

The spare pins AE11, U5, AF25, and V4 must be pulled down or left floating. However, if a customer needs HiP3 silicon to be compatible with HiP4 silicon, note the following:

- AF25 must be pulled up or left floating

HiP4 Silicon

The pins U5 and V4 and AE11 must be pulled down or left floating. However, on all HiP4 silicon (both PCI and non-PCI devices) when PCI is not used, note the following:

- AF25 must be pulled up or left floating

Refer to relevant *Hardware Specifications* document(s) available at www.freescale.com/semiconductors.

External Filter Capacitor (XFC)

This signal connects to the off-chip capacitor for the main PLL filter. One terminal of the capacitor is connected to XFC while the other terminal is connected to VCCSYN. 30 MΩ is the minimum parasitic resistance value that ensures proper PLL operation when connected in parallel with the XFC capacitor. Refer to the silicon-specific tables below (the following information replaces the XFC description found in Table 9-3, “Dedicated PLL Pins,” in the *MPC8260 PowerQUICC II User’s Manual*.

XFC on HiP3 Silicon: Revisions A.1 and B.x

Multiplication Factor	Maximum Allowed Capacitance	Minimum Allowed Capacitance	Unit
MF ≤ 4 [1]	MF x 840 - 90	MF x 750 - 90	pF
MF > 4	MF x 1220	MF x 1100	pF

[1] If MR is 2.5, 3.5, or >4 the internal PLL does not lock reliably; this results in erratic behavior.

XFC on HiP3 Silicon: Revision C.2 and Future Revisions

Maximum Allowed Capacitance	Minimum Allowed Capacitance	Unit
MF x 840 - 90	MF x 750 - 90	pF

XFC on HiP4 Silicon

Recommended Capacitance	Maximum Allowed Capacitance	Minimum Allowed Capacitance	Unit
MF x 680 - 120	MF x 780 - 140	MF x 580 -100	pF

Definition of Multiplication Factor (MF)

If the ratio of CPM_CLK/CLKIN is an integer (A), MF = A. If CPM_CLK/CLKIN is A.5, MF = 2 x A.5. For example, if CPM_CLK/CLKIN is 166.66 MHz/ 66.66 MHz = 2.5, then MF = 5. The relevant factors are as follows:

CPM_CLK/CLKIN	Multiplication Factor (MF)
2	2
2.5	5
3	3
3.5	7
4	4
5	5
6	6

RAM MICROCODES

Updates for microcode packages for sale should be obtained through your usual Freescale sales contact.

Updated microcode documentation for MPC82xx HiP4 silicon is available by going to http://www.freescale.com/semiconductors. Click on “PowerQUICC” and then “Tools.”

ERRATA

A few device errata exist in the HiP4 PowerQUICC II devices. A detailed list of the errata can be found in the MPC8260 product page’s “Errata” table. Go to www.freescale.com/semiconductors.

AN2258 Revision History

Document Revision	Substantive Changes
0	—
0.1	• Addition of note on recommended termination of pins AE11, U5, AF25, and V4
0.2	• Addition of external lter capacitor (XFC) calculations • Modi cation of note on recommended ter mination
0.3	• Modi cation of note on recommended ter mination for AE11
0.4	• Modi cation of de nition of XFC m ultiplication factor

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

AN2258/D