Freescale Semiconductor
Application Note

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Differences Among PowerQUICC™ II Devices and Revisions

This application note provides information that could affect customer designs that are being migrated from an earlier revision of a PowerQUICC™ II device. The MPC82xx family members contain PowerPC™ core processors, which are built on Power Architecture™ technology. This application note is subject to updates as deemed necessary by Freescale to reflect product developments and changes. Customers are encouraged to take note of future versions.

Contents

freescale™ semiconductor

1 PowerQUICC II Devices and Revisions

PowerQUICC II devices are available in multiple silicon revisions, as shown in Table 1.

Table 1. PowerQUICC II Devices and Silicon Revisions

Device	Silicon												
Process	0.29µm (HiP3)					0.25µm (HiP4)			0.13µm (HiP7)				
	MPC8260 Family								MPC8280 Family			MPC8272 Family	
Rev	A.1	B.1	B.2	B.3	C.2	A.0	B.1	C.0	0.0	0.1	A.0	0.0	A.0
Mask	1K22A	1K23A	2K23A	3K23A	6K23A, 7K23A	2K25A	4K25A	5K25A	0K49M	1K49M	2K49M 3K49M	0K50M	1K50M
MPC8260(A)[1]	√	√	√	√	√	√	√	√					
MPC8250[2]						√	√[2]	√[2]					
MPC8255(A)[1]	√	√	√	√	√	√	√	√					
MPC8264						√	√	√					
MPC8265						√	√	√					
MPC8266						√	√	√					
MPC8270[3]									√	√	√		
MPC8275[4]									√	√	√		
MPC8280									√	√	√		
MPC8272[4]												√	√
MPC8271[4]												√	√
MPC8248[4]												√	√
MPC8247[4]												√	√

1 "A" designates HiP4 revisions of a device that was originally available in a HiP3 version.

2 Also available in 516 PBGA (VR or ZQ) package in HiP4 Rev B.1 and Rev C.0 only. Refer to Section 9, "Package Parameters," for more information

3 Also available in 516 PBGA (VR or ZQ) package

4 Only available in 516 PBGA (VR or ZQ) package

1.1 PowerQUICC II Functionality

Table 2 lists the features of all current PowerQUICC II devices. Refer to Section 9, "Package Parameters," for information about the various PowerQUICC II packages listed in Table 2.

Table 2. PowerQUICC II Functionality

Functionality	Devices																
Process	0.29µm (HiP3)	0.25µm (HiP4)							0.13µm (HiP7)							
	MPC8260 Family								MPC8280 Family				MPC8272 Family			
Device	8255	8260	8250		8255A [1]	8260A [1]	8264	8265	8266	8270		8275	8280	8272	8248	8271	8247
Package	480 TBGA		480	516	480 TBGA					480	516	516	480	516 PBGA			
Serial communications controllers (SCCs)	4	4	4	4	4	4	4	4	4	4	4	4	4	3	3	3	3
QUICC multi-channel controller (QMC)	—	—	—	—	—	—	—	—	—	—	—	—	—	Yes	Yes	Yes	Yes
Fast communication controllers (FCCs)	2	3	3	3	2	3	3	3	3	3	3	3	3	2	2	2	2
I-Cache (Kbyte)	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
D-Cache (Kbyte)	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
Ethernet (10/100)	2	3	3	3	2	3	3	3	3	3	3	3	3	2	2	2	2
UTOPIA II Ports	2	2	0	0	2	2	2	2	2	0	0	2	2	1	0	1	0
Multi-channel controllers (MCCs)	1	2	1	1	1	2	2	2	2	1	1	1	2	0	0	0	0
PCI bridge	—	—	Yes	Yes	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Transmission convergence (TC) layer	—	—	—	—	—	—	Yes	—	Yes	—	—	—	Yes	—	—	—	—
Inverse multiplexing for ATM (IMA)	—	—	—	—	—	—	Yes	—	Yes	—	—	—	Yes	—	—	—	—
Universal serial bus (USB) 2.0 full/low rate	—	—	—	—	—	—	—	—	—	1	1	1	1	1	1	1	1
Security engine (SEC)	—	—	—	—	—	—	—	—	—	—	—	—	—	Yes	Yes	—	—

[1] "A" designates HiP4 revisions of a device that was originally available in a HiP3 version.

2 Masks and Versions

Table 3 lists PowerQUICC II masks and versions.

Table 3. Masks and Versions

Process	Family	Revision	Qualification	Mask	PVR	IMMR[16–31] [1]	Rev_Num [2]
0.29 µm (HiP3)	**MPC8260**	A.1	XC	0K26N	0x00810101	0x0011	0x0001
		B.3	XC	3K23A	0x00810101	0x0023	0x003B
		C.2	XC	6K23A, 7K23A	0x00810101	0x0024	0x007B
0.25 µm (HiP4)		A.0	XC	2K25A	0x80811014	0x0060	0x000D
		B.1	MC	4K25A	0x80811014	0x0062	0x002D
		C.0	MC	5K25A	0x80811014	0x0064	0x002D
0.13 µm (HiP7)	**MPC8280**	0.0	—	0K49M	0x80822011	0x0A00	0x0070
		0.1	MC	1K49M	0x80822013	0x0A01	0x0070
		A.0	MC	2K49M, 3K49M	0x80822014	pxpA10	0x0071
	MPC8272	0.0	PC	0K50M	0x80822013	0x0C00 0x0D00	0x00E0
		A.0	MC	1K50M	px80822014	0x0C10 (encryption enabled) 0x0D10 (encryption disabled)	0x00E1

1 The IMMR[16–31] indicates the mask number.

2 The Rev_Num located at offset 0x8AF0 in DPRAM indicates the CPM microcode revision number.

3 Device Errata

A number of device errata have been eliminated since the original PowerQUICC II silicon. This allows the removal of related workarounds in future design work with new silicon revisions. Note that because of the release of the new silicon, new errata have been discovered and investigated. Designers should regularly review the errata document to determine how their designs are affected.

PowerQUICC II device errata document(s) are shown in Table 4.

Table 4. Device Errata Documentation

Device	Document Title	Document ID
All MPC8260 family devices	MPC8260 PowerQUICC II Family Device Errata	MPC8260CE
All MPC8272 family devices	MPC8272 PowerQUICC II Family Device Errata	MPC8272CE
All MPC8280 family devices	MPC8280 PowerQUICC II Family Device Errata	MPC8280CE

A set of microcode patches called *RAM Microcode Patch for MPC8260 Device Errata* is located in the “Errata” section on the MPC8260 product summary page. Both the microcode patches and the device errata documents are available at www.freescale.com.

4 Voltage and Performance

When migrating a design from a previous revision of an MPC82xx device to a more recent version, the voltage and performance differences in Table 5 must be taken into account. Customers should refer to the most current device errata and hardware specifications documents available at www.freescale.com.

Table 5. Voltage and Performance Differences

Process	Devices	Core Supply Voltage	Maximum Speeds (CPU/CPM/bus)
0.29 µm (HiP3)	MPC8260 MPC8255	2.4–2.7 V	200/166/66 (MHz)
0.25 µm (HiP4)	MPC8260A MPC8255A MPC8250 [1] MPC8264 MPC8265 MPC8266	1.7–1.9 V (CPU less than or equal to 200 MHz) 1.7–2.1 V (CPU greater than 200 MHz but less than 233 MHz) 1.9–2.2 V (CPU greater than or equal to 233 MHz)	300/208/83 (MHz)
0.13 µm (HiP7)	MPC8280 MPC8275 [2] MPC8270[1]	1.45–1.6 V	450/300/100 (MHz)
0.13 µm (HiP7)	MPC8272[2] MPC8271[2] MPC8248[2] MPC8247[2]	1.425–1.575 V	400/267/133 (MHz)

1 ZU, VR and ZQ packages

2 VR and ZQ packages

5 Microcode

5.1 RAM Microcode

The RAM microcode packages in Table 6 are available at www.freescale.com. Users should consult the web to determine if they have the latest version. Microcode packages for sale should be obtained through a Freescale sales contact.

Table 6. RAM Microcode Packages for PowerQUICC II Devices

Microcode Packages [1]	Fee-Based
Standard Feature	
ATM Adaptation Layer (AAL2)	No
Signaling System 7 (SS7)	No
Inverse-Multiplexing for ATM (IMA) [2]	No
82xx Errata Patches	No

Table 6. RAM Microcode Packages for PowerQUICC II Devices (continued)

Microcode Packages [1]	Fee-Based
Expanded Capability	
Enhanced AAL2	Yes
Enhanced SS7 [3]	Yes
Fast Data Switching (FDS) [4]	Yes
Multi-Service Platform Controller (MSP)	Yes

1 All microcode packages that are NOT fee based will be put into ROM at some future date.

2 MPC8264, MPC8266, and MPC8280 only

3 Enhanced SS7 includes Annex A, Chinese 2M GB std, and JT-Q.703

4 FDS is formerly known as ATM to Ethernet Switching (AES).

5.2 ROM Microcode

On HiP3 Rev A.1 and B.2 silicon, the interrupt queue's BSY bit is not maskable. Because of this, the interrupt queue is filled with busy events on the same channel each time the BD is accessed and found to be not ready.

On HiP3 Rev C.2 and subsequent silicon, an internal state is implemented to avoid the interrupt queue being filled with duplicate interrupts and to ensure that there is only a single interrupt per channel on a busy event.

As note 1 in Table 6 states, standard feature RAM microcode packages will be put into ROM at some future date.

6 Features

Features of all HiP3 and HiP4 devices in the MPC8260 PowerQUICC II family are summarized in Chapter 1, "Overview," of the *MPC8260 PowerQUICC™ II Family Reference Manual*.

Additional features of HiP7 devices—the MPC8280 family and the MPC8272 family—are summarized in the following sections. Refer to Section 1, "PowerQUICC II Devices and Revisions," and Section 1.1, "PowerQUICC II Functionality," for an overview of the two families.

6.1 Additional Features of the MPC8280 Family

Features of the MPC8280 family include the features summarized in Chapter 1, "Overview," of the *MPC8260 PowerQUICC™ II Family Reference Manual* and the following:

- CPU
  - Enhanced memory management unit (MMU) with eight-entry data and instruction BAT arrays providing 128-KByte to 256-MByte blocks
  - Enhanced cache control

- CPM
  - 32-Kbyte dual-port RAM for data use, 32-KByte dual-port RAM for microcode only
  - 10-/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII) or reduced media independent interface (RMII)
  - Enhanced UTOPIA functionality
    - Extended number of UTOPIA PHY's for FCC2
    - Internal rate scheduling for 31 UTOPIA PHY's
  - Universal serial bus (USB) controller
    - Supports USB 2.0 full/low rate compatible
    - Supports USB slave mode
    - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
    - CRC16/CRC5 generation and checking
    - NRZI encoding/decoding with bit stuffing
    - 12-Mbps or 1.5-Mbps data rate
    - Flexible data buffers with multiple buffers per frame
    - Automatic retransmission upon transmit error
- ZU package pin compatible with previous HiP3 and HiP4 (ZU) devices
- VR package introduction
  - Decreased device footprint
  - No lead spheres
- ZQ package introduction
  - Decreased device footprint
  - Lead spheres
- Enhanced clock frequencies
  - Up to 300-MHz CPM clock
  - Up to 450-MHz 603e CPU clock
  - Up to 100-MHz bus clock
- Reduced system power
  - Less than 2 W at full performance
- Enhancements to the G2_LE core register set
  - Additional HID0 bits
    - Address bus enable (ABE), HID0[28]—allows the G2_LE core to broadcast **dcbf**, **dcbi**, and **dcbst** onto the 60x bus
    - Instruction fetch enable M (IFEM), HID0[24]—allows the G2_LE core to reflect the value of the M bit during instruction translation onto the 60x bus
  - HID2 register—enables true little-endian mode, the new additional BAT registers, and cache way locking for the G2_LE core

  - System version register (SVR)—identifies the specific version and revision level of the system-on-a-chip integration
  - Processor version register (PVR)—updated with a new value to identify the version and revision level of the processor
- Enhancements to cache implementation
  - Instruction cache is blocked only until the critical load completes (hit under reloads allowed)
  - Minimized stalls due to load delays. The critical double word is simultaneously written to the cache and forwarded to the requesting unit.
  - HID2 register enables instruction and data cache way locking
  - Optional data cache operation broadcast feature— allows for correct system management using an external copy-back L2 cache; enabled by HID0[ABE]
  - Cache control instructions—HID0[ABE] must be enabled to execute all cache control instructions (**icbi**, **dcbi**, **dcbf**, and **dcbst**) excluding **dcbz**
- Exceptions
  - Hardware support for misaligned little-endian (LE) accesses. LE load/store accesses that are not on a word boundary, with the exception of strings and multiples, generate exceptions under the same circumstances as big-endian (BE) accesses.
  - Graphics instructions cause an alignment exception if the access is not on a word boundary. The G2_LE core does not have misalignment support for **eciwx** and **ecowx**.
  - Critical interrupt exception that has higher priority than the system management interrupt
- Bus clock—new bus multipliers are selected by the encodings of core_pll_cfg[0–4]
- Instruction timing
  - Integer divide instructions—**divwu[o**][**.]** and **divw**[**o][.**]—execute in 20 clock cycles. Execution in the original MPC603e (PID6-603e) takes 37 clock cycles.
  - Support for single-cycle store
  - Adder/comparator added to system register unit—allows dispatch and execution of multiple integer add and compare instructions on each cycle
- Enhanced debug features
  - Addition of three breakpoint registers—IABR2, DABR, and DABR2
  - Addition of two breakpoint control registers—DBCR and IBCR

For more information on the execution units, refer to the *G2 PowerPC™ Core Reference Manual* (G2CORERM/D).

6.2 Additional Features of the MPC8272 Family

Features of the MPC8280 family include the features summarized in Chapter 1, “Overview,” of the *MPC8260 PowerQUICC™ II Family Reference Manual* and the following. Note that the CPM functionality differs from the MPC8260 and the MPC8280 families; refer to Section 1.1, “PowerQUICC II Functionality” on page 2.

- Separate PLLs for G2_LE core and for the CPM
  - G2_LE core and CPM can run at different frequencies for power/performance optimization
  - Internal core/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 4.5:1, 5:1, 5.5:1, 6:1, 7:1, and 8:1 ratios
  - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, and 6:1 ratios
- Integrated encryption engine (SEC) (MPC8272 and MPC8248 only)
  - Supports DES, 3DES, MD-5, SHA-1, AES, PKEU, RNG, and RC-4 encryption algorithms in hardware
- CPU
  - Enhanced MMU with eight-entry data and instruction BAT arrays providing 128-KByte to 256-MByte blocks
  - Enhanced cache control
- Communications processor module (CPM)
  - Interfaces to G2_LE core through on-chip dual-port RAM and DMA controller. (Dual-port RAM size is 16 Kbyte plus 4Kbyte dedicated instruction RAM.)
  - Two fast communication controllers (FCCs) supporting the following protocols
    - 10-/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII)
    - Transparent
    - HDLC—up to T3 rates (clear channel)
    - One of the FCCs supports ATM (MPC8272 only)—full-duplex SAR at 155 Mbps, 8-bit UTOPIA interface 31 Mphys, AAL5, AAL1, AAL2, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 64-K external connections
  - Three serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
    - Ethernet/IEEE 802.3 CDMA/CS
    - HDLC/SDLC and HDLC bus
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART
    - Binary synchronous (BiSync) communications
    - Transparent

- QMC (QUICC multichannel controller) up to 64 channels
  - Independent transmit and receive routing, frame synchronization
  - Serial-multiplexed (full-duplex) input/output 2048-, 1544-, and 1536-Kbps PCM highways
  - Compatible with T1/DS1 24-channel and CEPT E1 32-channels PCM highway, ISDN basic rate, ISDN primary rate, and user defined
  - Sub channeling on each time slot
  - Independent transmit and receive routing, frame synchs and clocking
  - Concatenation of any, not necessarily consecutive, time slots to channels independently for Rx/Tx
  - Supports H1,H11 and H12 channels
  - Allows dynamic allocation of channels
- SCC3 in NMSI mode is not usable when USB is enabled.

— Two serial management controllers (SMCs) identical to those of the MPC860
- Provide management for BRI devices as general-circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
- Transparent
- UART (low-speed operation)

— Up to two TDM interfaces
- Supports one group of two TDM channels
- 1024 bytes of SI RAM

— Universal serial bus (USB) controller
- Supports USB 2.0 full/low rate compatible
- Supports USB slave mode
- Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
- CRC16/CRC5 generation and checking
- NRZI encoding/decoding with bit stuffing
- 12-Mbps or 1.5-Mbps data rate
- Flexible data buffers with multiple buffers per frame
- Automatic retransmission upon transmit error

- VR package
  — Decreased device footprint from ZU package
  — No lead spheres
- ZQ package introduction
  — Decreased device footprint from ZU package
  — Lead spheres

- Enhancements to the G2_LE core register set
  - Additional HID0 bits
    - Address bus enable (ABE), HID0[28]—allows the G2_LE core to broadcast **dcbf**, **dcbi**, and **dcbst** onto the 60x bus
    - Instruction fetch enable M (IFEM), HID0[24]—allows the G2_LE core to reflect the value of the M bit during instruction translation onto the 60x bus
  - HID2 register—enables true little-endian mode, the new additional BAT registers, and cache way locking for the G2_LE core
  - System version register (SVR)—identifies the specific version and revision level of the system-on-a-chip integration
  - Processor version register (PVR)—updated with a new value to identify the version and revision level of the processor
- Enhancements to cache implementation
  - Instruction cache is blocked only until the critical load completes (hit under reloads allowed)
  - Minimized stalls due to load delays. The critical double word is simultaneously written to the cache and forwarded to the requesting unit.
  - HID2 register enables instruction and data cache way locking
  - Optional data cache operation broadcast feature— allows for correct system management using an external copy-back L2 cache; enabled by HID0[ABE]
  - Cache control instructions—HID0[ABE] must be enabled to execute all cache control instructions (**icbi**, **dcbi**, **dcbf**, and **dcbst**) excluding **dcbz**
- Exceptions
  - Hardware support for misaligned little-endian (LE) accesses. LE load/store accesses that are not on a word boundary, with the exception of strings and multiples, generate exceptions under the same circumstances as big-endian (BE) accesses.
  - Graphics instructions cause an alignment exception if the access is not on a word boundary. The G2_LE core does not have misalignment support for **eciwx** and **ecowx**.
  - Critical interrupt exception that has higher priority than the system management interrupt
- Bus clock—new bus multipliers are selected by the encodings of core_pll_cfg[0–4]
- Instruction timing
  - Integer divide instructions—**divwu[o**][**.]** and **divw**[**o][.**]—execute in 20 clock cycles. Execution in the original MPC603e (PID6-603e) takes 37 clock cycles.
  - Support for single-cycle store
  - Adder/comparator added to system register unit—allows dispatch and execution of multiple integer add and compare instructions on each cycle
- Enhanced debug features
  - Addition of three breakpoint registers—IABR2, DABR, and DABR2
  - Addition of two breakpoint control registers—DBCR and IBCR

For more information on the execution units, refer to the *G2 PowerPC™ Core Reference Manual* (G2CORERM/D).

7 Pin Termination

Recommended pin terminations are presented in *MPC8260 PowerQUICC™ II Design Checklist* (AN2290) as well as the hardware specification document available on each device's summary page at www.freescale.com. However, note the recommendations that follow.

7.1 HiP3 Silicon

The spare pins AE11, U5, AF25, and V4 may be pulled down (recommended) or may be left floating. However, if a customer needs a HiP3 PowerQUICC II design to be compatible with a HiP4 device, note the following:

- AF25 must be pulled up or left floating

7.2 HiP4 Silicon

The spare pins U5, V4, and AE11 (on PCI devices, AE11 is CLKIN2; refer to the "MPC82xx/MPC82xxA Functionality" table on page 2) may be pulled down (recommended) or may be left floating. However, on all HiP4 silicon (both PCI and non-PCI devices) when PCI is not used, note the following:

- AF25 must be pulled up or left floating

For information on designing with the MPC8250VR and MPC8250ZQ, consult the *MPC8250 Hardware Specifications* (MPC8250EC) and the *MPC8260 PowerQUICC™ II Design Checklist* (AN2290).

7.3 HiP7 Silicon

7.3.1 ZU Package (480 TBGA)

The spare pins (U5 and V4) and CLKIN2 (AE11) may be pulled down (recommended) or may be left floating. However, when PCI is not used, note the following:

- PCI_MODE (AF25) must be pulled up or left floating

The XFC pin on HiP3 and HiP4 devices is not used on HiP7 devices. There is no need for an external capacitor to operate the PLL. New HiP7 designs (or existing HiP3/HiP4 designs with XFC capacitor removed) should connect AB2 (XFC) to GND. Older designs in which a HiP7 device is used as a drop-in replacement can leave this pin connected to the current capacitor.

GNDSYN on HiP3 and HiP4 devices does not exist as a separate ground signal on HiP7 devices. New designs should connect AB1 to GND and follow the layout practices suggested in the *MPC8280 Hardware Specification* (MPC8280EC). Older designs in which a HiP7 device is used as a drop-in replacement can leave this pin connected to GND with the noise filtering capacitors.

NOTE: THERMAL[0:1]

The thermal pins are not supported on Rev 0.1 (mask number 1K49M). The pins—THERMAL0 at AA1 and THERMAL1 at AG4—are not connected.

The HiP7 ZU package is pin-compatible with all HiP3/HiP4 devices, except for the MPC8250VR/ZQ. However, the user should take note of additional pin multiplexing added to enable the following features:

- USB 2.0 full/low rate compatible
- 32 MultiPHYs for each UTOPIA FCC
- FCC 10/100 Ethernet RMII

The user should consult the *MPC8280 PowerQUICC™ II Specification: Addendum to the MPC8260 PowerQUICC II User's Manual* (MPC8280UMAD) for the available pin muxing configurations of these features.

7.3.2 VR and ZQ Package (516 PBGA)

Both the MPC8280 and the MPC8272 families are offered in the 516 PBGA package. However, because the pinout is different for each family, it is important to consult the appropriate section below.

7.3.2.1 MPC8280 Family

The spare pins (C14 and B15) and CLKIN2 (K21) may be pulled down (recommended) or may be left floating. However, when PCI is not used, note the following:

- PCI_MODE (AD24) must be pulled up or left floating

The XFC pin on the HiP3 and HiP4 devices is not used on the HiP7 devices. There is no need for an external capacitor to operate the PLL. New HiP7 designs (or existing HiP3/HiP4 designs with XFC capacitor removed) should connect A18 (XFC) to GND. Older designs in which a HiP7 device is used as a drop-in replacement can leave this pin connected to the current capacitor.

GNDSYN on HiP3 and HiP4 devices does not exist as a separate ground signal on HiP7 devices. New designs should connect B18 to GND and follow the layout practices suggested in the *MPC8280 Hardware Specification* (MPC8280EC). Older designs in which a HiP7 device is used as a drop-in replacement can leave this pin connected to GND with the noise filtering capacitors.

For information on designing with VR- and ZQ-package devices, consult the *MPC8280 Hardware Specifications* (MPC8280EC) and the *MPC8260 PowerQUICC™ II Design Checklist* (AN2290).

NOTE: THERMAL[0:1]

The thermal pins are not supported on Rev 0.1 (mask number 1K49M). The pins—THERMAL0 at E17 and THERMAL1 at C23—are not connected.

7.3.2.2 MPC8272 Family

The spare pin (AD24) and CLKIN2 (C21) may be pulled down (recommended) or may be left floating.

The XFC pin on HiP3 and HiP4 devices is not used on HiP7 devices. There is no need for an external capacitor to operate the PLL. New HiP7 designs (or existing HiP3/HiP4 designs with XFC capacitor

removed) should connect A18 (XFC) to GND. Older designs in which a HiP7 device is used as a drop-in replacement can leave this pin connected to the current capacitor.

GNDSYN on HiP3 and HiP4 devices does not exist as a separate ground signal on HiP7 devices. New designs should connect B18 to GND and follow the layout practices suggested in the *MPC8272 Family Hardware Specifications* (MPC8272EC). Older designs in which a HiP7 device is used as a drop-in replacement can leave this pin connected to GND with the noise filtering capacitors.

For more information, consult the *MPC82872 Family Hardware Specifications* (MPC8280EC) and the *MPC8260 PowerQUICC™ II Design Checklist* (AN2290).

NOTE: THERMAL[0:1]

The thermal pins are not supported. The pins—THERMAL0 at D19 and THERMAL1 at J3—are not connected.

8 Clocking

8.1 HiP3 and HiP4—External Filter Capacitor (XFC)

NOTE

XFC is not used on HiP7 devices.

This signal connects to the off-chip capacitor for the main PLL filter. One terminal of the capacitor is connected to XFC while the other terminal is connected to VCCSYN. The minimum parasitic resistance value that ensures proper PLL operation when connected in parallel with the XFC capacitor is 30 MΩ. The value of XFC is determined according to the multiplication factor (MF) as defined below. Note that XFC equations are silicon-specific; refer to the following tables.

8.1.1 Definition of Multiplication Factor (MF)

If the ratio of CPM_CLK/CLKIN is an integer (A), MF = A. If CPM_CLK/CLKIN is A.5, MF = 2 x A.5. The relevant ratios and factors are shown in Table 7.

Table 7. Clock Ratios and Multiplication Factors

CPM_CLK/CLKIN	Multiplication Factor (MF)
2	2
2.5	5
3	3
3.5	7
4	4
5	5
6	6

Table 8. .29μm (HiP3) Silicon: Rev. A.1 and B.x

Multiplication Factor	Maximum Allowed Capacitance	Minimum Allowed Capacitance	Unit
MF ≤ 4	MF x 840 - 90	MF x 750 - 90	pF
MF > 4	MF x 1220	MF x 1100	pF

Table 9. .29μm (HiP3) Silicon: Rev. C.2 and Future Revisions

Maximum Allowed Capacitance	Minimum Allowed Capacitance	Unit
MF x 840 - 90	MF x 750 - 90	pF

Table 10. .25μm (HiP4) Silicon

Recommended Capacitance	Maximum Allowed Capacitance	Minimum Allowed Capacitance	Unit
MF x 680 - 120	MF x 780 - 140	MF x 580 -100	pF

8.2 HiP7—Clock Mode Compatibility

The minimum operating frequency for the HiP7 devices varies according to the clock mode, as shown in the clock tables in the *MPC8280 Family Hardware Specifications* (MPC8280EC) and the *MPC8272 Family Hardware Specifications* (MPC8272EC). This restriction and the specific multiplication factors for a given clock mode establish the minimum allowable frequencies for the input bus clock and CPM. The maximum allowable frequencies are established by the rating of the user's device.

Customers who are migrating a previous PowerQUICC II design to a HiP7 device (refer to Table 1 on page 2) should verify that the design's configuration of clock frequencies is within the supported range for HiP7 devices.

8.3 HiP7—CPM PLL Programming Model

Customers who are migrating PowerQUICC II designs to HiP7 silicon from earlier silicon need to be aware that the PLL for the CPM has changed on HiP7.

In particular, the system clock mode register (SCMR) on HiP7 devices is different. Customers should refer to Section 4.5 in the *MPC8280 PowerQUICC™ II Specification: Addendum to the MPC8260 PowerQUICC II™ Family Reference Manual* (Document order number: MPC8280UMAD) for a complete description.

9 Package Parameters

PowerQUICC II devices are available in three packages (ZU, VR, and ZQ), as shown in Table 11.

Table 11. PowerQUICC II Device Packages

480 TBGA	516 PBGA	
ZU	VR (no lead spheres)	ZQ (lead spheres)
MPC8260(A) [1] MPC8250 MPC8255(A)[1] MPC8264 MPC8265 MPC8266 MPC8270 MPC8280	MPC8250 [2] MPC8270 MPC8275 MPC8272 MPC8248 MPC8271 MPC8247	

1 "A" designates HiP4 revisions of a device that was originally available in a HiP3 version.

2 HiP4 Rev B.1 only

Primary package differences are displayed in Table 12.

Table 12. Package Parameters

Package	Type	Outline (mm)	Pitch (mm)	Nominal Unmounted Height (mm)	Solder Ball Content	θ_{JA}
ZU	480 TBGA	37.5 x 37.5	1.27	1.55	SnAgPb	12°C/W
VR	516 PBGA	27 x 27	1	2.25	SnAgCu	20°C/W (estimated)
ZQ	516 PBGA	27 x 27	1	2.25	SnAgPb	20°C/W (estimated)

Package details, including pinouts, can be found in each device's hardware specification document.

10 Document Revision History

Table 13 lists significant changes between revisions of this hardware specification.

Table 13. Document Revision History

Revision	Date	Substantive Change(s)
0	0	Initial release
1	10/2002	• Addition of information for HiP4 Rev B.1 • Addition of information for HiP7 devices (8280, 8275, 8270)
1.1	5/2003	Temporary release
1.2	6/2003	• Change of title from “Migration through PowerQUICC II Revisions” to “Differences among PowerQUICC II Devices and Revisions” • Update to HiP4 voltage based on CPU operating frequency • Update of HiP7 information • Addition of features list for the HiP7 G2_LE core • Addition of note on ROM microcode in Section 5, “Microcode” • Removal of date and revision from the table “RAM Microcode Packages for PowerQUICC II Devices.” Refer to the web for current information. • Addition of Section 8.2, “HiP7—Clock Mode Compatibility”
1.3	8/2003	• Addition of references to ZQ package throughout the document • Addition of references to HiP4 Rev C.0 • Addition of note about THERMAL[0:1] under “HiP7” in Section 7, “Pin Termination” • Addition of Section 8.3, “HiP7—CPM PLL Programming Model”
1.4	9/2003	• Addition of information on the MPC827 family devices (MPC8272, MPC8248, MPC8271, and MPC8247), including Section 6.2, “Additional Features of the MPC8272 Family,” and Section 7.3.2.2, “MPC8272 Family.” • Table 3, “Masks and Versions”: addition of HiP4 Rev C.0 REVNUM and correction of HiP7 Rev 0.1 PVR • Section 3, “Device Errata”: removal of previous device errata documents from the table. All PowerQUICC II device errata are now presented in the single document listed. • Update to references to USB support: the MPC8280 and the MPC8272 families support USB 2.0 full/low rate compatible • Removal of “HiP4 Features” from Section 6, “Features.” This information is now contained in the *MPC8260 PowerQUICC II™ Family Reference Manual*.
1.5	8/2006	• Table 1 on page 2: Addition of Rev. A.0 to the MPC8272 and MPC8280 families • Table 3 on page 4: Addition of Rev. A.0 to the MPC8272 and MPC8280 families and update of Rev_Num for MPC8272 Rev. 0.0 • Table 4 on page 4: Addition of MPC8272 and MPC8280 device errata documents
2.0	10/2008	• Table 5 on page 5: Updated Core Supply Voltage for MPC8280, MPC8275, MPC8270; updated Maximum Speeds for MPC8272, MPC8271, MPC8248, MPC8247

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How to Reach Us:

Home Page:
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Freescale Semiconductor
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1300 N. Alma School Road
Chandler, Arizona 85224
(800) 521-6274
480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 2666 8080
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
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