Freescale Semiconductor
Application Note

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Reference Design for High Resolution LCD Software Development

MC9328MX1

This document describes a reference design for developing high resolution software using the MC9328MX1 Application Development System (ADS). The scope of this text involves the hardware required to support the software development and the initialization code for such hardware including a test image.

Contents

1 Introduction

This reference design is intended for software developers who want to design high density resolution software applications utilizing the MC9328MX1 ADS. For complete information about the MC9328MX1 ADS please visit the i.MX Web site (www.freescale.com/imx).

This reference design enables software developers to set up one hardware apparatus and to set up the display area to display varying resolutions as required by the applications. The maximum resolution this hardware will support on a TFT panel is 640 × 480, otherwise known as Full VGA resolution.

2 Hardware

For this reference design two 18 bpp TFT panels of the same resolution (640 × 480) are used. The first panel requires a 5V interface while the second panel requires a 3V interface. It is important to note that the MC9328MX1 ADS supports 3V I/O on the LCD interface connector.

The two panels chosen are from Sharp®, a popular LCD manufacturer. This setup however could be used to support other TFT panels from other manufacturers. The two panels chosen are 6.4” and 10.4” requiring 5V and 3V interfaces respectively.

2.1 640×480 Sharp TFT Panel Interface

2.1.1 Block Diagram Using Sharp 6.4” TFT Panel LQ64D343

Using this panel requires a 3V to 5V interface to drive the 5V pins of the panel. The block diagram in Figure 1 on page 3 shows one working solution utilizing three MC74ACT245N drivers. ACT type drivers are recommended as they offer fast switching to handle the interface signals.

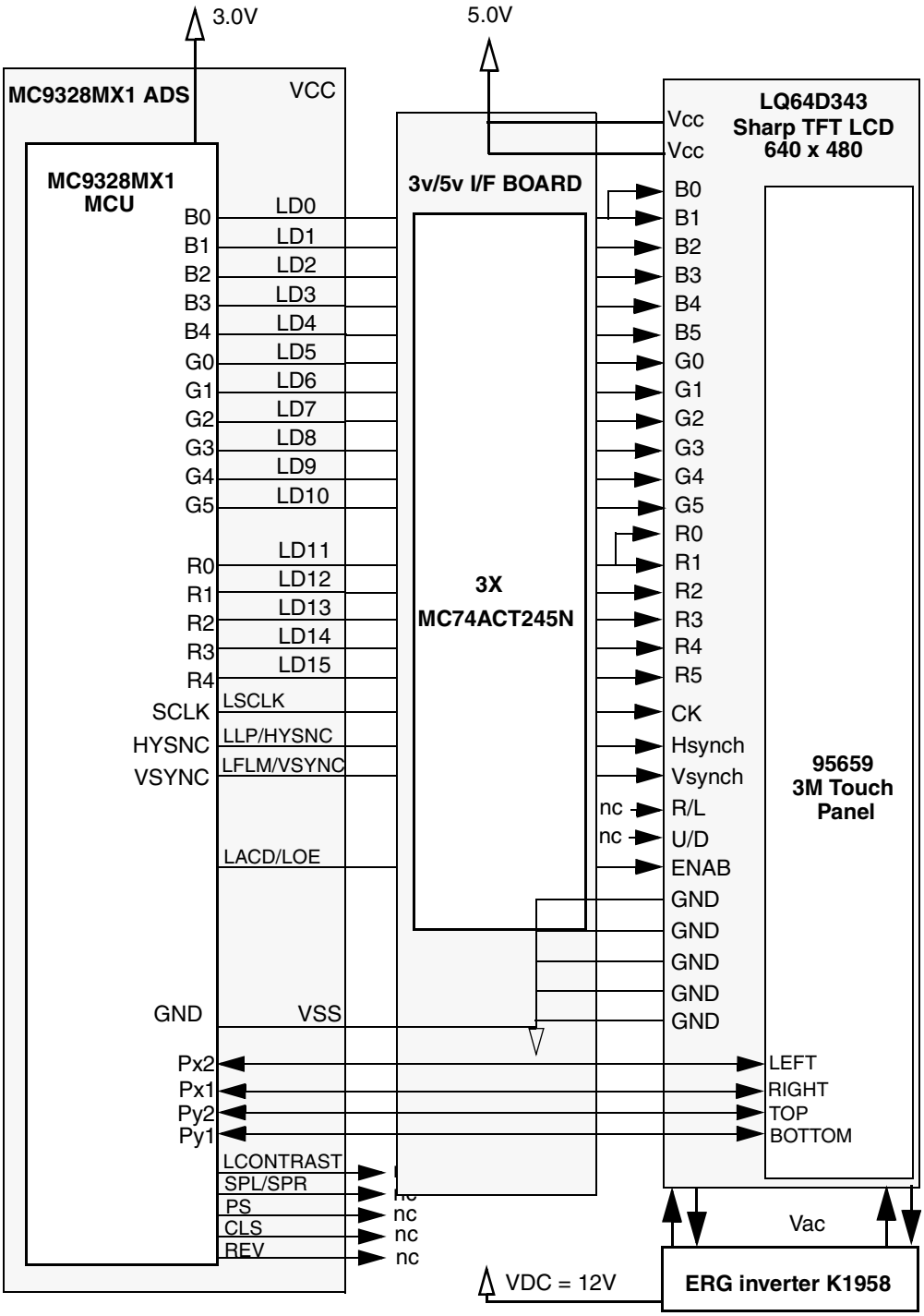

Figure 1. Block Diagram Using Sharp 6.4” TFT Panel LQ64D343

2.1.1.1 Parts List Using Sharp 6.4” TFT Panel LQ64D343

Table 1. Parts List Using Sharp 6.4” TFT Panel LQ64D343

Description	Quantity	Manufacturer Information and Spec Sheet	Notes
MC9328MX1/L ADS	1	Freescale Semiconductor Inc. www.freescale.com/imx	—
3 V DC power supply adaptor	1	—	Included with MC9328MX1 ADS
34 pin ribbon header F-F connector	1	Any	MC9328MX1 ADS to 3v/5v I/F Board
3V/5V I/F Board PCB w/ 3x MC74ACT245N	1	Freescale Semiconductor Inc	Not available from Freescale, users must build their own using reference
DF9M-31S-18D Hirose connector	1	International Component Technology www.intcomptech.com	3V/5V I/F Board to LQ64D343 Panel
The Hirose connector can be ordered from ICT. ICT may terminate the discrete wires of the Hirose connector using Molex 2.54 mm (0.100”) Pitch SL Crimp Housing 70450 Dual Row Version B Polarized, 22-55-2342 and slip the terminated wires into a Molex 2.54 mm (0.100”) Pitch SL Crimp Housing 70450 Dual Row Version B Polarized, 22-55-2342. Pins 1–29 of the Hirose terminated connector should be slipped into slots 1–29 of the Crimp Housing. Slot 30 is left unconnected and slots 31–34 are for the touch screen per the connection table.			
Molex 2.54 mm (0.100”) Pitch SL Crimp Housing 70450 Dual Row Version B Polarized, 22-55-2342	1	International Component Technology www.intcomptech.com	Slip Molex 2.54 mm (0.100”) Pitch SL Terminals into 33 of 34 slots per connection table
Molex 2.54 mm (0.100”) Pitch SL Terminal 71851 Female, High Force Crimp, 16-02-113	33	International Component Technology www.intcomptech.com	Crimp to DF9M-31S-18D Hirose connector and 4 pin single row header (29 Hirose connector and 4 for 4 pin single row male header post for touch screen)
0.100” Pitch 4 pin single row male header post	1	Any	Standard 4 pin male header, connect to Resistive Touch Screen Berg connector 4 pin female P/N 65801-004
LQ64D343 Panel	1	Sharp datasheet LD-10107	May substitute LQ104V1DG11 (datasheet LCY-99102)
95659 3M Resistive Touch Screen	1	3M/Dynapro www.dynapro.com	Could also substitute 3M 6.5” Resistive Touch Screen RES-6.5-FG4
ERG inverter K1958	1	ERG www.ergpower.com	Mfg. includes wire harness to connect to 12V DC power jack

Table 1. Parts List Using Sharp 6.4” TFT Panel LQ64D343 (continued)

Description	Quantity	Manufacturer Information and Spec Sheet	Notes
H2403305 “pigtail” connector	1	—	K1958 to 12V DC supply DC Power Jack
DPD120080-P5 CUI STACK 12V DC 800 mA power supply	1	DIGIKEY www.digikey.com	12V DC supply to drive ERG K1958
DC Power Jack 2.1 mm x 5.5 mm	1	PHILMORE	Fry’s Electronics
DPR050030-P6 CUI STACK 5V DC 300 mA power supply	1	DIGIKEY www.digikey.com	5V DC supply for 3V/5V I/F board
DC Power Jack 2.5 mm x 5.5 mm	1	PHILMORE	Fry’s Electronics

2.1.1.2 Connection Table for 6.4” Sharp TFT Panel

Table 2. MC9328MX1 ADS Connections to 640×480 6.4” Panel

MC9328MX1 Pin Number and Name on ADS Connector (2x34)		**Connector** (2x34)	**Sharp 640x480 Panel** Pin Number and Name (Hirose Connector)		**Touch Screen** Pin Number and Name		**Function**
2	VSS	1	1	GND			
6	LSCLK	2	2	CK			Clock signal for sampling each data signal
4	LLP/HYSNC	3	3	HSYNCH			Horizontal Synchronous Signal
5	LFLM/VSYNCH	4	4	VSYNCH			Vertical Synchronous Signal
2	VSS	5	5	GND			
18	LD11	6	6	R0			RED data signal (LSB)
29	LD11	7	7	R1			RED data signal
18	LD12	8	8	R2			RED data signal
17	LD13	9	9	R3			RED data signal
16	LD14	10	10	R4			RED data signal
15	LD15	11	11	R5			RED data signal (MSB)
2	VSS	12	12	GND			
28	LD5	13	13	G0			GREEN data signal (LSB)
27	LD6	14	14	G1			GREEN data signal

Table 2. MC9328MX1 ADS Connections to 640×480 6.4” Panel (continued)

MC9328MX1 Pin Number and Name on ADS Connector (2x34)		**Connector** (2x34)	**Sharp 640x480 Panel** Pin Number and Name (Hirose Connector)		**Touch Screen** Pin Number and Name		**Function**
14	LD7	15	15	G2			GREEN data signal
13	LD8	16	16	G3			GREEN data signal
12	LD9	17	17	G4			GREEN data signal
11	LD10	18	18	G5			GREEN data signal
2	VSS	19	19	GND			
10	LD0	20	20	B0			BLUE data signal (LSB)
25	LD0	21	21	B1			BLUE data signal
10	LD1	22	22	B2			BLUE data signal
9	LD2	23	23	B3			BLUE data signal
8	LD3	24	24	B4			BLUE data signal
7	LD4	25	25	B5			BLUE data signal
2	VSS	26	26	GND			
3	LACD/LOE	27	27	ENAB			Signal to settle the horizontal display position (driven by LOE)
		28	28	VCC			+5.0V power supply
		29	29	VCC			+5.0V power supply
		NC	30	R/L			Horizontal display mode select signal, not connected-open
		NC	31	U/D			Vertical display mode select signal, not connected-open
33	Py2	33			1	TOP	Touch panel
34	Py1	34			2	BOTTOM	Touch panel
31	Px2	31			3	LEFT	Touch panel
32	Px1	32			4	RIGHT	Touch panel
1	VCC	PAD					3.0 V Supply
19	LCONTRAST	NC					not connected
20	PWMO1	NC					not connected
21	LSPL	NC					not connected

Table 2. MC9328MX1 ADS Connections to 640×480 6.4” Panel (continued)

MC9328MX1 Pin Number and Name on ADS Connector (2x34)		**Connector** (2x34)	**Sharp 640x480 Panel** Pin Number and Name (Hirose Connector)		**Touch Screen** Pin Number and Name		**Function**
22	REV	NC					not connected
23	PS	NC					not connected
24	CLS	NC					not connected

2.1.1.3 Assembly and Setup Instructions

1. Place touch screen on LCD panel using double sided fixative (3M recommended).
2. Build the 3V/5V I/F board. The board should contain the level translators plus two 2x34 male headers to connect to.
3. Build a 34 signal straight through ribbon cable connector using ribbon cable and two 2x34 0.100” Pitch (100 mil) female headers.
4. Connect the cable to the MC9328MX1 ADS TFT LCD interface 2x34 male header and the input side of the 3V/5V I/F board 2x34 male header.
5. Solder 4 terminated (terminated with Molex 2.54 mm (0.100”) Pitch SL Terminal) wires to 4 post header, slip terminations into the Molex 2.54 mm (0.100”) Pitch SL Crimp Housing per the connection diagram.
6. Build the Hirose connector and slip terminated discrete wires of the Hirose connector into the Molex 2.54 mm (0.100”) Pitch SL Crimp Housing per the connection diagram.
7. Solder or connect 12V DC Power jack to ERG inverter K1958 wire harness included with inverter.
8. Plug in ERG inverter K1958 to the LCD panel.
9. Connect the LCD panel to the Hirose connector from the 3V/5V I/F board. Also connect the touch screen to the built Hirose connector.
10. Plug in 5V DC and 12V DC power supplies to the 3V/5V interface boards and ERG inverter K1958 respectively.
11. Plug in the 3V DC adaptor to the MC9328MX1 ADS.

2.1.2 Block Diagram Using Sharp 10.4” TFT Panel LQ104V1DG51

This panel may be driven directly by the MC9328MX1 ADS I/O 3.3V level signals. The two Vcc inputs of the panel may be directly sourced by the MC9328MX1 ADS Vcc supply. The block diagram for the Sharp 10.4” TFT panel is shown in Figure 2 on page 8.

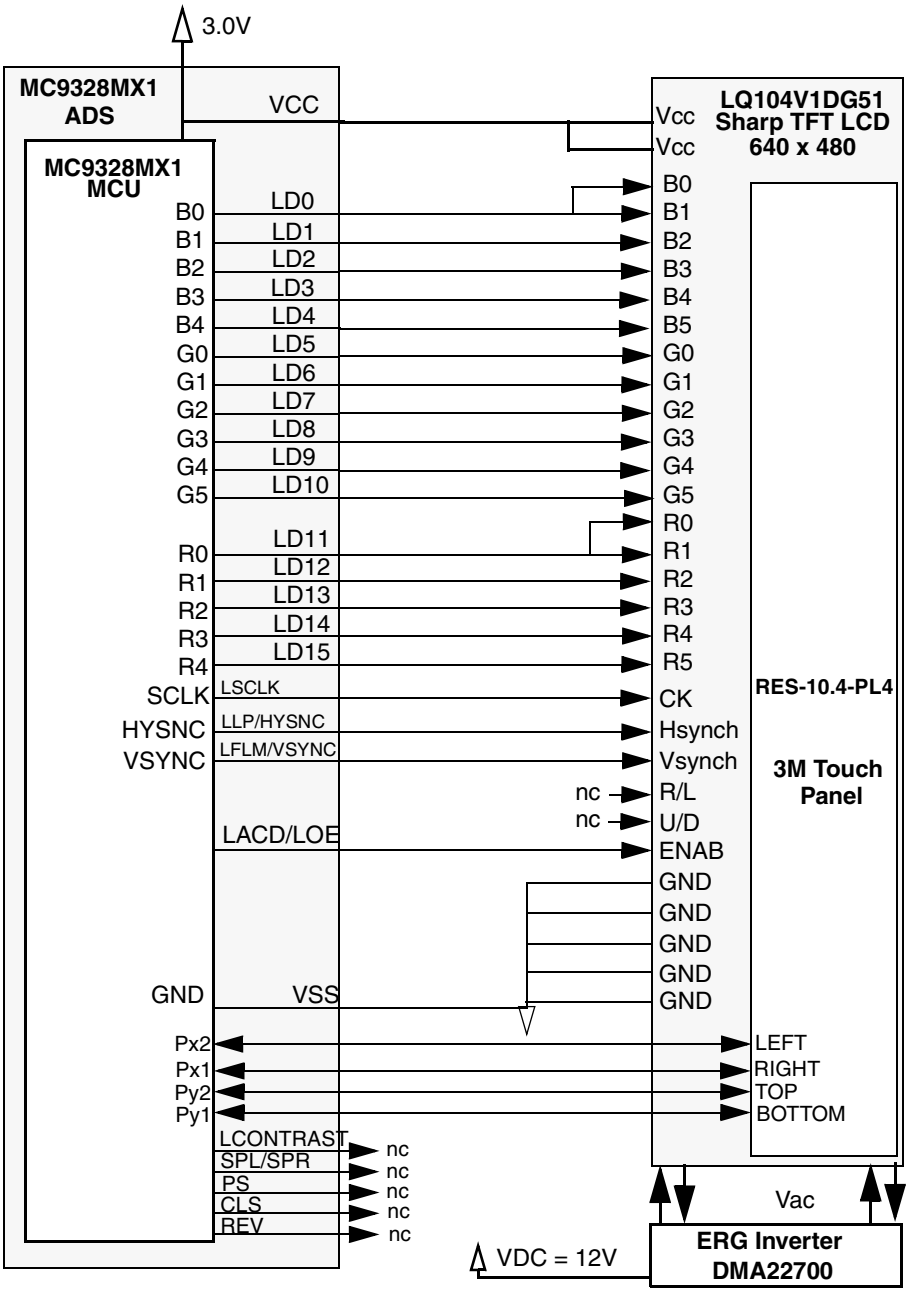

Figure 2. Block Diagram Using Sharp 10.4” TFT Panel LQ104V1DG51

2.1.2.1 Parts List Using Sharp 10.4” TFT Panel LQ104V1DG51

Table 3. Parts List Using Sharp 10.4” TFT Panel LQ104V1DG51

Description	Quantity	Manufacturer Information and Spec Sheet	Notes
MC9328MX1 ADS	1	Freescale Semiconductor Inc. www.freescale.com/imx	—

Table 3. Parts List Using Sharp 10.4” TFT Panel LQ104V1DG51 (continued)

Description	Quantity	Manufacturer Information and Spec Sheet	Notes
3.0 V DC power supply adaptor	1	—	Included with MC9328MX1 ADS
Freescale Semiconductor Inc. MC9328MX1ADS/LQ104V1DG51 Adaptor Cable using DF9M-31S-18D Hirose connector and 0.100” Pitch 4 pin single row male header post	1	International Component Technology www.intcomptech.com	Connects the MC9328MX1 ADS directly with the Sharp Panel and 10.4” Resistive Touch Screen 4 pin female Berg connector P/N 65801-004
LQ104V1DG51 Panel	1	Sharp datasheet LD-13708	May substitute LQ104V1DG11 (datasheet LCY-99102)
RES-10.4-PL4 3M 10.4” Resistive Touch Screen	1	3M/Dynapro www.dynapro.com	May also use R410.412 Resistive Touch Screen
ERG inverter DMA22700	1	ERG www.ergpower.com	Mfg. includes wire harness to connect to 12V DC power jack
H2403305 “pigtail” connector	1	—	DMA22700 to 12V DC supply connector
DPD120080-P5 CUI STACK 12V DC 800 mA power supply	1	DIGIKEY www.digikey.com	—
DC Power Jack 2.1 mm x 5.5 mm	1	PHILMORE	Fry’s Electronics

2.1.2.2 Connection Table for 10.4” Sharp TFT Panel

Table 4. MC9328MX1 ADS Connections to 640×480 10.4” Panel

MC9328MX1 Pin Number and Name on ADS Connector (2x34)		**Sharp 640x480 Panel** Pin Number and Name (Hirose Connector)		**Touch Screen** Pin Number and Name		**Function**
2	VSS	1	GND			
6	LSCLK	2	CK			Clock signal for sampling each data signal
4	LLP/HYSNC	3	HSYNCH			Horizontal Synchronous Signal
5	LFLM/VSYNCH	4	VSYNCH			Vertical Synchronous Signal
2	VSS	5	GND			
18	LD11	6	R0			RED data signal (LSB)
29	LD11	7	R1			RED data signal
18	LD12	8	R2			RED data signal

Table 4. MC9328MX1 ADS Connections to 640×480 10.4” Panel (continued)

MC9328MX1 Pin Number and Name on ADS Connector (2x34)		**Sharp 640x480 Panel** Pin Number and Name (Hirose Connector)		**Touch Screen** Pin Number and Name		**Function**
17	LD13	9	R3			RED data signal
16	LD14	10	R4			RED data signal
15	LD15	11	R5			RED data signal (MSB)
2	VSS	12	GND			
28	LD5	13	G0			GREEN data signal (LSB)
27	LD6	14	G1			GREEN data signal
14	LD7	15	G2			GREEN data signal
13	LD8	16	G3			GREEN data signal
12	LD9	17	G4			GREEN data signal
11	LD10	18	G5			GREEN data signal
2	VSS	19	GND			
10	LD0	20	B0			BLUE data signal (LSB)
25	LD0	21	B1			BLUE data signal
10	LD1	22	B2			BLUE data signal
9	LD2	23	B3			BLUE data signal
8	LD3	24	B4			BLUE data signal
7	LD4	25	B5			BLUE data signal
2	VSS	26	GND			
3	LACD/LOE	27	ENAB			Signal to settle the horizontal display position (driven by LOE)
1	VCC	28	VCC			+5.0V power supply
1	VCC	29	VCC			+5.0V power supply
		30	R/L			Horizontal display mode select signal, not connected-open
		31	U/D			Vertical display mode select signal, not connected-open
33	Py2			1	TOP	Touch panel

Table 4. MC9328MX1 ADS Connections to 640×480 10.4” Panel (continued)

MC9328MX1 Pin Number and Name on ADS Connector (2x34)		Sharp 640x480 Panel Pin Number and Name (Hirose Connector)		Touch Screen Pin Number and Name		Function
34	Py1			2	BOTTOM	Touch panel
31	Px2			3	LEFT	Touch panel
32	Px1			4	RIGHT	Touch panel
19	LCONTRAST					not connected
20	PWMO1					not connected
21	LSPL					not connected
22	REV					not connected
23	PS					not connected
24	CLS					not connected

2.1.2.3 Assembly and Setup Instructions

1. Place touch screen on LCD panel using double sided fixative (3M recommended).
2. Connect the Freescale MC9328MX1 ADS/LQ104V1DG51 adaptor cable to the MC9328MX1 ADS TFT LCD interface 2 × 34 male header, the LCD Panel, and the touch screen.
3. Solder or connect 12 V DC Power jack to ERG inverter DMA22700 wire harness included with inverter.
4. Plug in ERG inverter DMA22700 to the LCD panel.
5. Plug in 12 V DC power supply to the ERG inverter DMA22700 wire harness.
6. Plug in the 3 V DC adaptor to the MC9328MX1 ADS.

3 Software

Both the Sharp 10.4” TFT Panel LQ104V1DG51 and Sharp 6.4” TFT Panel LQ64D343 require similar timings. So they may be initialized using the same script. Depending on the resolution desired the script will change. It is important to know how to make the change.

3.1 Timing and Code Example for 640×480 Resolution on 640×480 Panel

Obviously, the 640 × 480 resolution panels may be driven in 640 × 480 mode. To achieve this, for the panels in this reference design, the MC9328MX1 chip and LCDC (LCD controller) may be set up to provide the Horizontal and Vertical timings to the panel shown in Figure 3 and Figure 4.

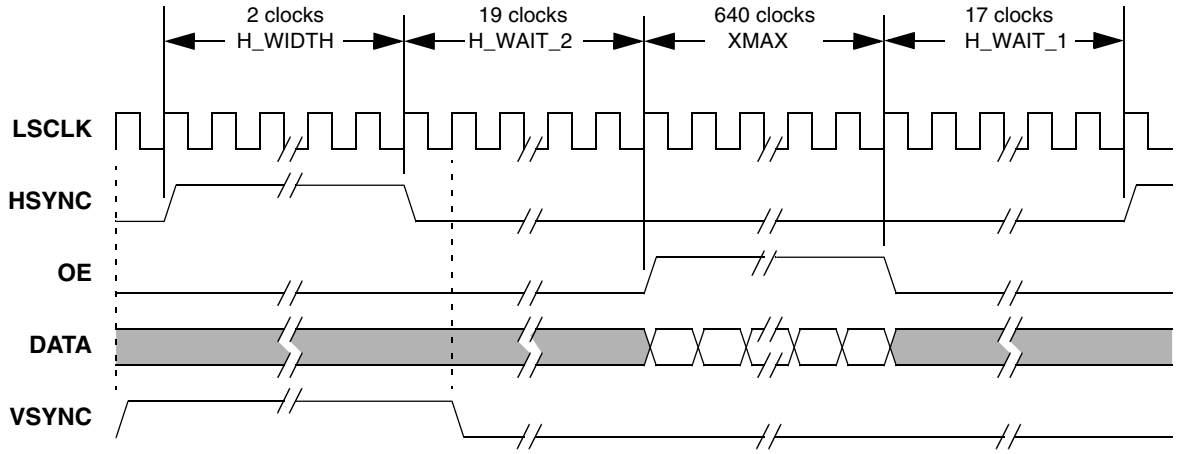

Figure 3. Horizontal Sync Pulse Timing Using 640x480 Resolution

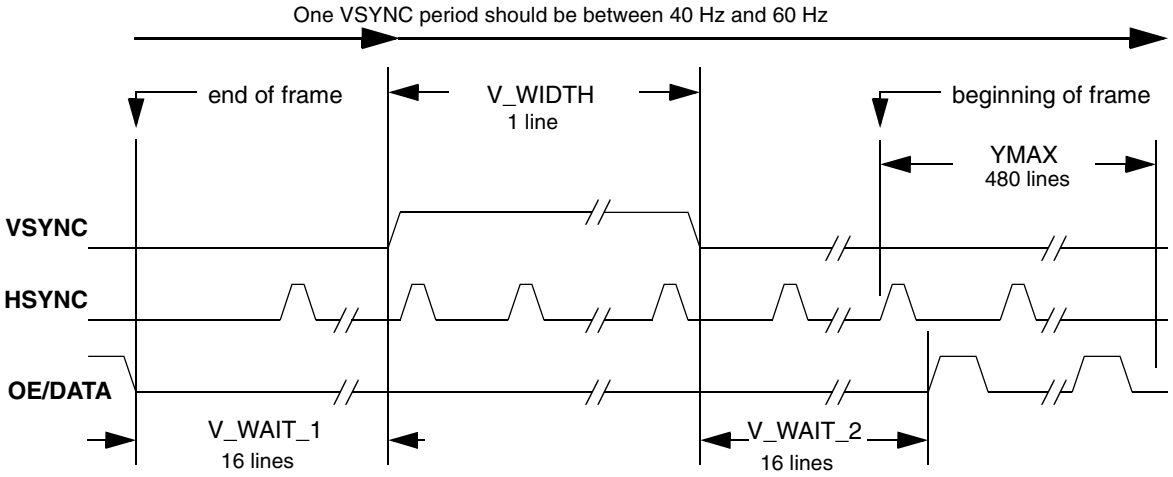

Figure 4. Vertical Sync Pulse Timing Using 640x480 Resolution

Let H_WIDTH, H_WAIT_2, XMAX, H_WAIT_1 be timing labels for the above diagrams which determine specific settings per the MC9328MX1 reference manual. XMAX corresponds to the desired image horizontal width, in this case 640 pixels. Therefore, the Horizontal Period, number of clocks between HSYN assertions, for the panels becomes:

$$\overline{H} = H\_WIDTH + H\_WAIT\_2 + XMAX + H\_WAIT\_1 \qquad \textit{Eqn. 1}$$

$$\overline{H} = (2\ clocks) + (19\ clocks) + (640\ clocks) + (17\ clocks) = 678\ clocks \qquad \textit{Eqn. 2}$$

Let V_WIDTH, V_WAIT_2, YMAX, V_WAIT_1 be timing labels for the above diagrams which determine specific settings per the MC9328MX1 reference manual. YMAX corresponds to the desired image vertical height, in this case 480 pixels. Therefore, the Vertical Period, number of lines between VSYNC assertions, for the panels becomes:

$$\overline{V} = V\_WIDTH + V\_WAIT\_2 + YMAX + V\_WAIT\_1 \qquad \textit{Eqn. 3}$$

$$\overline{V} = (1\ line) + (16\ lines) + (480\ lines) + (16\ lines) = 513\ lines \qquad \textit{Eqn. 4}$$

The Virtual Page Width needs to be set to match the width of the image to be displayed. In this case Virtual Page Width = 640 pixels. The register setting in the MC9328MX1 becomes VPW = 640/2 = 320.

In this timing example, the panel is set up for 640×480 resolution. However, if the customer requires a smaller image vertical height for their application simply changing the YMAX timing from 480 lines to say for example 240 lines will provide 640×240 resolution using this same hardware and initialization script, with exception of the change in vertical height. In this case, the refresh requirement has been decreased and some bandwidth released allowing the interface clock to be reduced while maintaining the 60 Hz refresh rate required by the panels.

NOTE

The refresh rate should be maintained at 60 Hz whenever possible. The 40–60 Hz refresh rate will not produce visual flicker, however this depends on the loading of the CPU while displaying data. If the panel is run at the higher end of the allowable visual margin, say 60 Hz, then there is some margin for OS loading without producing visual flicker. The refresh rate period is defined as the period from one VSYNC pulse assertion to the next assertion.

Example 1 configures the MC9328MX1 ADS to drive the panels discussed here in 640×480 resolution.

Example 1. Code Listing for 640×480 Resolution Display

```
Code Listing for 640×480 Resolution Display
comment ### Select CLKO mux to output HCLK(BCLK) ###
setmem 0x21B000 0x2F00AC03, 32

comment ### Change BCLK (CPUCLK) to 16MHz
comment setmem 0x21B000 0x2F009403, 32

comment ### Change BCLK (CPUCLK) to 24MHz
comment setmem 0x21B000 0x2F008C03, 32

comment ### Change BCLK (CPUCLK) to 32MHz
comment setmem 0x21B000 0x2F008803, 32

comment ### Change BCLK (CPUCLK) to 48MHz
comment setmem 0x21B000 0x2F008403, 32

comment ### Change BCLK (CPUCLK) to 96MHz
setmem 0x21B000 0x2F008003, 32

comment ### Change PerCLK2 (LCDCLK) to 96MHz
comment setmem 0x21B020 0x000B000B, 32

comment ### Change PerCLK2 (LCDCLK) to 48MHz
setmem 0x21B020 0x000B001B, 32

comment ### Change PerCLK2 (LCDCLK) to 32MHz
comment setmem 0x21B020 0x000B002B, 32
```

```
comment ### Change PerCLK2 (LCDCLK) to 16MHz
comment setmem 0x21B020 0x000B005B, 32

comment ### Change PerCLK2 (LCDCLK) to 8MHz
comment setmem 0x21B020 0x000B00BB, 32

comment ### CS0 - boot flash, 32 wait states, 8-bit ###
setmem 0x220000 0x00002000, 32
setmem 0x220004 0x11110301, 32

comment ### CS1 - SRAM, wait states, 32-bit ###
setmem 0x220008 0x00000300, 32
setmem 0x22000C 0x11110601, 32

comment ### CS4 - External UART, 10 wait states, 8-bit ###
setmem 0x220020 0x00000A00, 32
setmem 0x220024 0x11110301, 32


comment ##########################################
comment   INIT FILE FOR SHARP 640X480 LCD DISPLAY
comment ##########################################

comment LCD buffer point to external SRAM
setmem 0x00205000 0x12000000, 32

comment LCD buffer point to eSRAM
comment setmem 0x00205000 0x00300000, 32

comment set LCD display size 640x480
setmem 0x00205004 0x028001E0, 32

comment vpwC480(dec) for 8bpp  40 for 4bpp

comment set vpw to 640/2=320 => 0x140
setmem 0x00205008 0x00000140, 32

comment set cursor position & attributes
setmem 0x0020500C 0x40010001, 32
setmem 0x00205010 0x1F1F0000, 32
setmem 0x00205014 0x0000F800, 32

comment 16 bpp , tft , color,  div by 2
setmem 0x00205018 0xF8E00081, 32

comment h_width, h_wait1, h_wait2
setmem 0x0020501C 0x04001010, 32
```

```
comment v_width, v_wait1, v_wait2
setmem 0x00205020 0x04000022, 32

comment panning offset
setmem 0x00205034 0x00000000, 32

comment ##########################
comment   IO PORT INIT FOR LCD
comment   config PC16 to output port for LCD ON
comment   config PD to functional use for LCD signals
comment ########################################

comment PORT D GIUS
comment clear PORT D for LCD signal
setmem 0x0021C320 0x00000000, 32

comment PORT D GPR
setmem 0x0021C338 0x00000000, 32

comment PORT C GIUS
setmem 0x0021C220 0x00010000, 32

comment PORT C OCR2
setmem 0x0021C208 0x00000003, 32

comment PORT C DDIR
setmem 0x0021C200 0x00010000, 32

comment PORT C GPR
setmem 0x0021C238 0x00010000, 32

comment PORT C DR (data register)
comment set PC16 will turn off LCD
setmem 0x0021C21C 0x00010000, 32


comment ############
comment   LCD ON
comment ############

comment PORT C DR (data register)
comment set PC16 will turn off LCD
setmem 0x0021C21C 0x00010000, 32

comment LCD enabled
setmem 0x00205034 0x0F000002, 32
```

NOTE

This example provides a way to configure the internal clocks of the MC9328MX1 chip, however depending on the application and system requirements the clocks could be different.

3.2 Timing and Code Example for 320×480 Resolution on 640×480 Panel

As an example of an alternate horizontal resolution the 640×480 panels may be operated in 320×480 resolution using the same hardware. Figure 5 and Figure 6 show the Horizontal and Vertical timings to the panel discussed.

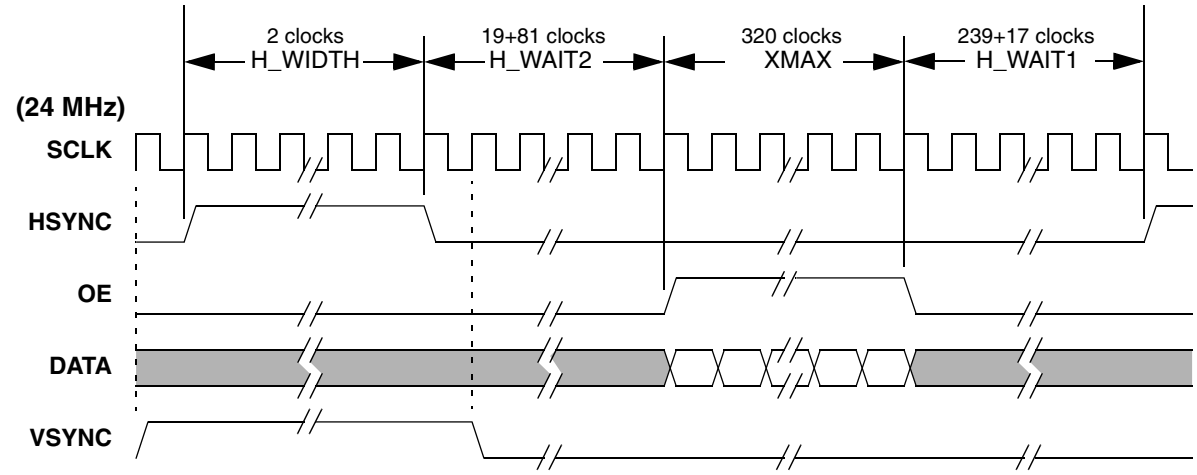

Figure 5. Horizontal Sync Pulse Timing Using 320x480 Resolution

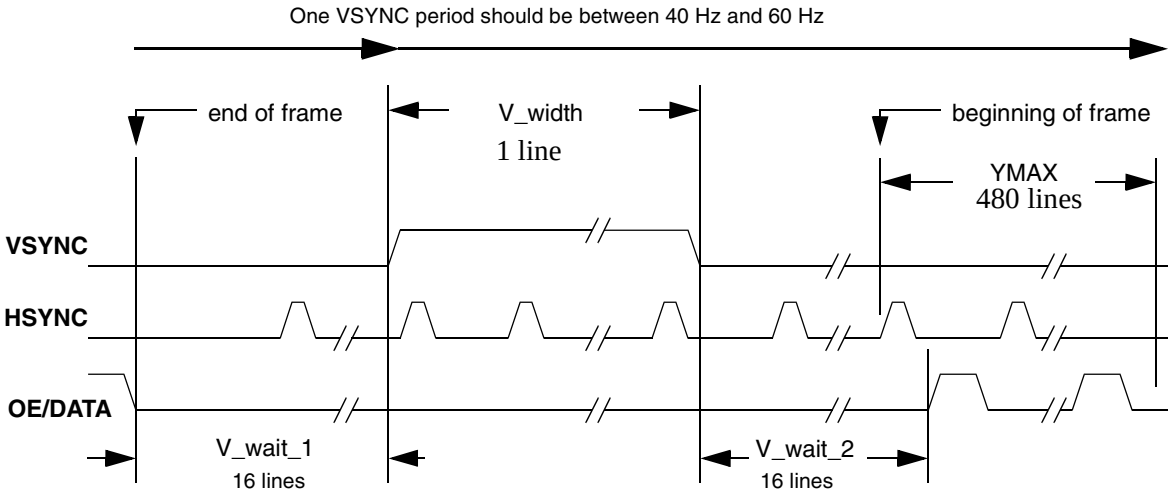

Figure 6. Vertical Sync Pulse Timing Using 320x480 Resolution

Let H_WIDTH, H_WAIT_2, XMAX, H_WAIT_1 be timing labels for the above diagrams which determine specific settings per the MC9328MX1 reference manual. XMAX corresponds to the desired image horizontal width, in this case 320 pixels. However, because the panel physical width size in pixels

is 640 pixels the horizontal period $\overline{H}$ = 678 clocks must be kept constant for the panel to function correctly. Therefore, the Horizontal Period, number of clocks between HSYNC assertions, for the panels becomes:

$$\overline{H} = H\_WIDTH + H\_WAIT\_2 + XMAX + H\_WAIT\_1 \quad \textit{Eqn. 5}$$

$$\overline{H} = (2\ clocks) + (19 + 81\ clocks) + (320\ clocks) + (17 + 239\ clocks) = 678\ clocks \quad \textit{Eqn. 6}$$

The Vertical Period also remains the same:

$$\overline{V} = V\_WIDTH + V\_WAIT\_2 + YMAX + V\_WAIT\_1 \quad \textit{Eqn. 7}$$

$$\overline{V} = (1\ line) + (16\ lines) + (480\ lines) + (16\ lines) = 513\ lines \quad \textit{Eqn. 8}$$

The Virtual Page Width needs to be set to match the width of the image to be displayed. In this case Virtual Page Width = 320 pixels. The register setting in the MC9328MX1 becomes VPW = 320/2 = 160.

In this timing example, the panel is set up for 320×480 resolution. However, if the customer requires a smaller image vertical height for their application simply changing the YMAX timing from 480 lines to say for example 240 lines will provide 320×240 resolution using this same hardware and initialization script, with exception of the change in vertical height. In this case, the refresh requirement has been decreased and some bandwidth released allowing the interface clock to be reduced while maintaining the 60 Hz refresh rate required by the panels. When using horizontal resolution widths less than 640 pixels the region of the display where the panel will display the user's image is known as the active display area. The area of the display where the panel will not display any images is known as the inactive display area.

NOTE

When driving the 640×480 panels in less than 640 pixel horizontal resolution, the last pixel of each line will repeat across the inactive area. This is because the MC9328MX1 LCD controller will hold the LD[15:0] lines at the same state as the last pixel and as the LSCLK keeps toggling, because of the clocks added by H_WAIT_1 and H_WAIT_2, the panel will display those pixels. No bandwidth from the internal system is required while the LCD controller is in the Inactive Display Area.

Example 2 configures the MC9328MX1 ADS to drive the panels discussed here in 320×480 resolution.

Example 2. Code Listing for 320×480 Resolution Display

```
Code Listing for 320X480 Resolution Display
comment ### Select CLKO mux to output HCLK(BCLK) ###
setmem 0x21B000 0x2F00AC03, 32

comment ### Change BCLK (CPUCLK) to 16MHz
comment setmem 0x21B000 0x2F009403, 32

comment ### Change BCLK (CPUCLK) to 24MHz
comment setmem 0x21B000 0x2F008C03, 32

comment ### Change BCLK (CPUCLK) to 32MHz
comment setmem 0x21B000 0x2F008803, 32
```

```
comment ### Change BCLK (CPUCLK) to 48MHz
comment setmem 0x21B000 0x2F008403, 32

comment ### Change BCLK (CPUCLK) to 96MHz
setmem 0x21B000 0x2F008003, 32

comment ### Change PerCLK2 (LCDCLK) to 96MHz
comment setmem 0x21B020 0x000B000B, 32

comment ### Change PerCLK2 (LCDCLK) to 48MHz
setmem 0x21B020 0x000B001B, 32

comment ### Change PerCLK2 (LCDCLK) to 32MHz
comment setmem 0x21B020 0x000B002B, 32

comment ### Change PerCLK2 (LCDCLK) to 16MHz
comment setmem 0x21B020 0x000B005B, 32

comment ### Change PerCLK2 (LCDCLK) to 8MHz
comment setmem 0x21B020 0x000B00BB, 32

comment ### CS0 - boot flash, 32 wait states, 8-bit ###
setmem 0x220000 0x00002000, 32
setmem 0x220004 0x11110301, 32

comment ### CS1 - SRAM, 10 wait states, 32-bit ###
setmem 0x220008 0x00000300, 32
setmem 0x22000C 0x11110601, 32

comment ### CS4 - External UART, 10 wait states, 8-bit ###
setmem 0x220020 0x00000A00, 32
setmem 0x220024 0x11110301, 32

comment ##########################################
comment   INIT FILE FOR SHARP 640X480 LCD DISPLAY in 320x480 mode
comment ##########################################  ~~~~~~~

comment LCD buffer point to external SRAM
setmem 0x00205000 0x12000000, 32

comment LCD buffer point to eSRAM
comment setmem 0x00205000 0x00300000, 32

comment set LCD display size 320x480
setmem 0x00205004 0x014001E0, 32

comment vpwC480(dec) for 8bpp  40 for 4bpp
```

```
comment set vpw to 320/2= 160 => 0xA0
setmem 0x00205008 0x000000a0, 32

comment set cursor position & attributes
setmem 0x0020500C 0x40010001, 32
setmem 0x00205010 0x1F1F0000, 32
setmem 0x00205014 0x0000F800, 32

comment 16 bpp , tft , color,
setmem 0x00205018 0xF8E00081, 32

comment h_width, h_wait1, h_wait2
setmem 0x0020501C 0x0400FF64, 32

comment v_width, v_wait1, v_wait2
setmem 0x00205020 0x04000022, 32

comment panning offset
setmem 0x00205034 0x00000000, 32

comment ##########################
comment   IO PORT INIT FOR LCD
comment   config PC16 to output port for LCD ON
comment   config PD to functional use for LCD signals
comment ########################################

comment PORT D GIUS
comment clear PORT D for LCD signal
setmem 0x0021C320 0x00000000, 32

comment PORT D GPR
setmem 0x0021C338 0x00000000, 32

comment PORT C GIUS
setmem 0x0021C220 0x00010000, 32

comment PORT C OCR2
setmem 0x0021C208 0x00000003, 32

comment PORT C DDIR
setmem 0x0021C200 0x00010000, 32

comment PORT C GPR
setmem 0x0021C238 0x00010000, 32

comment PORT C DR (data register)
comment set PC16 will turn off LCD
setmem 0x0021C21C 0x00010000, 32
```

```
comment ############
comment   LCD ON
comment ############

comment PORT C DR (data register)
comment set PC16 will turn off LCD
setmem 0x0021C21C 0x00010000, 32

comment LCD enabled
setmem 0x00205034 0x0F000002, 32
```

3.3 Summary on Varying Resolutions Using This Hardware

The important points to remember when reconfiguring the panels chosen here to support varying resolutions less than or equal to 640×480 are:

1. The horizontal width of the display area used by the application may be less than or equal to 640 pixels wide. However, the Horizontal Period $\overline{H}$ must be respected when reconfiguring the MC9328MX1 ADS registers.
2. The Virtual Page Width must be set to the width of the image used. To determine the register setting refer to the MC9328MX1 reference manual.
3. The vertical height of the display area used by the application may be less than or equal to 480 lines tall. Therefore the same Vertical Period $\overline{V}$ as explained in the example 640×480 resolution and 320×480 resolution will not be the same if the vertical height of the display area is changed. The Vertical Period will remain calculated as follows:

$$\overline{V} = V\_WIDTH + V\_WAIT\_2 + YMAX + V\_WAIT\_1 \qquad \textit{Eqn. 9}$$

4. The Vertical Period $\overline{V}$ may be between 40 Hz and 60 Hz to provide flickerless operation to the naked eye. However it is recommended to drive the panel at 60 Hz refresh. This period may be adjusted by changing the interface clock setting to the panel, LSCLK, down if there is sufficient bandwidth in the system for the current resolution operation. As an example a 640×480 resolution will require more bandwidth than a 320×480 resolution even though they require the same Horizontal Period H. Therefore in the 320×480 case, the refresh rate or Vertical Period $\overline{V}$ may be adjusted down slightly using the PCD divider to control the LSCLK frequency and hence the Vertical Period. W_WIDTH, W_WAIT_1, and V_WAIT_2 are fixed for a given resolution and are not used to save bandwidth.
5. The clock input to the LCD Controller of the MC9328MX1 chip, LCD_CLK, may function up to 96 MHz, however this is application specific. Routing problems causing long delays may affect the panel performance at this frequency. It is important to note however, that to prevent flickering, the panel must be operated at between 40 Hz and 60 Hz refresh, 60 Hz recommended. The setting for LCD_CLK directly affects the refresh rate.

3.4 Testing-Out the Display

The following sections describe briefly how to test-out the hardware whether using the Sharp 6.4” TFT Panel LQ64D343 or the Sharp 10.4” TFT Panel LQ104V1DG51.

3.4.1 Creating a Proper Test Image to Download

Not only will the user want to test the display for correct colors, but also test the framing of the image within the display area. For this purpose it is important to create the proper test image. Using a Windows based application for editing bitmaps can do the job. Also, a conversion program to convert the bitmap image to binary for downloading to the MC9328MX1 ADS RAM is required. The author recommends the following programs for these purposes:

- Windows Paint Brush application—available on most PC’s
- bmp24to16.exe utility for the MC9328MX1 ADS—available from: http://www.freescale.com/imx

3.4.1.1 Proper Test Bitmap Creation

Figure 7 on page 22 shows what a test image might look like to test-out 320×480 resolution. The image can be created using the Paint Brush application. To obtain the correct resolution in Paint Brush use the menu option “Image” and select “Attributes” to set the image Width and Height. The image resolution should match the panel resolution that will be displayed, not necessarily the physical panel size.

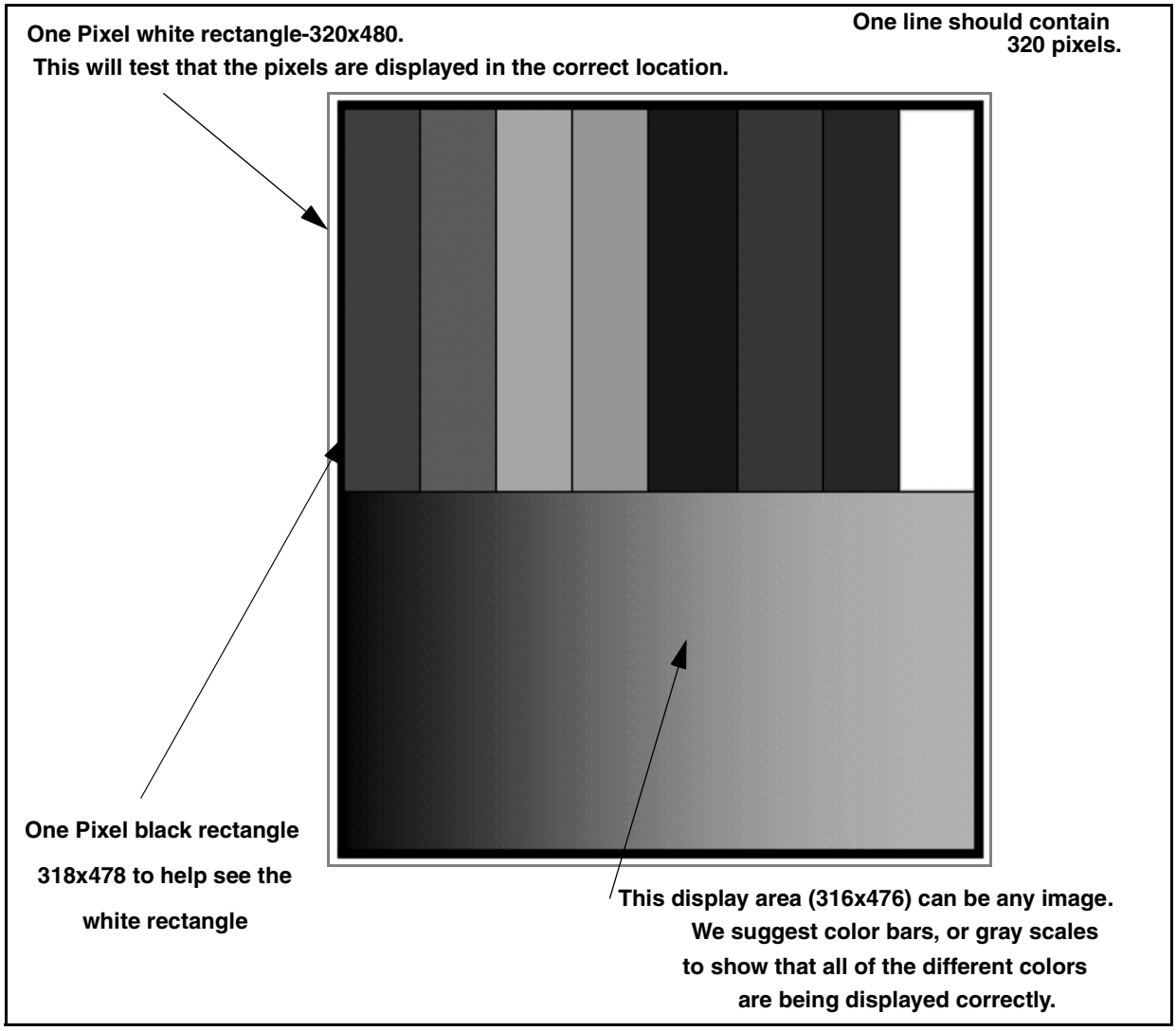

Figure 7. Example 320×480 Bitmap Test Image

3.4.1.2 bmp24to16.exe Conversion Utility

Use the bmp24to16.exe utility from Freescale to convert the bmp format image to binary format for direct downloading into RAM on the MC9328MX1 ADS. The instructions follow:

```
************************************************************
* BITMAP 24-BIT TO 16-BIT (5-6-5) CONVERTOR version 0.2      *
* Note : Gamma Correction is applied to reduce posterization *
************************************************************

usage   : bmp24to16 [file_in] [file_out] [file_dump]
                    [lcdc_endian (L = little, B = big)]
                    [gamma factor (0.0 <= gFactor <= 1.0)]

example : bmp24to16 test.bmp test.bin dump.bmp B 0.8
```

3.4.2 Initializing the MC9328MX1 ADS

Using the ARM® eXtended Debugger AXD, download the initialization script provided in Example 1 or Example 2 after saving those scripts to a text file, named—for example, init_640×480.txt. The command to use is “obey”, for example:

```
Debug> obey init_640x480.txt
```

Using either of the scripts in Example 1 or Example 2, at this point the LCD should have a RED cursor on the upper left had corner of the display. The display area will display random data but the entire display should be stable (for example, not flickering nor with strange artifacts). The address used in the example scripts is 0x12000000.

3.4.3 Downloading the Image

The binary image created from the original bmp image may be downloaded directly to RAM using the AXD “File/Load Memory From File” command. Please note that the address at which the image will be downloaded must be specified, and that this address must match the address in the LSSA register initialized by the initialization script. Using other debuggers such as Metrowerks Codewarrior 2.1 which offers a memory (SDRAM, Flash) writing tool may be used as well.

4 Conclusion

This application note provides a reference design for supporting software development using the MC9328MX1 ADS if the customer requires a variety of resolutions for their application. It has been shown that panels with 5V or 3V interfaces may be used, with the appropriate hardware, to create a flexible platform for developing software.

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