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Interfacing the MSC8101 to SDRAM on the MSC8101ADS

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Synchronous DRAM (SDRAM) is one of the most cost effective read/write memories on the market, offering high-performance throughput with the cost benefits of a commodity item. In synchronous DRAM, all the memory signal timing relates to a single clock that allows SDRAM to provide significantly faster access time than DRAM.

This application note discusses the interface between the Freescale MSC8101 memory controller (SDRAM machine) and an example JEDEC-compatible MICRON SDRAM device, which is referred to as the MT48LC2M32B2TG device. It begins with an overview of SDRAM basics, including the signals for interfacing an SDRAM device to the MSC8101 device, and then discusses the MSC8101 (DSP side) SDRAM machine. Finally, the application note shows how to initialize SDRAM using the MSC8101 SDRAM machine.

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1 SDRAM Machine Basics

Figure 1 shows the MSC8101 memory controller (MEMC), which consists of three user-programmable machines (UPMs), one general-purpose chip-select machine (GPCM), and one SDRAM machine. The SDRAM machine is available only on the system bus, which can assign memory banks to the SDRAM machine. Features of the SDRAM machine include:

- Control functions and signals for a glueless connection to JEDEC-compliant SDRAM devices

- Two types of page mode, each selectable per memory bank: back-to-back page mode for consecutive and back-to-back accesses and page mode for intermittent accesses
- 2-, 4-, and 8-way bank interleaving
- An SDRAM port size of 64 bits, 32 bits, 16 bits, or 8 bits
- External address and/or command line buffering

The SDRAM machine operates in one of two bus modes, Single-Master Bus mode and Multi-Master Bus mode. In Single-Master Bus mode, the MSC8101 device is the only master on the system bus, and the MSC8101 device interfaces directly to memory and slave peripherals. It sends address and control signals for a direct, glueless interface to the SDRAM. There is no need for external address latching because the MSC8101 MEMC handles address multiplexing.

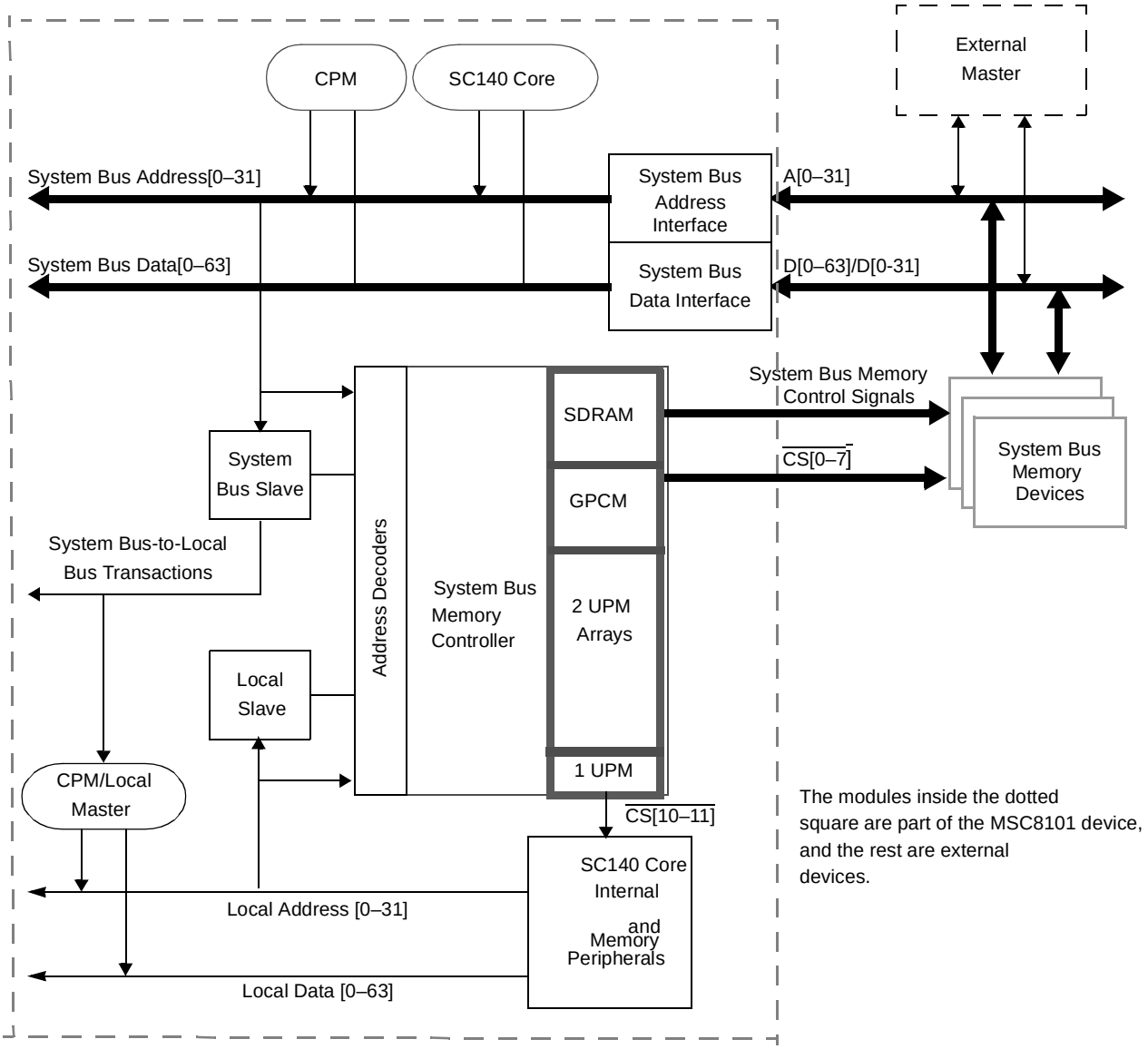

Figure 1. MSC8101 Memory Controller

Figure 2 depicts Single-Master Bus mode. In system bus Multi-Master Bus mode, there are separate address and data tenure phases during which the address is not driven for the entire bus transaction, so internal address multiplexing is not used. Furthermore, external logic must latch the address and multiplex the columns and row addresses to the SDRAM device at the appropriate time.Thus, the MSC8101 uses the Address Latch Enable (ALE) and Select Pin (SDMUX) signals to control the interface between the MSC8101 and SDRAM devices. This application note focuses on the SDRAM hardware interconnect for Single-Master Bus mode.

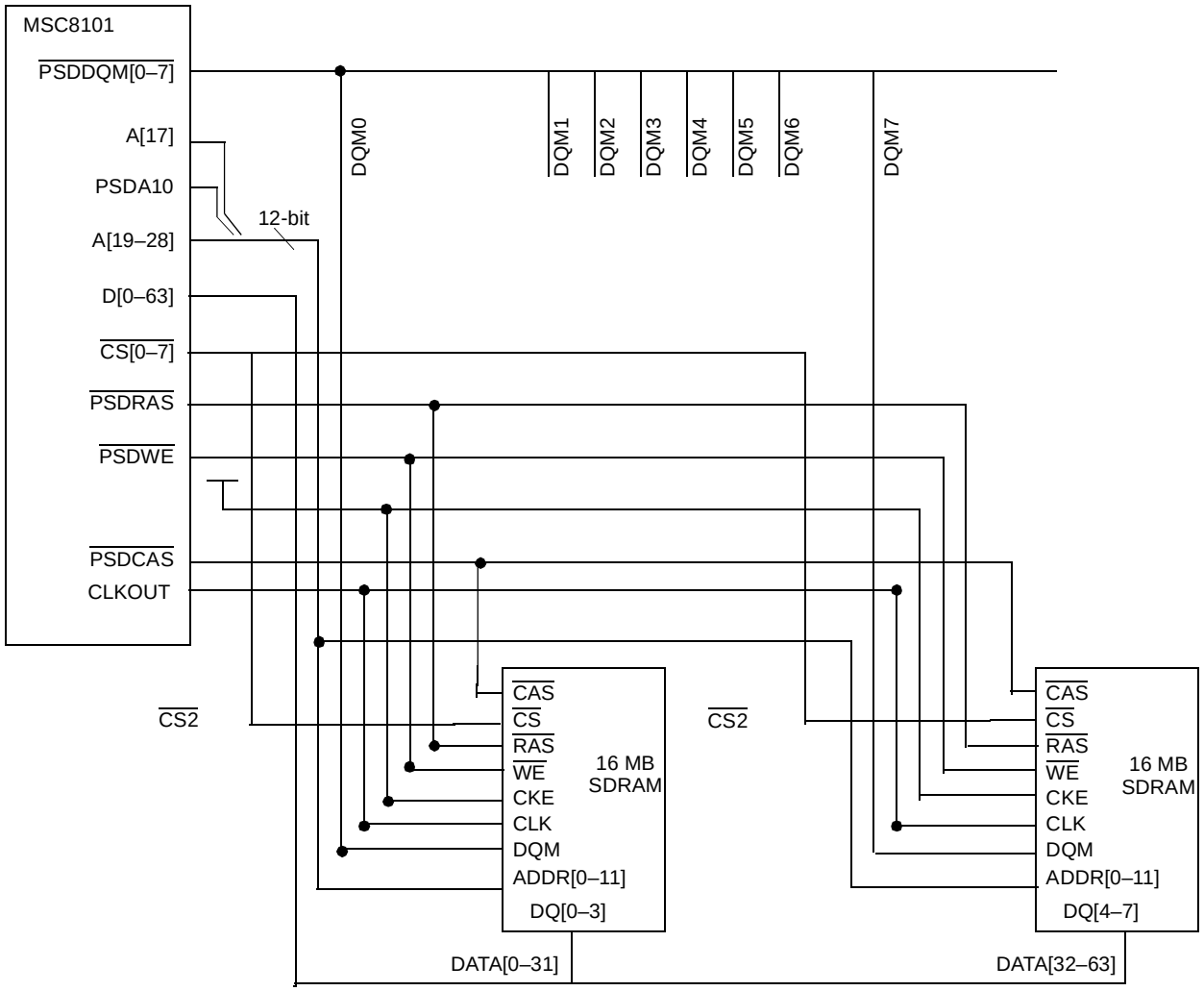

Figure 2. Single-Bus Mode SDRAM Hardware Interconnect to MSC8101 SDRAM Machine[1]

Table 1 lists the key components of the SDRAM architecture of the SDRAM device that connects to the MSC8101 memory controller SDRAM machine.

1. On the MSC8101ADS, the CKE signal of one SDRAM module is tied low for a 32-bit wide bus.

Table 1. SDRAM Architecture

Component	Description
Clock	The clock is an oscillator that toggles between 0 volts and V_{CC} (V_{CC} = 3.3 volts in this case). The period of the clock is the time to complete one cycle and is the inverse of the frequency. For the MSC8101, SDRAM read and write operations are synchronized to the system bus clock.
Command Control	The MT48LC2M32B2TG SDRAM device uses 4-bit long command words. These command control signals are inputs that control the SDRAM device. The command decoder monitors $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ to determine which command to execute
Bank Architecture	The SDRAM memory array is divided into two or more banks so that one bank of the memory array can precharge while the other bank is accessed. This scheme eliminates precharge latency and effectively increases the bandwidth.
Pipelined Operation	The MT48LC2M32B2TG SDRAM device employs a three-stage pipeline that allows new memory accesses to be initiated before the preceding access completes. When the pipeline is full, data can be accessed on every clock cycle. Along with burst mode access, this feature significantly improves data transfer performance.
A10/Auto Precharge	During ACTIVE operation, A[0–10] provide row address information. During read and write operations, A10 pulled high enables the auto precharge feature, and A10 pulled low disables it. BA[0–1] determine which bank is being read from or written to.
Refresh and Refresh Counter	During the refresh operation the SDRAM auto refreshes if Clock Enable (CKE) is high; it self refreshes if CKE is low. A refresh counter controls row addressing and tracks the next row number to be refreshed in preparation for the next refresh command. When the MSC8101ADS board is configured for a 32-bit bus mode, one SDRAM CKE signal is tied low. When the CKE signal is tied low, the SDRAM device can retain its values while it is in self refresh mode.
$\overline{CAS}$ Latency	The MSC8101 SDRAM machine accesses a row of the memory matrix by putting an address on the memory address pins and activating the $\overline{RAS}$ signal. After a defined number of clock cycles (known as $\overline{RAS}$-to-$\overline{CAS}$ delay), the column address is put on the address pins, and the $\overline{CAS}$ signal is activated to access the correct column of the memory matrix. Finally, after another defined number of clock cycles ($\overline{CAS}$ latency), the data appears on the pins of the RAM.

2 MT48LC2M32B2TG SDRAM Device

The MT48LC2M32B2TG SDRAM device contains a mode register that is initialized at power-up (see **Figure 3**). This register configures basic SDRAM device operation, such as the following:

- $\overline{CAS}$ latency (1, 2, or 3)
- Burst length (4 beats for 64-bit and 16-bit port sizes, 8 beats for 32-bit and 8-bit port sizes)
- Burst type (sequential or interleaved)

The burst operation uses an on-chip burst counter that increments the column addresses, yielding very fast burst accesses.

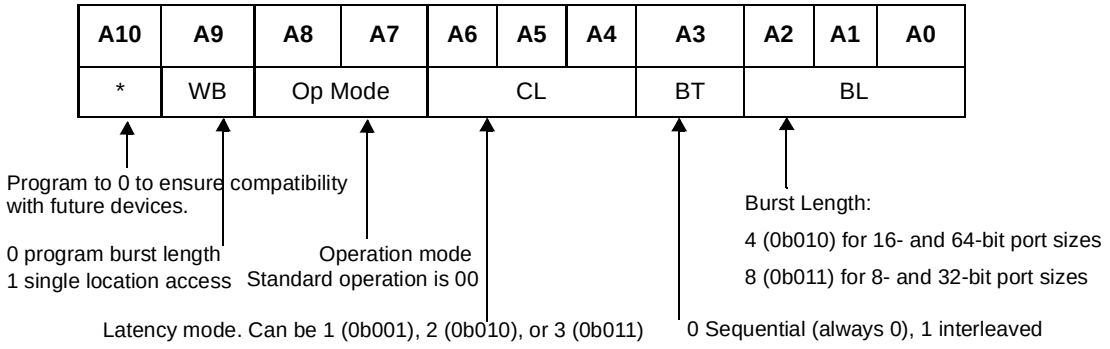

Figure 3. Mode Register Definition

When the Mode Register Set (MRS) command is issued during SDRAM initialization, the MSC8101 PSDMR[2–4]:OP field must contain a value of 011 to initialize the SDRAM (see **Table 22** for details). To program the SDRAM device for a $\overline{\text{CAS}}$ latency of 2- and 8-beat bursts in Single-Master Bus mode with a 32-bit port size, the bits in the MSC8101 PSDMR register must be configured as follows:

- PSDMR[23]:BL = 1
- PSDMR[30–31]:CL = 010

When WB (shown in **Figure 3**) is cleared, the burst length programmed via BL applies to both read and write bursts. When WB is set to 1, the programmed burst length applies to read bursts, but write bursts are single location (non burst) access. To select the Normal operating mode, assign the SDRAM mode register OP mode bits (8 and 7) a value of 00. Other combinations of values are reserved for future use.

To program the SDRAM device for a $\overline{\text{CAS}}$ latency of 2 and burst lengths of 8 beats in Multi-Master Bus mode, these settings must be also be in effect. Also, the value in the SDRAM register is 0x23, which requires a write to the mode register at address 0x20000000 + 0x8C. The port size is 32 bits because the SDRAM Mode Register is shifted by two bits (A[30–31]) to account for the port size settings (see **Figure 4**).

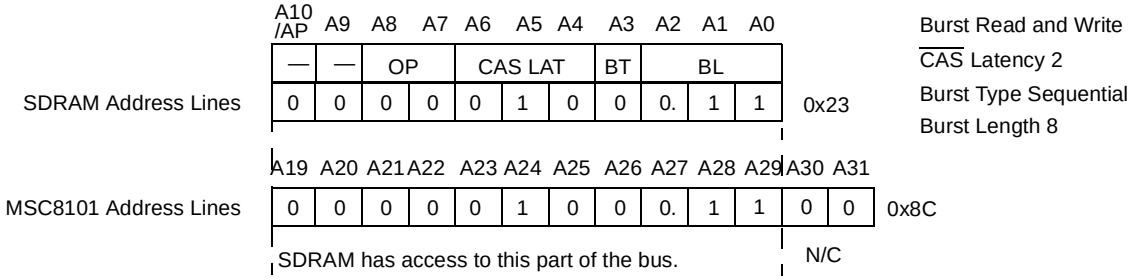

Figure 4. SDRAM Mode Register Programming Example for 32-Bit Port Size

2.1 SDRAM Main Interface Commands

The MSC8101 device performs all accesses to SDRAM in compliance with JEDEC-standard SDRAM interface commands. The SDRAM device samples command and data inputs on the rising edge of the MSC8101 bus clock. Data at the output of the SDRAM device must also be sampled on the rising edge of the MSC8101 bus clock. A successful read/write transaction proceeds as follows:

- ACTIVATE. Occurs when a new row in the bank is accessed. The row is transferred to the page data register. The ACTIVATE command opens (or activates) a row in a particular bank for a subsequent access.
- READ. Occurs when data is transferred from the SDRAM page data register to the data bus.The READ command initiates a burst read access to an active row. The value on the BA[0–1] inputs selects the bank, and the address on inputs A[0–7] selects the starting column location.
- WRITE. Occurs when data is transferred from the data bus to the SDRAM page data register. The WRITE command initiates a burst write access to an active row. The value on the BA[0–1] inputs selects the bank, and the address provided on inputs A[0–7] selects the starting column location.
- PRECHARGE. Deactivates the open row in a particular bank or the open row in all banks. This operation occurs when data is written back to SDRAM from the page data register. The row in SDRAM must be precharged before the data is written. A10 determines whether auto precharge is used. If auto precharge is selected, the accessed row is precharged at the end of the read or write burst; if auto precharge is not selected, the row remains open for subsequent accesses.
- AUTO REFERESH. Used during normal operation of the SDRAM. The internal refresh controller generates the addressing, so the address bits have a value of “Don’t Care” when an auto refresh command executes. The SDRAM memory requires 4,096 auto refresh cycles every 64 µs, regardless of the width option selected. Providing a distributed AUTO REFRESH command every 15.625 µs meets the refresh requirement and ensures that each row is refreshed.

2.2 SDRAM Operations

Table 2 shows the functions of the SDRAM device and the pins associated with them.

Table 2. SDRAM Truth Table

Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	DQM	DQs
Command Inhibit (NOP)	H	X	X	X	X	X	X
No Operation (NOP)	L	H	H	H	X	X	X
Active (Select bank and activate Row)	L	L	H	L	Bank/Row	X	X
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	X	X
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	H/L	Valid
Burst terminate	L	H	L	H	Code	X	ACTIVE
PRECHARGE (Deactivate row in bank or banks)	L	H	L	L	X	Code	X
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X
LOAD MODE REGISTER	L	L	L	L	X	OPCODE	X
Write Enable/Output Enable						L	High Z
Write Inhibit/Output High-Z						H	ACTIVE

Following are important points about these commands to keep in mind:

- CKE is high for all SDRAM commands except SELF REFRESH.
- During load mode register operation, A[0–10] define the opcode written to the SDRAM Mode Register.
- During active operation, A[0–10] provide the row address, and BA[0–1] determine which bank is active.
- During read and write operation, A[0–7] provide the column address. A10 sampled high enables the auto precharge feature, and A10 sampled low disables it. BA[0–1] determine which bank is read or written.
- During precharge operation, A10 LOW: BA0 and BA1 determine which bank is precharged. A10 HIGH: All banks are precharged, and BA0 and BA1 are “Don't care.”
- During a refresh operation, auto refreshes occur if CKE is held high, and self refreshes occur if CKE is held low.
- During refresh operation, an internal refresh counter controls row addressing; all inputs and I/Os are “Don't care” except for CKE.
- During write inhibit/output high Z operations, the DQ signals s are activated or deactivated during writes (zero-clock delay) and reads (two-clock delay). DQM0 controls DQ[0–7]; DQM1 controls DQ[8–15]; DQM2 controls DQ[16–23]; and DQM3 controls DQ[24–31].

2.3 SDRAM Row and Column Addressing

SDRAM is usually based on a 2-, 4-, or 8-bank architecture. The Micron MT48LC2M32B2TG consists of 4 banks. BA[0–1] are bank address inputs that define the bank to which the ACTIVE, READ, WRITE, or PRECHARGE command is applied. Bank select lines are controlled using the Bus Configuration Register (BCR). When BCR[EAV] is cleared, bank select signals are driven on system bus address lines. There is no full address visibility. When BCR[EAV] is set, bank select signals are not driven on the address bus. Bank select lines are used to drive the BA[0–1] signals. You can use the address lines or BNKSEL to drive the BA[0–1] signals. BNKSEL signals can be used to drive bank select signals in single or multi-master environments.

The row address lines are used to activate a specific bank for commands such as READ, WRITE, or PRECHARGE. MT48LC2M32B2TG uses address inputs A[0–10] as row address lines to activate a specific bank. The column address lines are used to issue a READ or WRITE command based on the status of the $\overline{\text{WE}}$ signal. If $\overline{\text{WE}}$ is high, a read operation is applied on the bank, and if $\overline{\text{WE}}$ is low, a write operation is applied instead. MT48LC2M32B2TG uses address inputs A[0–7] as column address lines to fetch data during a read or write operation to a specific area in memory when a READ/WRITE command executes.

2.4 SDRAM Timing Diagrams

This section covers the timing diagrams of the MSC8101’s SDRAM machine interface to SDRAM during read, write, read burst and write burst operations.

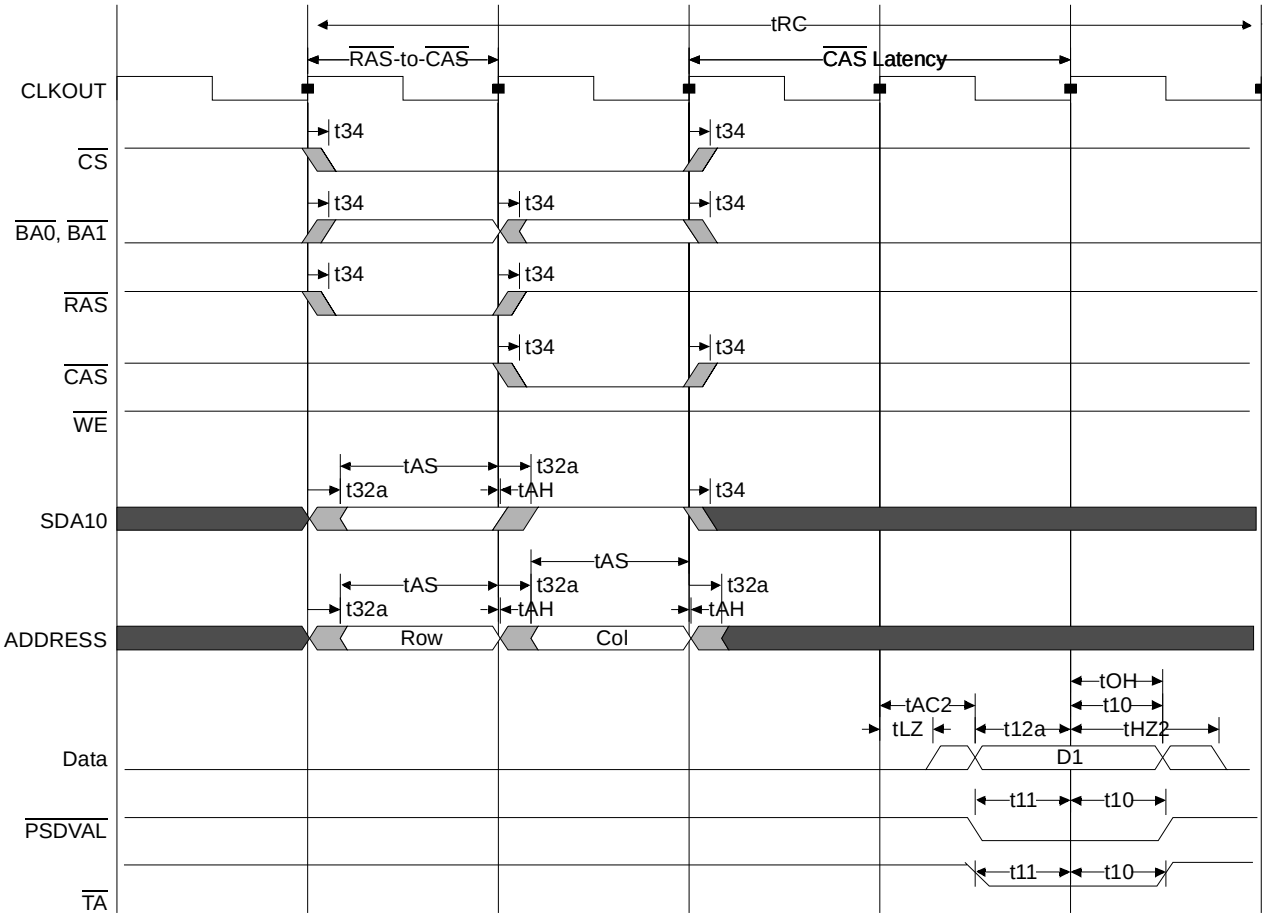

Figure 5. Single Read Transaction

Table 3. Single Read Transaction

Name	Min	Max	Comment
tAC2		8	Access time from CLK (positive edge) with latency of 2
tLZ	1		Data-out low-impedance time
t32a	0.5	8.5	Address bus/Address attributes/$\overline{\text{GBL}}$ delay from CLKIN rising edge
t12a	4.55		Data bus setup time before CLKIN rising edge - normal mode
t11	5		$\overline{\text{AACK}}$/$\overline{\text{ARTRY}}$/$\overline{\text{TA}}$/$\overline{\text{TEA}}$/$\overline{\text{DBG}}$/$\overline{\text{BG}}$/$\overline{\text{BR}}$ set-up time before the CLKIN rising edge
tOH	2.5		Data-out hold time
tHZ2		8	Data-out high-impedance time
t10	0.5		Hold time for all signals after the CLKIN rising edge
tAS	2		Address set-up time
tAH	1		Address hold time

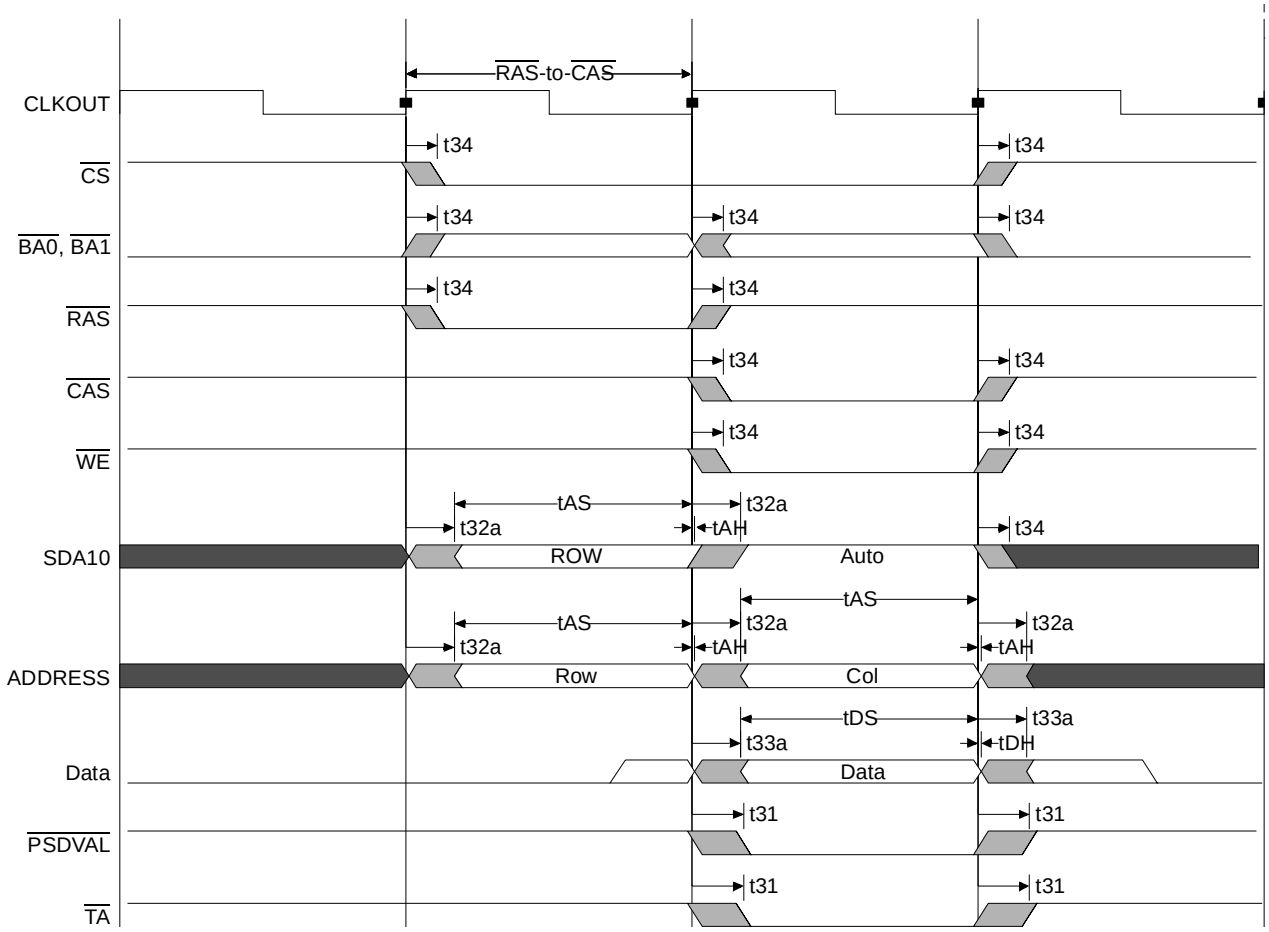

Figure 6. Write Transaction

Table 4. Write Transaction to SDRAM

Name	Min	Max	Comment
t34	0.5	5.5	Memory controller signals/ALE delay from CLKIN rising edge
t32a	0.5	8.5	Address bus/Address attributes/$\overline{\text{GBL}}$ delay from CLKIN rising edge
t31	0.5	9	$\overline{\text{PSDVAL}}$/$\overline{\text{TEA}}$/$\overline{\text{TA}}$ delay from CLKIN rising edge.
t33a	0.5	8.5	Data bus delay from CLKIN rising edge
tDS	2		Data-in set-up time
tDH	1		Data-in hold time
tAS	2		Address set-up time
tAH	1		Address hold time

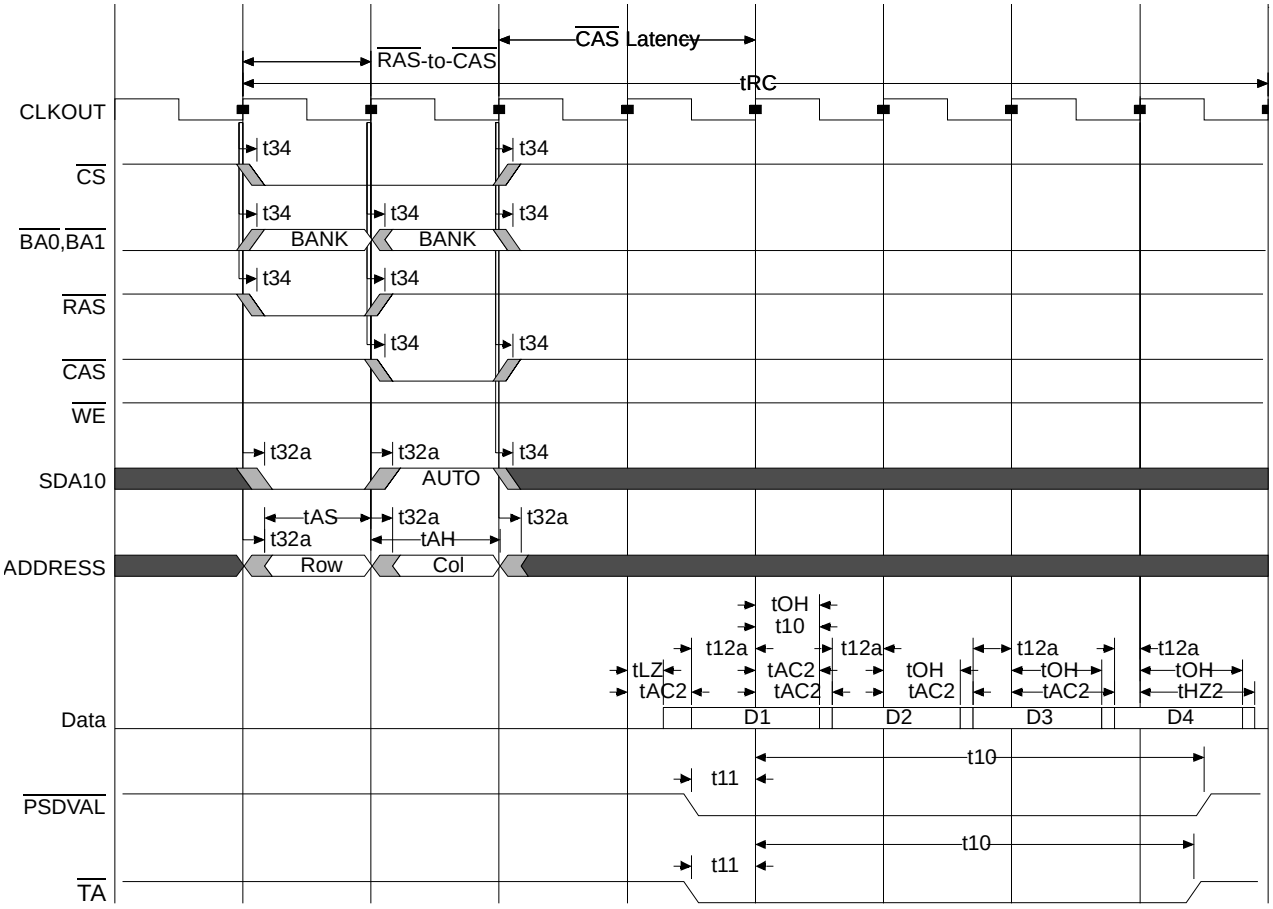

Figure 7. Read Burst from SDRAM

Table 5. Read Burst from SDRAM

Name	Min	Max	Comment
tAC2		8	Access time from CLK (positive edge) with latency of 2
tLZ	1		Data-out low-impedance time
tOH	2.5		Data-out hold time
t34	0.5	5.5	Memory controller signals/ALE delay from CLKIN rising edge
t32a	0.5	8.5	Address bus/Address attributes/$\overline{GBL}$ delay from CLKIN rising edge
t12a	4.55		Data bus set-up time before CLKIN rising edge, normal mode
t10	0.5		Hold time for all signals after CLKIN rising edge
t11	5		$\overline{AACK}$/$\overline{ARTRY}$/$\overline{TA}$/$\overline{TEA}$/$\overline{DBG}$/$\overline{BG}$/$\overline{BR}$ set-up time before the CLKIN rising edge
tHZ2		8	Data-out high-impedance time
tAS	2		Address set-up time
tAH	1		Address hold time

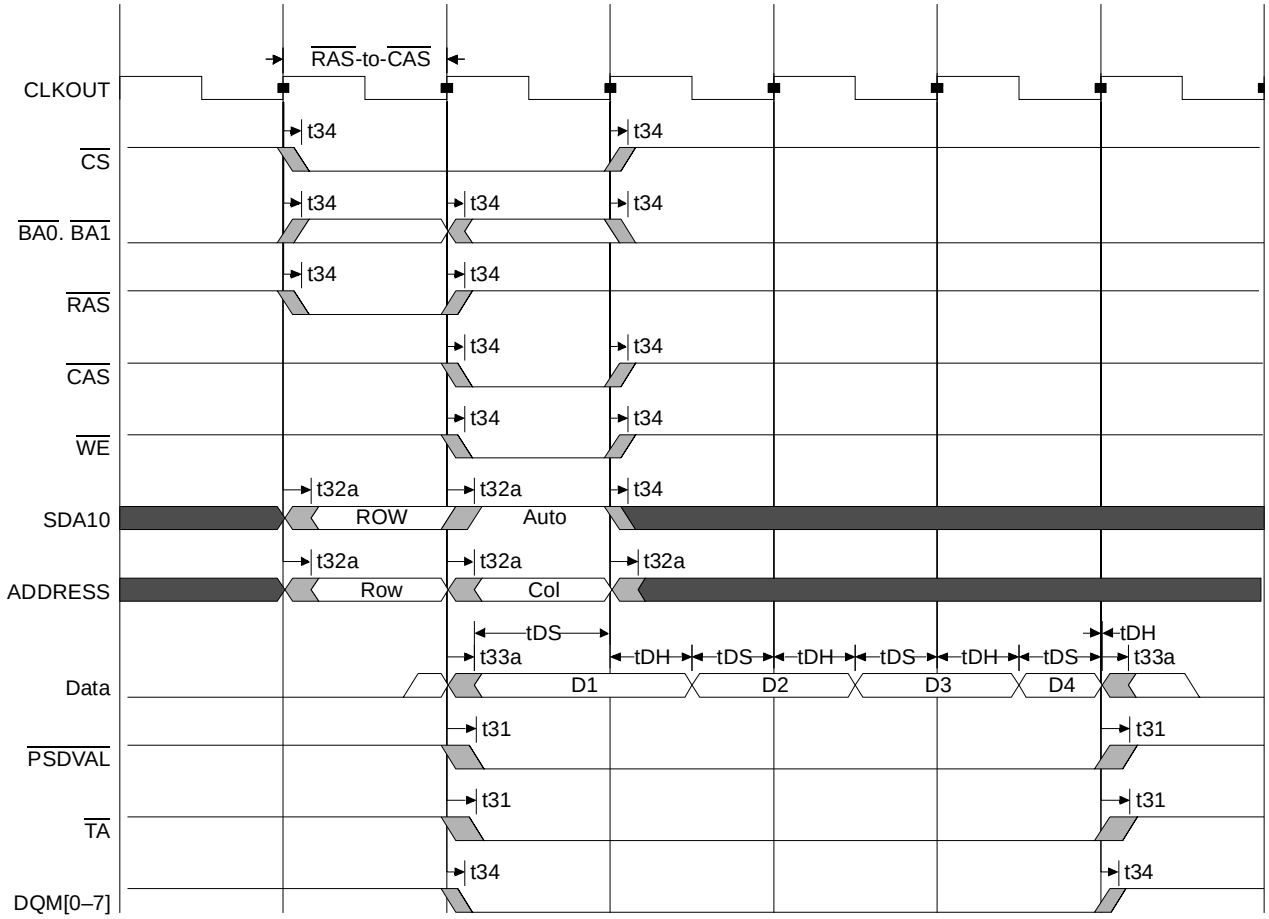

Figure 8. Write Burst to SDRAM

Table 6. Write Burst to SDRAM

Name	Min	Max	Comment
t34	0.5	5.5	Memory controller signals/ALE delay from CLKIN rising edge
t32a	0.5	8.5	Address bus/Address attributes/$\overline{\text{GBL}}$ delay from CLKIN rising edge
t34	0.5	5.5	Memory controller signals/ALE delay from CLKIN rising edge
t33a	0.5	8.5	Data bus delay from CLKIN rising edge
t31	0.5	9	$\overline{\text{PSDVAL}}$/$\overline{\text{TEA}}$/$\overline{\text{TA}}$ delay from CLKIN rising edge.
tDS	2		Data-in set-up time
tDH	1		Data-in hold time

3 Programming the MSC8101 SDRAM Machine

This section discusses how to interface the MICRON MT48LC2M32B2 SDRAM to the MSC8101 SDRAM machine. To program the SDRAM machine to communicate with the SDRAM correctly, complete the following steps:

1. Issue a precharge command to all banks.
2. Issue eight auto refreshes.
3. Program the SDRAM device mode register.

3.1 Selecting the SDRAM Machine

The MT48LC2M32B2 has 11 row address lines and 8 column address lines. The defined SDRAM base address is written to the MSC8101 BRn (Base register 0–7). The SDRAM bank size is written to the MSC8101 ORn (Option register 0–7). Each time a bus cycle access is requested on the system bus, the access address is compared with the addresses of all memory controller banks. If a match occurs, for example, on memory controller bank 2, BR2 and OR2 are selected (since BR2[MSEL] is set to the SDRAM machine), and the attributes defined in BR2 and OR2 are used to control the memory access.

3.2 Page Hit Checking

The SDRAM machine supports page mode operation. Each time a page is activated on the SDRAM device, the SDRAM machine stores its address in a page register. The page information, which the user writes to the ORn register, is used along with the bank size to compare page bits of the address to the page register each time a bus cycle access is requested. If a match occurs together with a bank match, the bus cycle is defined as a page hit. The SDRAM machine automatically closes an open page if the bus becomes idle, unless ORn [PMSEL] is set.

3.3 Partitioning the System Bus

This section discusses two types of interleaving, page-based and bank-based.

3.3.1 Page-Based Interleaving

Page-based interleaving yields the best performance and is the preferred interleaving method. Page-based interleaving supports consecutive back-to-back accesses. It uses low address bits as the bank select for the SDRAM, thus allowing interleaving on every page boundary. Paged-based interleaving is activated by setting PSDMR[PBI]. This section covers two topics:

- Partitioning the system bus address bus based on the port size settings of 32 bits or 64 bits (see **Table 7** and **Table 8**).
- Partitioning the SDRAM device address port from the SDRAM device executing a bank ACTIVATE command and read/write commands using 32- and 64-bit port size settings (see **Table 9** through **Table 12**).

Table 7. System Bus Address Bus Partition for a 64-Bit Port Size

A[0–7]	A[8–18]	A[19–20]	A[21–28]	A[29–31]
MSB of start address	Row	Bank Select	Column	LSB

Table 8. System Bus Address Bus Partition for a 32-Bit Port Size

A[0–8]	A[9–19]	A[20–21]	A[22–29]	A[30–31]
MSB of start address	Row	Bank Select	Column	LSB

When the system bus address bus is partitioned for page-based interleaving, the LSB vary between a 32-bit and a 64-bit port size because address lines 31–29 are ignored for the 64-bit port size and address lines 31–30 are ignored for a 32-bit port size. The 8-bit and 16-bit port sizes are not covered because the minimum access for the MSC8101ADS SDRAM is 32 bits. That is, there are 32 data lines for each SDRAM device, so each device has a

32-bit port size. Since there are two devices, the total number of data lines is 64, for a 64-bit port size. Therefore, this application note focuses on the 32-bit and 64-bit port sizes. These configurations are based on the MSC8101ADS and are subject to change if an SDRAM with a different size and bank architecture is used.

The column address lines are A[21–28] for a 64-bit port size and A[22–29] for a 32-bit port size. The SDRAM on the MSC8101ADS board contains 11 row address lines and 8 column address lines. The row address lines are A[8–18] for a 64-bit port size and A[9-19] for a 32-bit port size. There are two bits for bank select lines because the SDRAM adapted on the MSC8101ADS has 4 banks.

Table 9. SDRAM Device Address Port During ACTIVATE Command for a 64-Bit Port Size

Driven Signals	A[0–15]	A[16–17]	A[18–28]	A[29–31]
System bus Bus partition	—	A[19–20] (Internal bank select)	A[8–18] (Row address)	—

Note: Driven signals are signals driven on external pins when address multiplexing is enabled.

Table 10. SDRAM device Address Port During ACTIVATE Command for 32-Bit Port size

Driven Signals	A[0–16]	A[17–18]	A[19–29]	A[30–31]
System Bus partition	—	A[20–21] (Internal bank select)	A[9–19] (Row Address)	—

During the ACTIVATE command period, the MSC8101 sends the row address lines to the SDRAM to activate the specified bank. The MSC8101 device must choose a bank before attempting to read or write from the activated bank.

Table 11. SDRAM Device Address Port During READ/WRITE Command for 64-Bit Port Size

Driven Signals	A[16–17]	A[18]	A[19]	A[20]	A[21–28]	A[29–31]
System bus Bus partition	Internal bank select	Don't care	Don't care	Don't care	Column	—

Table 12. SDRAM Device Address Port During READ/WRITE Command for 32-Bit Port Size

Driven Signals	A[17–18]	A[19]	A[20]	A[21]	A[22–29]	A[30–31]
System bus Bus partition	Internal bank select	Don't care	Don't care	Don't care	Column	—

The READ/WRITE command follows the ACTIVATE command. After the MSC8101 device sends the row address lines to activate the bank, the MSC8101 must either read or write to that specific bank. At this point, the MSC8101 sends the column address lines to the SDRAM to specify the starting column in the SDRAM for read or write operations. A $\overline{\text{CAS}}$ latency occurs during reads from the SDRAM; there is no latency during writes to the SDRAM. It is important to specify auto precharge, which precharges all SDRAM banks, or single precharge, which precharges only the selected bank during execution of the ACTIVATE command.

Table 13 shows the SDAM[5–7] bits in the PSDMR for 32-bit and 64-bit port sizes in page mode interleaving. The cells highlighted in italics apply to the 32-bit port size, and the cells highlighted in bold (red) apply to the 64-bit port size. Note the overlap.

Table 13. SDRAM Address Multiplexing for 64- and 32-Bit Port Sizes

SDAM	External System Bus Address Pins	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31
000	Signal driven on external pins when address multiplexing is enabled	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23
001		A7	*A8*	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22
010		A6	A7	*A8*	**A9**	**A10**	**A11**	**A12**	**A13**	**A14**	**A15**	**A16**	**A17**	**A18**	**A19**	A20	A21
011		A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20
100		A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19
101		—	—	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18

Following are the PSDMR settings for SDRAM page mode interleaving, as listed in **Table 22**:

- SDAM[5–7]. The A[8–18] signals are driven on the external pins when address multiplexing is enabled. For the 64-bit port size, these signals match the A[18–28] external system bus address pins. For the 32-bit port size, the A[9–19] signals are driven on the external pins when address multiplexing is enabled. These signals match the A[19–29] external system bus address pins. Thus, SDAM is set to 010. Therefore, bits 5–7 in the PSDMR are the same for both 32-bit and 64-bit port sizes.
- BSMA[8–10]. Since the row address lines start at A8 for 64-bit port size and at A9 for 32-bit port size, the range of bank select lines ends at A17 for the 64-bit port size and A18 for the 32-bit port size Thus, the PSDMR[BSMA] bits [8–10] are set to 011 for the 64-bit port size and to 100 for the 32-bit port size, respectively. This configuration applies only when the MT48LC2M32B2 is used on the MSC8101ADS. These configurations vary depending on SDRAM bank architecture (that is, 2 or 4 banks), and the number of row and column addresses.
- SDA10 [11–13]. The starting row address for the 64-bit port size is A8, and the starting row address for the 32-bit port size is A9. Thus, SDA10 [11–13] is set to 010 for the 64-bit port size and to 001 for the 32-bit port size.

Figure 9 summarizes the address multiplexing for a 32-bit port size.

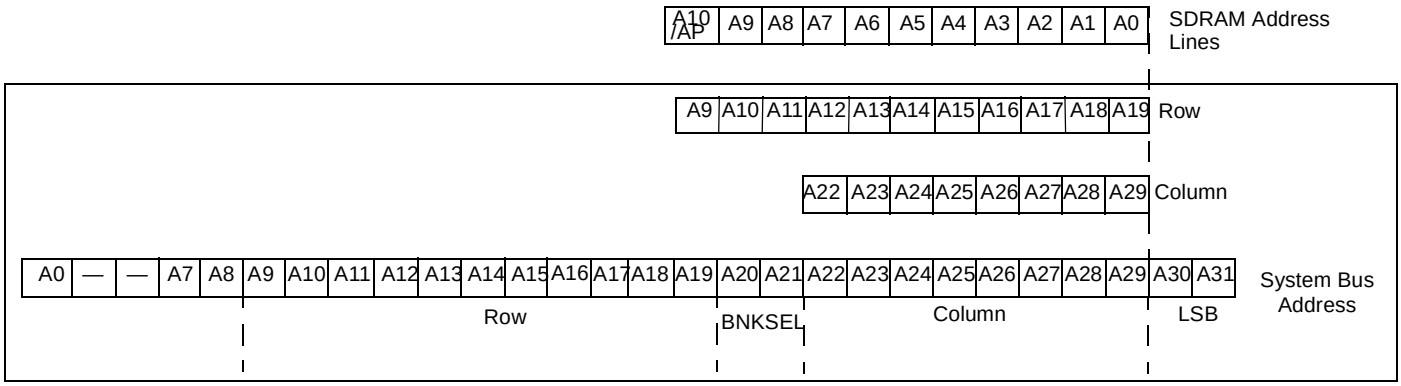

Figure 9. MSC8101 SDRAM Address Multiplexing.

Note: Partitioning is affected if a different SDRAM is used. Usually the number of row and column address lines varies according to the size of the SDRAM. As long as the SDRAM device address

port and the system bus address bus is partitioned according to the correct number of row and columns address lines, BR, OR, and PSDMR are programmed correctly.

3.3.2 Bank-Based Interleaving

Bank-based interleaving uses the most significant address bits as the bank select for the SDRAM, thus allowing interleaving only on bank boundaries. It is activated by clearing PSDMR[PBI]. See **Table 14** through **Table 19**.

Table 14. System Bus Address Bus Partition for 64-Bit Port Size

A[0–7]	A[8–9]	A[10–20]	A[21–28]	A[29–31]
MSB of start address	Internal bank address	Row	Column	LSB

Table 15. System Bus Address Bus Partition for 32-Bit Port Size

A[0–8]	A[9–10]	A[11–21]	A[22–29]	A[30–31]
MSB of start address	Internal bank address	Row	Column	LSB

Table 16. SDRAM Address Port During ACTIVATE for 64-Bit Port Size

Driven Signals	A[0–15]	A[16–17]	A[18–28]	A[29–31]
System bus partition	—	A[8-9] (Internal bank select)	A[10-20] (Row address)	—

Table 17. SDRAM Address Port During ACTIVATE for 32-Bit Port Size

Driven Signals	A[0–16]	A[17–18]	A[19–29]	A[30–31]
System bus partition		A[9-10] (Internal bank select)	A[11-21] (Row address)	

Table 18. SDRAM Device Address Port During READ/WRITE for 64-Bit Port Size

Driven Signals	A[16–17]	A18	A19	A20	A[21–28]	A[29–31]
System bus partition	Internal bank select	Don't care	Don't care	Don't care	Column	—

Table 19. SDRAM Device Address Port During READ/WRITE for 32-Bit Port Size

Driven Signals	A[17–18]	A19	A20	A21	A[22–29]	A[30–31]
System bus partition	Internal bank select	Don't care	Don't care	Don't care	Column	—

3.4 Memory Controller Bank Registers

This section shows the MSC8101 registers and bit settings necessary to program the SDRAM machine properly for page-based interleaving both the 32-bit and 64-bit port sizes. The MSC8101 is connected to the MT48LC2M32B2 SDRAM device. The interface timings, bursts, and interleaving are easily programmed in the SDRAM machine registers. The MSC8101 registers to be programmed are as follows:

- Base Registers (BRx)
- Option Registers (ORx)
- 60x SDRAM Mode Register (PSDMR)
- 60x Bus-Assigned SDRAM Refresh Timer (PSRT)
- Memory Refresh Timer Prescaler Register (MPTPR)

All possible bit settings are shown for each register, and, for each bit, the selected setting for this application is highlighted in bold.

BRx Base Registers **(BR2) 0x10110**

	Bit 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	BA															
TYPE	R/W															
RESET	Depends on reset configuration sequence.															

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	BA	—		PS		DECC		WP	MSEL			EMEMC	ATOM		DR	V
TYPE	R/W.															
RESET	Depends on reset configuration sequence.															

NOTES: 1. After a system reset, the V bit is set in BR0 and reset in BR[1-11].

NC

The base registers contain the base address and address type that the memory controller uses to compare the address bus value with the current address accessed.

Table 20. BR*x* Bit Settings

Name	Reset	Description	Settings
BA 0–16	1	**Base Address** The upper 17 bits of each base address register are compared to the address on the address bus to determine if the bus master is accessing a memory bank controlled by the memory controller. BRx[BA] is used with ORx[AM].	
— 17–18	0	Reserved. Write to zero for future compatibility.	
PS 19–20	0	**Port Size** Specifies the port size of this memory region.	**00 64-bit.** **11 32-bit.** **10 16-bit.** **01 8-bit.**

Table 20. BR*x* Bit Settings

Name	Reset	Description	Settings
DECC 21–22	0	**Data Error Correction and Checking** Specifies the method for data error checking and correction.	**00** Data errors checking disabled. **01** Normal parity checking. **10** Read-modify-write parity checking. **11** ECC correction and checking.
WP 23	0	**Write Protect** Can restrict write accesses within the address range of a BR. An attempt to write to this address range while WP = 1 can cause TEA to be asserted by the bus monitor logic (if enabled) which terminates the cycle. When WP is set, the memory controller does not assert CSx and PSDVAL on write cycles to this memory bank. TESCR1[WP] or L_TESCR1[WP] is set if a write to this memory bank is attempted	**0** Read and write accesses are allowed. **1** Only read access is allowed.
MSEL 24–26	0	**Machine Select** Specifies machine select for the memory operations handling and assigns the bank to the system bus if GPCM or SDRAM are selected. If UPM*x* is selected, the bus assignment is determined by M*x*MR[BSEL].	**000** GPCM— system bus (reset value). **001** GPCM— local bus. **010** SDRAM— system bus. **011** Reserved. **100** UPMA. **101** UPMB. **110** UPMC. **111** Reserved.
EMEMC 27	0	**External MEMC Enable** Overrides MSEL and assigns the bank to the system bus. However, other BRx fields remain in effect. When this bit is set, the external memory controller is expected to assert AACK, TA, and PSDVAL.	**0** Accesses are handled by the memory controller according to MSEL. **1** Accesses are handled by an external memory controller (or other slave) on the system bus.
ATOM 28–29	0	**Atomic Operation** Note that If the device fails to release the bus, the lock is released after 256 clock cycles. Writes to the address space handled by the memory controller bank cause the MSC8101 to lock the bus for the exclusive use of the master. The lock is released when the master performs a read operation from this address space. This feature is intended for CAM operations. Reads from the address space handled by the memory controller bank cause the MSC8101 to lock the bus for the exclusive use of the accessing device. The lock is released when the device performs a write operation to this address space.	**00** The address space controlled by the memory controller bank is not used for atomic operations. **01** Read-after-write-atomic (RAWA). **10** Write-after-read-atomic (WARA). **11** Reserved.
DR 30	0	**Data Pipelining** This feature is for memory regions that use ECC or parity checks and need to improve data set-up time.	**0** No data pipelining. **1** Data beats of accesses to the address space controlled by the memory controller bank are delayed by one cycle.
V 31	0[2]	**Valid Bit** Indicates that the contents of the BR*x* and OR*x* pair are valid. The CS signal does not assert until V is set. An access to a region with no V bit set may cause a bus monitor time-out. After a system reset, BR0[V] is set.	**0** This bank is invalid. **1** This bank is valid.

NOTES: 1. Depends on reset configuration sequence.

2. After a system reset, the V bit is set in BR0 and reset in BR[1–11].

ORx Option Registers—SDRAM Mode **(OR2) 0x10114**

	Bit 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	SDAM												LSDAM			
TYPE	R/W															
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	16	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
	LSDAM	BPD		ROWST				NUMR			PMSEL	IBID	—			
TYPE	R/W															
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OR defines the size of memory banks and address attributes. All possible bit settings are shown, and, for each bit, the selected setting for this application is highlighted in bold.

Table 21. OR*x* Bit Settings (SDRAM Mode)

Name	Reset	Description	Settings
SDAM 0–11	0	**SDRAM Address Mask** Masks corresponding BR*x* bits. Masking address bits independently allows SDRAM devices of different size address ranges to be used. Clearing bits masks the corresponding address bit. Setting bits causes the corresponding address bit to be compared with the address pins. Address mask bits can be set or cleared in any order, allowing a resource to reside in more than one area of the address map. SDAM can be read or written at any time. NOTE: If PSDMR[PBI]=0, the maximum size of the memory bank should not exceed 128 MB.	**0000_0000_00004 GB** **1000_0000_00002 GB** **1100_0000_0000 1 GB** **1110_0000_0000512 MB** **1111_0000_0000256 MB** **1111_1000_0000 128 MB** **1111_1100_000064 MB** **1111_1110_000032 MB** **1111_1111_000016 MB (for 64-bit port size)** **1111_1111_1000 8 MB (for 32-bit port size)** **1111_1111_1000 8 MB** **1111_1111_1100 4 MB** **1111_1111_1110 2 MB** **1111_1111_1111 1 MB**
LSDAM 12–16	0	**Lower SDRAM Address Mask** Reset LSDAM to 0x0 to implement a minimum size of 1 MB when SDRAM is used.	
SDRAM Page Information			
BPD 17–18	0	**Banks Per Device** Sets the number of internal banks per SDRAM device. Note that for 128-MB SDRAMs, BPD must have a value of 00 or 01.	**00** **2 internal banks per device.** **01** **4 internal banks per device (settings are common for both 32-bit and 64-bit port sizes).** **10** **8 internal banks per device (not valid for 128-MB SDRAMs).** **11** **Reserved.**

Table 21. OR*x* Bit Settings (SDRAM Mode)

Name	Reset	Description	Settings
ROWST 19–22	0	**Row Start Address Bit** Sets the demultiplexed row start address bit. The value of ROWST depends on PSDMR[PBI].	**For PSDMR[PBI] = 0**: **0010 A7.** **0100 A8.** **0110 A9.** **1000 A10.** **1010 A11.** **1100 A12.** **1110 A13.** Other values are reserved. **For PSDMR[PBI] = 1**: **0000 A0.** **0001 A1.** **0010 A2.** **...** **1000 A8 (for 64-bit port size).** **1001 A9 (for 32-bit port size).** **1101–1111 Reserved.**
NUMR 23–25	0	**Number of Row Address Lines** Sets the number of row address lines in the SDRAM device.	**000 9 row address lines.** **001 10 row address lines.** **010 11 row address lines (settings are common for both 32-bit and 64-bit port sizes).** **011 12 row address lines.** **100 13 row address lines.** **101 14 row address lines.** **110 15 row address lines.** **111 16 row address lines.**
PMSEL 26	0	**Page Mode Select** Selects page mode for the SDRAM connected to the memory controller bank.	**0 Back-to-back page mode (normal operation). Page is closed when the bus becomes idle.** **1 Page is kept open until a page miss or refresh occurs.**
IBID 27	0	**Internal Bank Interleaving Within Same Device Disable** Setting this bit disables bank interleaving between internal banks of a SDRAM device connected to the chip-select line. IBID should be set in multi-master bus mode if the SDRAM device is not connected to the BNKSEL pins.	**0 Enables bank interleaving (setting is common for both 32-bit and 64-bit port sizes).** **1 Disables bank interleaving.**
— 28–31	0	Reserved. Write to zero for future compatibility.	

PSDMR 60x SDRAM Mode Register **0x10190**

	Bit 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	PBI	RFEN	OP			SDAM			BSMA			SDA10			RFRC	
TYPE	R/W															
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	RFRC	PRETOACT			ACTTORW			BL	LDOTOPRE		WRC		EAMUX	BUFCMD	CL	
TYPE	R/W															
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PSDMR configures operations pertaining to the SDRAM machine on the system bus. All possible bit settings are shown, and, for each bit, the selected setting for this application is highlighted in bold.

Table 22. PSDMR Settings

Name	Reset	Description	Settings
PBI 0	0	**Page-Based Interleaving** Selects the address multiplexing method. PBI works in conjunction with PSDMR[SDA10].	**0** **Bank-based interleaving.** **1** **Page-based interleaving (normal operation).**
RFEN 1	0	**Refresh Enable** Indicates that the SDRAM needs refresh services.	**0** **Refresh services are not required.** **1** **Refresh services are required.**
OP 2–4	0	**SDRAM Operation** Determines which operation occurs when the SDRAM device is accessed. If Multi-Master Bus mode is in effect on the system bus or the SDRAM port size is 8-/16-bit or the SDRAM is connected to the BADDR lines (not needed for 64-/32-bit port size), the bus master must supply the mode register data on the low bits of the address during the access. NOTE: The selection of OP depends on the operation during SDRAM initialization.	**000** **Normal operation.** **001** **CBR refresh, used in SDRAM initialization.** **010** **Self refresh (for debug purpose).** **011** **Mode Register write, used in SDRAM initialization.** **100** **Precharge bank (for debug purpose).** **101** **Precharge all banks, used in SDRAM initialization.** **110** **Activate bank (for debug purpose).** **111** **Read/write (for debug purpose).**

Table 22. PSDMR Settings (Continued)

<table>
<tr><th>Name</th><th>Reset</th><th>Description</th><th>Settings</th></tr>
<tr><td>SDAM
5–7</td><td>0</td><td>Address Multiplex Size
Determines how the address of the current memory cycle can be output on the address pins.</td><td>
<table>
<tr><th>SDAM</th><th>External System Bus Address Pin</th><th>Signal Driven on External Pin</th></tr>
<tr><td>000</td><td>A[13–31]</td><td>A[5–23]</td></tr>
<tr><td>001</td><td>A[14–31]</td><td>A[5–22]</td></tr>
<tr><td>010</td><td>A[15–31]</td><td>A[5–21]</td></tr>
<tr><td>011</td><td>A[16–31]</td><td>A[5–20]</td></tr>
<tr><td>100</td><td>A[17–31]</td><td>A[5–19]</td></tr>
<tr><td>101</td><td>A[18–31]</td><td>A[5–18]</td></tr>
</table>
NOTE: The selection shown in bold (the 010 value) applies to both 32-bit and 64-bit
</td></tr>
<tr><td>BSMA
8–10</td><td>0</td><td>Bank Select Multiplexed Address Line
Selects the address pins to serve as bank-select address for the system bus SDRAM. The bank select address can also be output on the BANKSEL pins (optional).</td><td>000 A[12–14].
001 A[13–15].
010 A[14–16].
011 A[15–17] (for 64-bit port size).
100 A[16–18] (for 32-bit port size).
101 A[17–19].
110 A[18–20].
111 A[19–21].</td></tr>
<tr><td>SDA10
11–13</td><td>0</td><td>“A10” Control
With PSDMR[PBI], determines which address line can be output to SDA10 during an ACTIVATE command, when SDRAM is selected, to control the memory access.</td><td>For PBI = 0:
000 A12.
001 A11.
010 A10.
011 A9
100 A8
101 A7.
110 A6.
111 A5.
For PBI = 1:
000 A10.
001 A9 (for 32-bit port size).
010 A8 (for 64-bit port size).
011 A7.
100 A6.
101 A5.
110 A4.
111 A3.</td></tr>
</table>

Table 22. PSDMR Settings (Continued)

Name	Reset	Description	Settings
SDRAM Device-Specific Parameters:			
RFRC 14–16	0	**Refresh Recovery** Defines the earliest timing for an activate command after a REFRESH command. Sets the refresh recovery interval in clock cycles.	**000 Reserved.** **001 3 clock cycles.** **010 4 clock cycles.** **011 5 clock cycles.** **100 6 clock cycles.** **101 7 clock cycles.** **110 8 clock cycles.** **111 16 clock cycles.**
PRETOACT 17–19	0	**Precharge to Activate Interval** Defines the earliest timing for an ACTIVATE or REFRESH command after a PRECHARGE command.	**001 1 clock-cycle wait states.** **010 2 clock-cycle wait states.** **...** **111 7 clock-cycle wait states.** **000 8 clock-cycle wait states.**
ACTTORW 20–22	0	**Activate to Read/Write Interval** Defines the earliest timing for a READ/WRITE command after an ACTIVATE command.	**001 1 clock cycle.** **010 2 clock cycles.** **...** **111 7 clock cycles.** **000 8 clock cycles.**
BL 23	0	**Burst Length** Defines the SDRAM burst length.	**0 SDRAM burst length is 4. Use this value if the device port size is 64 or 16.** **1 SDRAM burst length is 8. Use this value if the device port size is 32 or 8.**
LDOTOPRE 24–25	0	**Last Data Out to Precharge** Defines the earliest timing for PRECHARGE command after the last data was read from the SDRAM.	**00 0 clock cycles.** **01 –1 clock cycle.** **10 –2 clock cycles.** **11 Reserved.**
WRC 26–27	0	**Write Recovery Time** Defines the earliest timing for PRECHARGE command after the last data was written to the SDRAM.	**01 1 clock cycle.** **10 2 clock cycles.** **11 3 clock cycles.** **00 4 clock cycles.**
EAMUX 28	0	**External Address Multiplexing Enable/Disable** If this bit is set, PSDMR[ACTTORW] **should** be a minimum of two clock cycles. In multi-master bus mode, external address multiplexing is placed on the address lines. If the additional delay of the multiplexing endangers the device setup time, EAMUX should be set. Setting this bit causes the memory controller to add another cycle for each address phase. Note that EAMUX can also be set in any case of delays on the address lines, such as address buffers.	**0 No external address multiplexing. Fastest timing.** **1 The memory controller asserts SDAMUX for an extra cycle before issuing an ACTIVATE command to the SDRAM. This is useful when external address multiplexing can cause a delay on the address lines.**

Table 22. PSDMR Settings (Continued)

Name	Reset	Description	Settings
BUFCMD 29	0	**Command Buffer** If external buffers are placed on the control lines going to both the SDRAM and address lines, setting the BUFCMD bit causes all SDRAM control lines except $\overline{CS}$ to be asserted for two cycles, instead of one. In multi-master bus mode, external buffers can be placed on the command strobes, except $\overline{CS}$, as well as on the address lines. If the additional delay of the buffers endangers the device setup time, BUFCMD should be set, which causes the memory controller to add a cycle for each SDRAM command.	**0** **Normal timing for the control lines.** **1** **All control lines except $\overline{CS}$ are asserted for two cycles.**
CL 30–31	0	**CAS Latency** Defines the timing for first read data after SDRAM samples a column address.	**00** **Reserved** **01** **1.** **10** **2.** **11** **3.**

PSRT 60x Bus-Assigned SDRAM Refresh Timer **0x1019C**

	Bit 0	1	2	3	4	5	6	7
	PSRT							
TYPE	R/W							
RESET	0	0	0	0	0	0	0	0

PSRT determines the timer period for SDRAM refresh requests.

Table 23. PSRT Bit Descriptions

Name	Reset	Description
PSRT 0–7	0	**Refresh Timer Period** Determines the timer period according to the following equation: $TimerPeriod = (PSRT + 1) \times \frac{MPTPR[PTP] + 1}{\text{Bus frequency}}$ This timer generates refresh requests for all valid banks that selected a SDRAM machine assigned to the system bus and is refresh-enabled (PSDMR[RFEN] = 1). Each time the timer expires, all banks that qualify generate a bank staggering auto refresh request using the SDRAM machine. Example: For a 25 MHz system bus clock and a required service rate of 15.6 µs, given MPTPR[PTP] = 32, the PSRT value should be 12 decimal. 12/(25 MHz/32) = 15.36 µs, which is less than the required service period of 15.6 µs.

MPTPR Memory Refresh Timer Prescaler Register **0x10184**

	Bit 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	PTP								—							
TYPE	R/W															
RESET	0	0	0	0	0	0	1	*x*	0	0	0	0	0	0	0	0

MPTPR determines the period of the memory refresh timer input clock. It divides the bus clock

Table 24. MPTPR Bit Settings

Name	Reset	Description
PTP 0–5	0	**Memory Timers Prescaler** Determines the period of the memory refresh timers input clock. It divides the bus clock.
PTP 6	1	
PTP 7	*x*	
— 8–15	0	Reserved. Write to zero for future compatibility.
Where *x* can be a zero or one—that is, 0000_0010 or 0000_0011.		

3.5 SDRAM Machine Initialization on the MSC8101ADS

The following code can be compiled using CodeWarrior™.

Table 25. Program SDRAM For the 64-Bit Port Size

Command	Explanation
writemmr8 PSRT 0xe	1. Program PSRT.
writemmr32 OR2 0xff003080	2. Program OR2 for 16 MB. • The bank size is 16 MB • There are 11 row address lines, and the first row address line starts at A8, • 4 banks per device • Bank interleaving is enabled
writemmr32 BR2 0x20000041	3. Program BR2 for 64-bit port size. • Base address 0x20000000 • Data pipelining is not enabled • No error correction • SDRAM Machine is the memory controller of choice • Bank is valid

Table 25. Program SDRAM For the 64-Bit Port Size (Continued)

Command	Explanation
writemmr32 PSDMR 0xc2689212	4. Program PSDMR for normal operation. • SDRAM address multiplex size (SDAM) = 010 • Bank select Multiplexed Address line (BSMA) = 011 • SDRAM A10 control (SDA10) is A8 • Refresh recovery (RFRC) is 3 clock cycles • Precharge to Activate interval (PRETOACT) = 1 clock cycle • Activate to read/write interval (ACTTORW) = 1 clock cycle • Burst length is 4 data beats • Last data out to Precharge (LDOTOPRE) = 0 cycles • Write recovery time is 2 cycles • External Address Multiplexing Enable/Disable (EAMUX) = 0 • Command buffer (BUFCM) is normal (1 clock cycle for all memory control signals • $\overline{\text{CAS}}$ latency (CL) = 2
writemem32 0x20000020 0x0	5. Write to a random location in memory.
writemmr32 PSDMR 0xaa689212	6. Program the PSDMR register to PRECHARGE all banks.
writemem32 0x20000020 0x0	
writemmr32 PSDMR 0x8a689212	7. Program the PSDMR register to issue 8 auto refreshes. 8. Write 0x0 to a random location in memory eight times.
writemem32 0x20000000 0x0	
writemem32 0x20000000 0x0	
writemem32 0x20000000 0x0	
writemem32 0x20000000 0x0	
writemem32 0x20000000 0x0	
writemem32 0x20000000 0x0	
writemem32 0x20000000 0x0	
writemem32 0x20000000 0x0	
writemmr32 PSDMR 0x9A689212	9. Program PSDRAM to program the mode register. 0x20000032 indicates a $\overline{\text{CAS}}$ latency of 3-beat and 4-beat bursts.
writemem32 0x20000032 0x0	
writemmr32 OR2 0xFF0030A0	10. Program the BR2, OR2, and PSDMR2 for normal operation. • Base address 0x20000000 • Data pipelining is not enabled • No error correction • SDRAM Machine is the memory controller of choice • Bank is valid
writemmr32 BR2 0x20000041	
writemmr32 PSDMR 0xc2689212	
writemmr8 PSRT 0x13	11. Program the PSRT.
writemmr16 MPTPR 0x2800	12. Program the MPTPR.

Table 26. Program SDRAM For the 32-Bit Port Size

Command	Explanation
writemmr8 PSRT 0xe	1. Program the PSRT.
writemmr32 OR2 0xff803280	2. Program OR2 for 8 MB. • Bank size = 16 MB • There are 11 row address lines and the first row address line starts at A8 • 4 banks per device • Bank interleaving is enabled
writemmr32 BR2 0x20001841	3. Program BR2 for the 32-bit port size.
writemmr32 PSDMR 0xc2849312	4. Program PSDMR for normal operation. • SDRAM address multiplex size (SDAM) = 010 • Bank select Multiplexed Address line (BSMA) = 100 • SDRAM A10 control (SDA10) = A9 • Refresh recovery (RFRC) = 3 clock cycles • Precharge to Activate interval (PRETOACT) = 1 clock cycle • Activate to read/write interval (ACTTORW) = 1 clock cycle • Burst length = 8 data beats • Last data out to Precharge (LDOTOPRE) = 0 cycles • Write recovery time = 2 cycles • External Address Multiplexing Enable/Disable (EAMUX) = 0 • Command buffer (BUFCM) is normal (1 clock cycle for all memory control signals • $\overline{\text{CAS}}$ latency (CL) = 2
writemem32 0x20000020 0x0	5. Write to a random location in memory.
writemmr32 PSDMR 0xaa849312	6. Same as above PSDMR but operation is PRECHARGE all banks.
writemem32 0x20000020 0x0	
writemmr32 PSDMR 0x8a849312	7. Same as above PSDMR but operation is issue 8 auto refreshes. 8. Write 0x0 to a random location in memory eight times.
writemem32 0x20000000 0x0	
writemem32 0x20000000 0x0	
writemem32 0x20000000 0x0	
writemem32 0x20000000 0x0	
writemem32 0x20000000 0x0	
writemem32 0x20000000 0x0	
writemem32 0x20000000 0x0	
writemem32 0x20000000 0x0	
writemmr32 PSDMR 0x9a849312	9. Program PSDMAR to program the SDRAM mode register. 0x2000008C indicates a $\overline{\text{CAS}}$ latency of 2-beat and 8-beat bursts.
writemem32 0x2000008C 0x0	

Table 26. Program SDRAM For the 32-Bit Port Size (Continued)

Command	Explanation
writemmr32 OR2 0xff0032a0	10. Program the BR2, OR2, and PSDMR2 for normal operation. • Base address 0x20000000 • Data pipelining is not enabled • No error correction • SDRAM Machine is the memory controller of choice • Bank is valid
writemmr32 BR2 0x20001841	
writemmr32 PSDMR 0xc2849312	
writemmr8 PSRT 0x13	11. Program PSRT.
writemmr16 MPTPR **0x2800**	12. Program MPTPR.

4 Related Reading

- *MSC8101 User's Guide* (MSC8101UG/D). See the chapter on "Connecting External Memories and Memory-Mapped devices."
- *MSC8101 Reference Manual* (MSC8101RM/D). See the chapter on the Memory Controller.
- *Micron MT48LC2M32B2TG SDRAM Data Sheet.* Visit www.micron.com.

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