

Using the MSC8101 Serial Interface

By Barbara Johnson

The MSC8101 CPM multiplexing logic (CMX) connects the universal test and operations PHY interface for ATM (UTOPIA) or the media-independent interface (MII) physical layers to the FCCs, SCCs, and SMCs. This connection is achieved in the non-multiplex serial interface (NMSI) or the time-division multiplex (TDM) mode. **Figure 1** shows the serial controller connections in the NMSI and TDM modes. In NMSI mode, the serial controllers are programmed independently to work with their respective individual signals, as follows:

- FCC1 and FCC2 can connect to their own MII set of signals. FCC1 can also connect to a UTOPIA level-2 interface.
- SCC1 and SCC2 can connect to their own set of modem control signals.
- SMC1 and SMC2 can connect to their own set of four signals.

In TDM mode, the CMX logic connects the serial controllers to the two serial interfaces (SI1 and SI2). These two SI blocks can be programmed to handle up to four TDM lines concurrently. The SI provides routing for the serial controllers to two time-slot assigners (TSAs). The TSAs can multiplex any combination of MCCs, FCCs, SCCs and SMCs to multiplex data on any of the four TDM lines. FCC3, SCC3, and SCC4 work only with the TSA, and no dedicated signals are available on the NMSI. The actual routing of data between the TDMs and the serial controllers is programmed in the SI RAM.

This application note focuses on connecting the serial controllers in TDM mode. It begins with a look at SI basics and then presents examples of SI RAM programming.

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1 Serial Interface Basics

Each MSC8101 serial interface block, SI1 or SI2, can connect to independent TDM buses. SI1 supports one TDM bus (TDMA1), and SI2 supports three TDM buses (TDMB2, TDMC2, and TDMD2). Each TDM can function as follows:

- T1 or E1 line
- Integrated services digital network (ISDN) primary rate
- ISDN basic rate interchip digital link (IDL)
- ISDN basic rate general circuit interface (GCI)
- E3 or DS3 (TDMA1 only)
- A user-defined interface

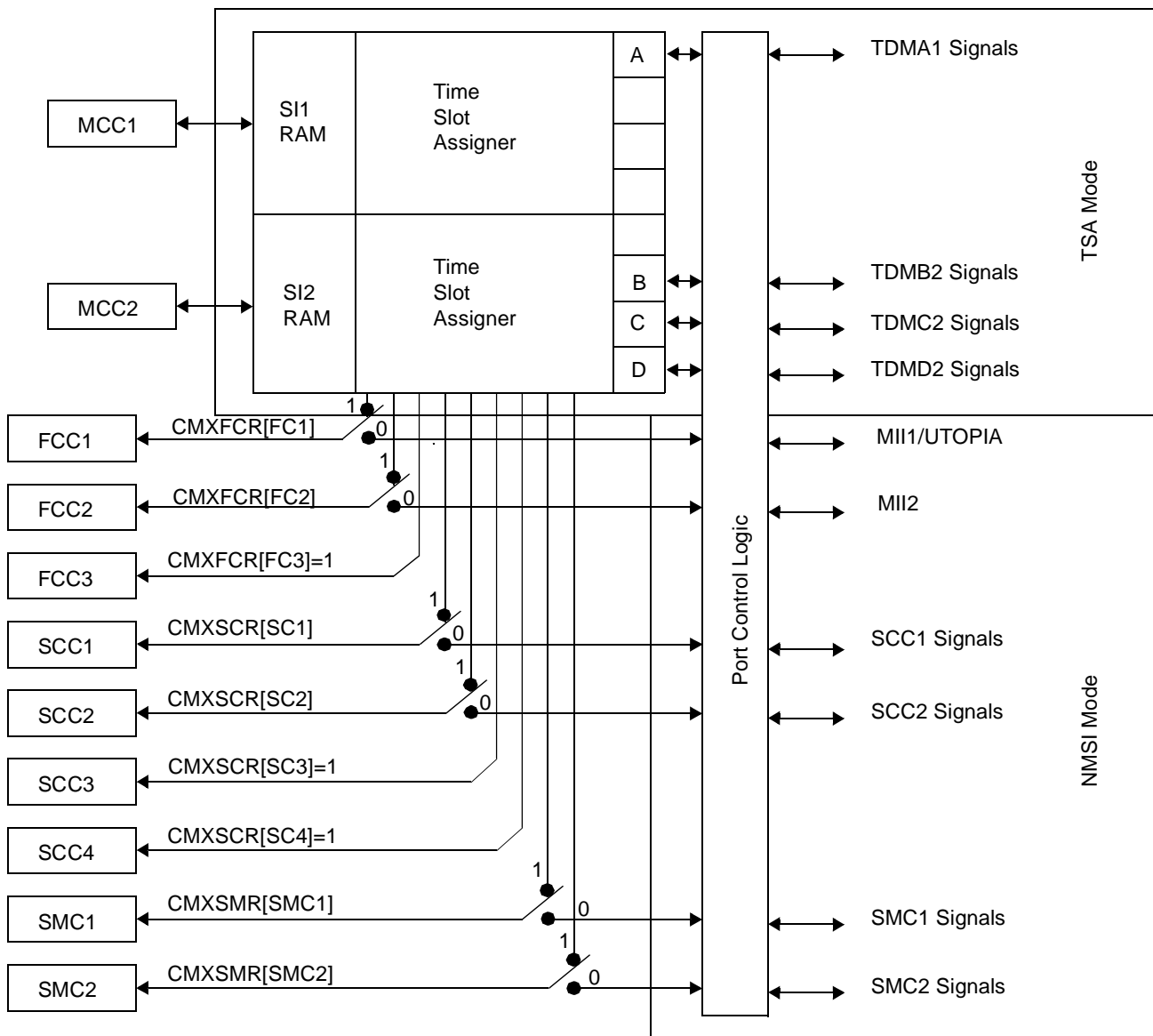


Figure 1. NMSI and TDM Connections

Features of the SI include:

- Independent and programmable transmit/receive routing, frame syncs, and clocks
- Selection of rising or falling edge for frame sync and data bits
- Support for 1x or 2x input clocks (one or two clocks per data bit)
- Selectable delay (0–3 bits) between frame sync and frame start
- Four programmable strobe output signals and four 2x clock output signals
- 1- or 8-bit resolution in routing, masking, and strobe selections
- Support for frames up to 16384 bits long
- Dynamic programming for routing and strobes
- Support for automatic echo and loopback for each TDM

Figure 2 shows a diagram of the TDM, which functions like an incremental switch. The SI RAM controls the matrix that specifies which serial controller connects to each node of the switch. When the frame sync is asserted, the switch increments at a rate relative to the clock input. The SI RAM defines the number of clock cycles at each switch position, as well as the levels on the four strobe signals. While the switch is set at a given position, the transmit SI RAM defines the data that is sent from the selected controller to the TDM transmit data signal. Similarly, the receive SI RAM defines the data that the serial controller receives from the TDM receive data signal. The TSA routes data appearing on a signal to a given controller and *vice versa*, for a defined period of time. It has no control over that data. Because TSA programming is independent of the protocol used, the target controller can be programmed for any synchronous protocol without affecting TSA programming. The target controller handles the data of the actual protocol.

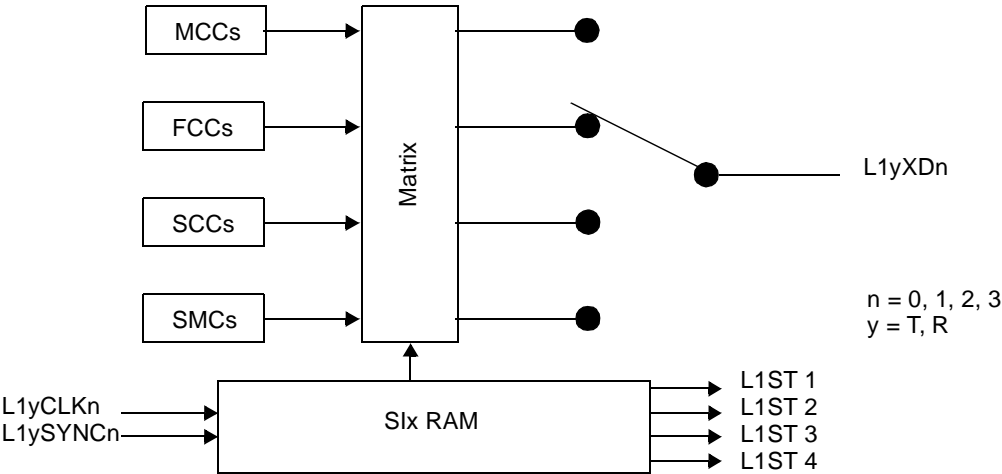


Figure 2. Theoretical TDM

Figure 3 shows an example of how data from serial controllers is multiplexed on a TDM. For this example, the transmit and receive share the same clock and frame sync, L1RCLKn and L1RSYNCn. The transmit and receive routing of data are independent. On the transmit side, four bits of SCC2 data are transmitted in the first timeslot while the L1ST1 strobe is asserted. Timeslot 2 is occupied by three bits from FCC1, and L1ST2 is asserted during this timeslot. The last two timeslots are occupied by SCC2 and SMC1, and L1ST1 is asserted again during the SCC2 timeslot. On the receive side, three bits of FCC2 data are received in the first timeslot while the L1ST3 strobe is asserted. Timeslot 2 is occupied by four bits from SCC1.

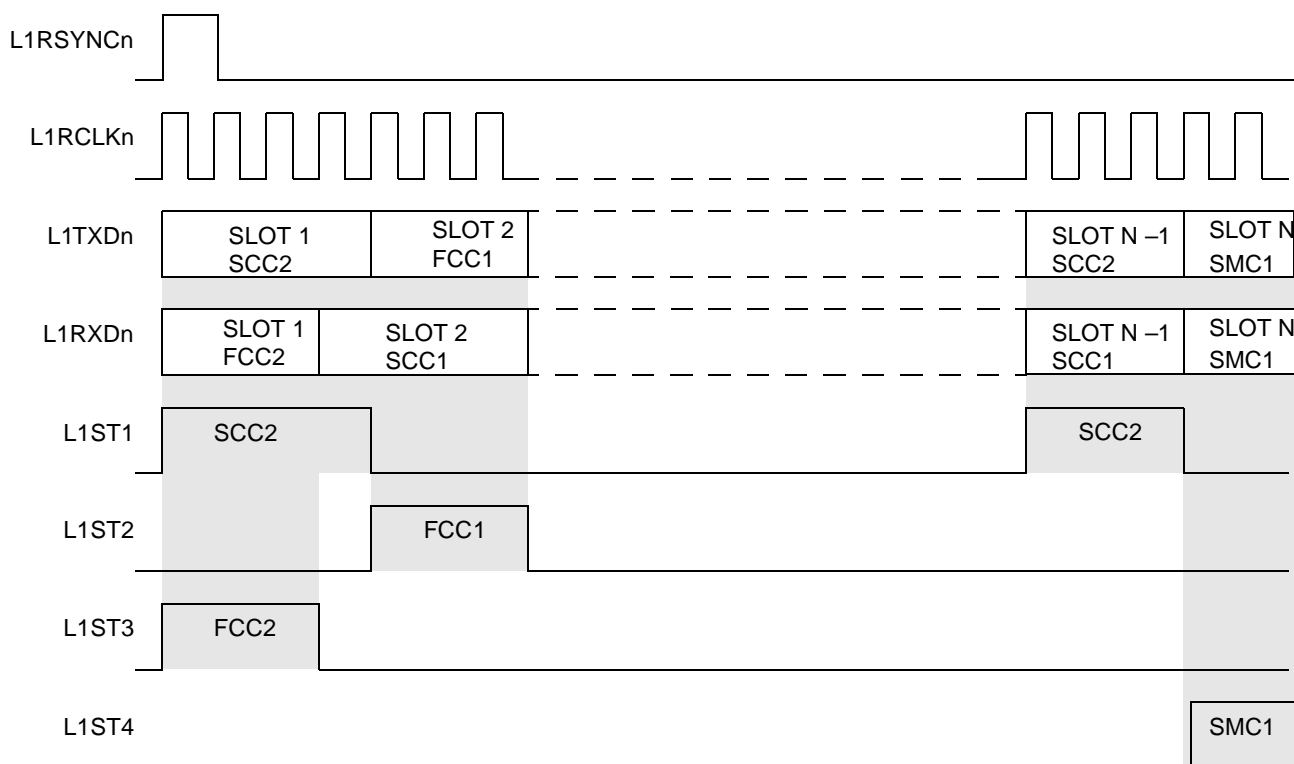


Figure 3. TDM Example

2 SI RAM Bank Assignment Examples

Each SIx RAM is divided into transmit and receive sections that can be independently programmed. Each transmit and receive section consists of 256 entries of 16 bits. Each section is divided into four banks of 64 entries each (see **Figure 4**). The SI1 and SI2 RAM are located in the internal memory space. The base address of the internal memory space is programmed in the Internal Memory Map Register (IMMR):

- The SI1 RAM transmit is located at an offset of 0x12000 from the IMM base address, and the SI1 RAM receive is located at an offset of 0x12400 from the IMM base address.
- The SI2 RAM transmit is located at an offset of 0x12800 from the IMM base address and the SI2 RAM receive is located at an offset of 0x12C00 from the IMM base address.

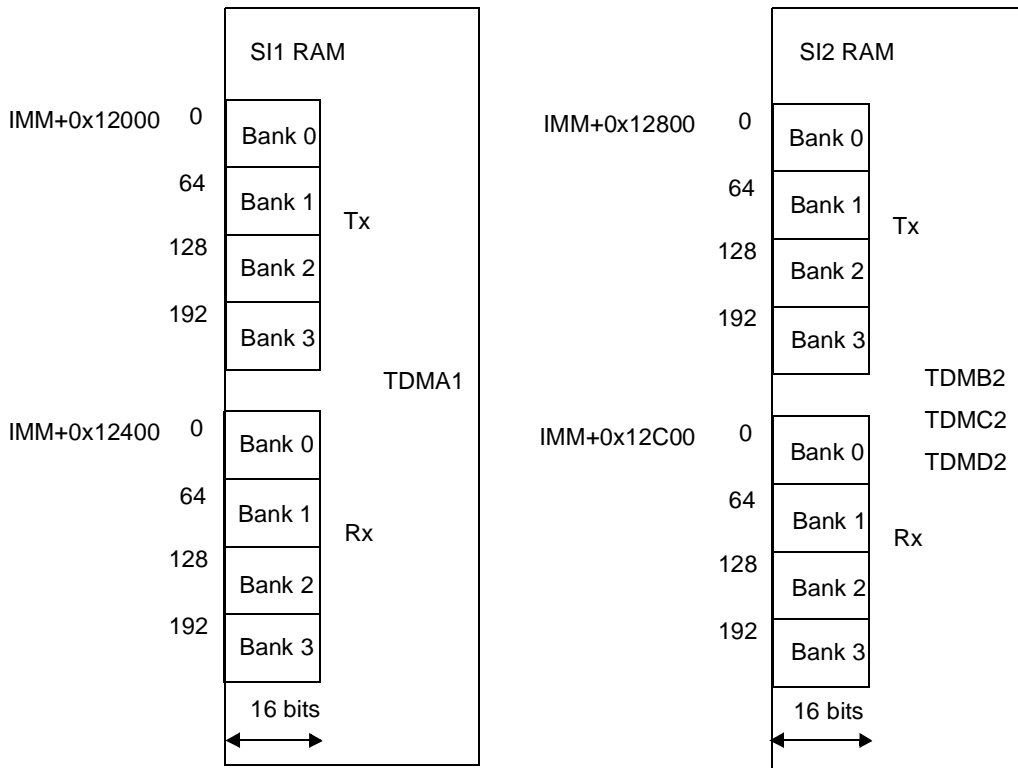


Figure 4. SI RAM Structure

The starting bank address (SAD_x) field in the SI Mode Registers SI1AMR, SI2BMR, SI2CMR, and SI2DMR is used to assign the SI RAM banks to a TDM (see **Figure 5**). Each 64-entry bank can be subdivided into two sections, the first 32 entries and the second 32 entries. Such a division is especially valuable for dynamic switching, in which one subsection is the current routing and the other subsection is the alternative routing. Dynamic switching is discussed in **Section 3**. The starting bank address of a TDM in the SI RAM must be a multiple of 32 entries. The rules for assigning SI RAM banks are as follows:

- The starting bank address of a TDM in the SI RAM must be a multiple of 32 entries. This requirement provides eight different starting addresses in the SI RAM.
- TDMs cannot share the same bank. A TDM can use multiple banks, but a bank can belong to only one TDM.
- The starting bank address of a TDM must be the same in the transmit and the receive SI RAM. You cannot independently allocate the SI RAM banks for the transmit and receive since the SI1xMR[SAD_x] and SI2xMR[SAD_x] fields apply to both the transmit and receive sections of SI RAM.

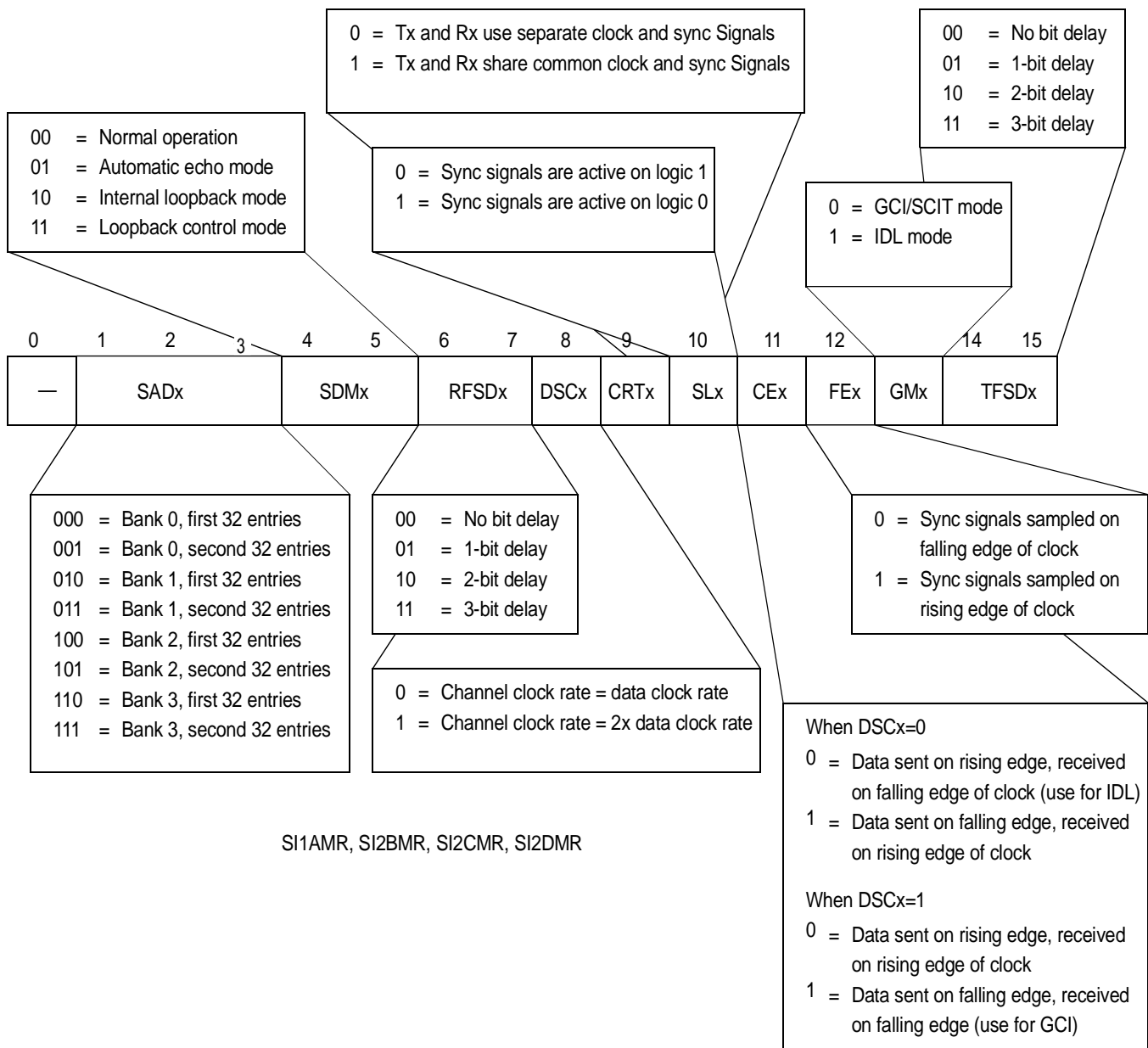


Figure 5. SI Mode Registers

Figure 6 shows a valid SI RAM bank assignment. Since only one TDM is used, all 256 entries can be used for that TDM.

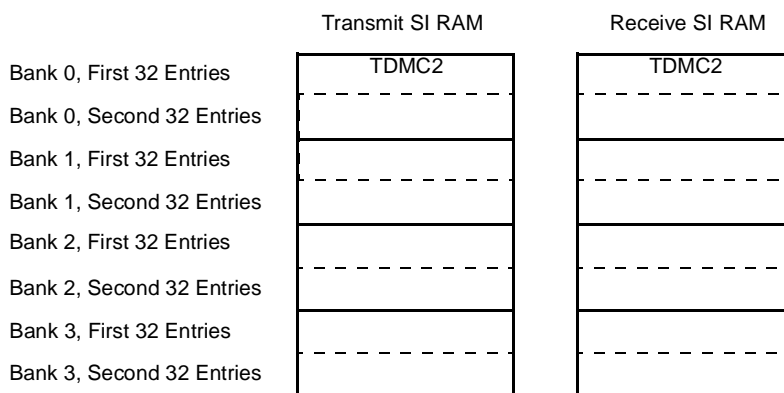


Figure 6. Valid SI RAM Bank Assignment With a Single TDM

Figure 7 shows a bank assignment that violates the rule that TDMs cannot share the same SI RAM bank. This example shows both TDMC2 and TDMD2 assigned to Bank 2 of the transmit and receive SI RAM. A bank can belong to only one TDM.

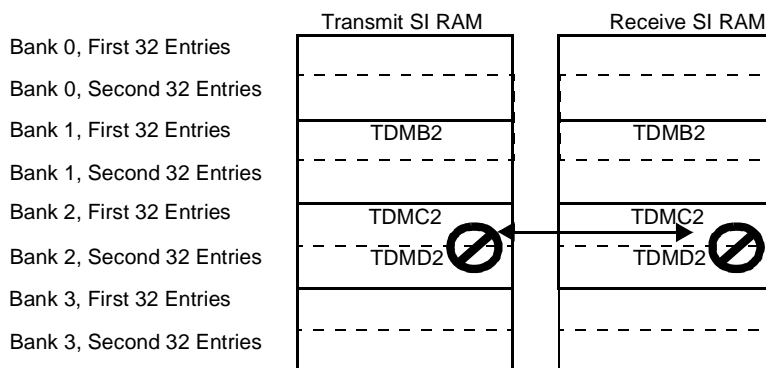


Figure 7. Invalid Bank Assignment With Multiple TDMs Sharing the Same Bank

In Figure 8, in the transmit SI RAM, Bank 1 is assigned to TDMB2, but in the receive SI RAM, Bank 1 is assigned to TDMC2. The other problem with this bank assignment is that the SI RAM allocation for TDMD2 uses different starting bank addresses for the transmit and receive sections. A TDM must have the same starting bank addresses in both the receive and transmit SI RAM.

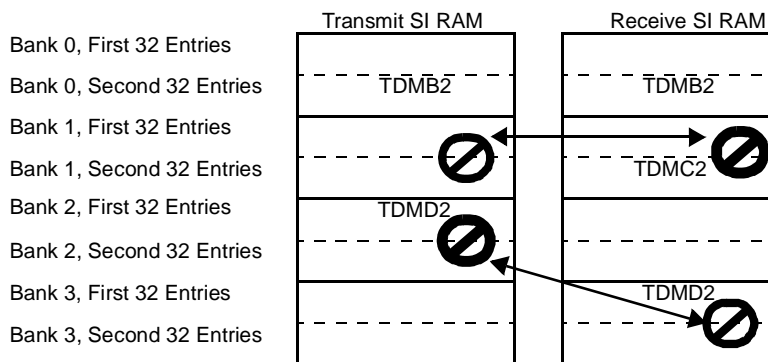


Figure 8. Invalid Bank Assignment, Different Starting Bank Addresses for Transmit/Receive

Figure 9 shows a valid SI RAM bank assignment. Each bank belongs to only one TDM and the starting bank address of each TDM is the same in the transmit and receive SI RAM.

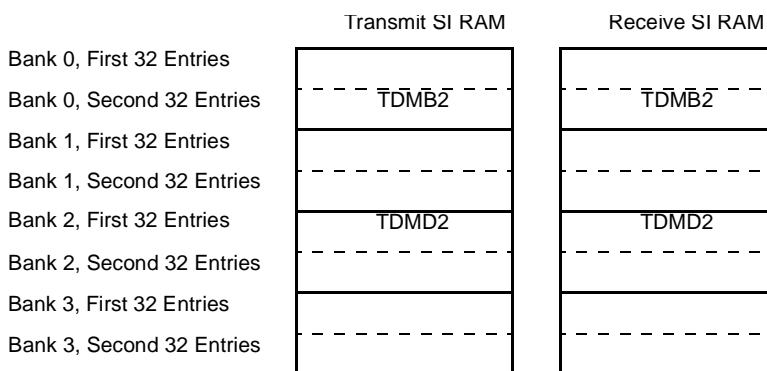


Figure 9. Valid Bank Assignment Using Multiple TDMs

3 Dynamic Frame Switching

Suppose there is a requirement that a frame differ from the previous one as shown in **Figure 10**. In this example, the current frame requires SCC2 data to be followed by FCC1 data. However, the next frame requires FCC2 data to be sent instead of FCC1 data. Because the frame routing is different, a change in the SI RAM routing definition is necessary.

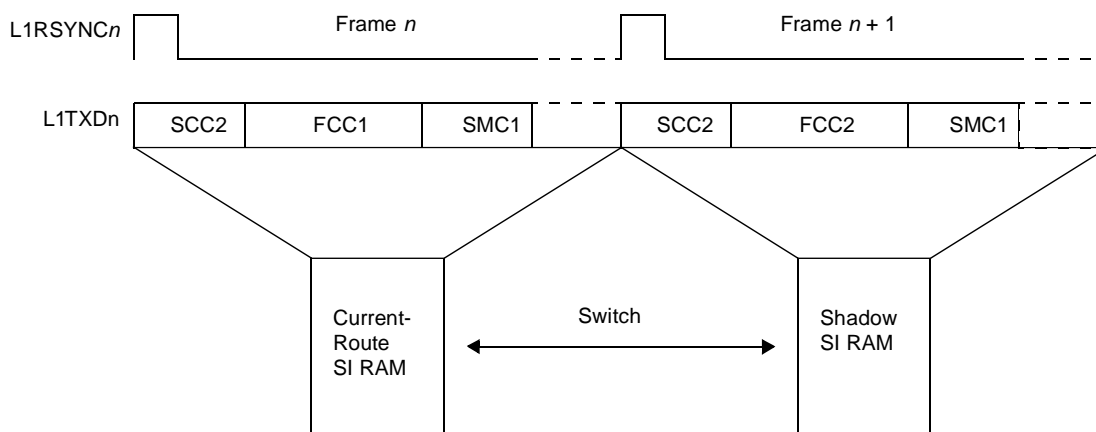


Figure 10. Dynamic Frame Switching

3.1 Shadow RAM Bank Assignment

Shadow SI RAM enables dynamic switching of frames. When dynamic frame switching is required, the SI RAM is divided into the current-route and shadow RAM. The shadow RAM contains the alternative SI RAM routing and is programmed in another portion of the SI RAM. The use of shadow RAMs reduces the number of available SI RAM entries for a TDM. **Figure 11** shows the SIx RAM Shadow Address Registers (SI1RSR and SI2RSR), which define the starting addresses of the shadow section in the SI RAM for each TDM. The same basic rules on bank assignment discussed in **Section 2** also apply to shadow RAM bank assignment. The current-route and shadow SI RAMs of different TDMs should not be interleaved. There is no way to independently allocate the shadow SI RAM banks for the transmit and receive, so the starting addresses of a TDM shadow RAM must be the same for the transmit and receive.

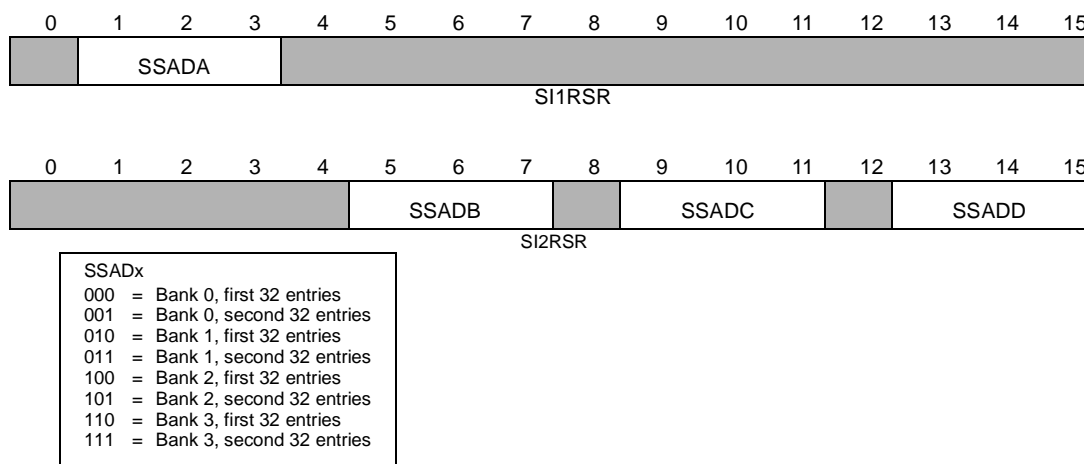


Figure 11. SI RAM Shadow Address Registers

3.2 Current-Route and Shadow RAM Switching

Figure 12 shows the SI_x Command Registers (SI1CMDR and SI2CMDR), which allow the shadow RAM for the TDMs to replace the current-route RAM. Setting the CSRR_x causes the receiver to replace the current-route RAM with the shadow RAM. Similarly, setting the CSRT_x causes the transmitter to replace the current-route RAM with the shadow RAM. The original current-route RAM becomes the shadow RAM and *vice versa*. The SI clears these bits as soon as the switch completes. The switch command can be applied at any time within a frame period, and the current-route and shadow RAM exchange occurs at the next frame.

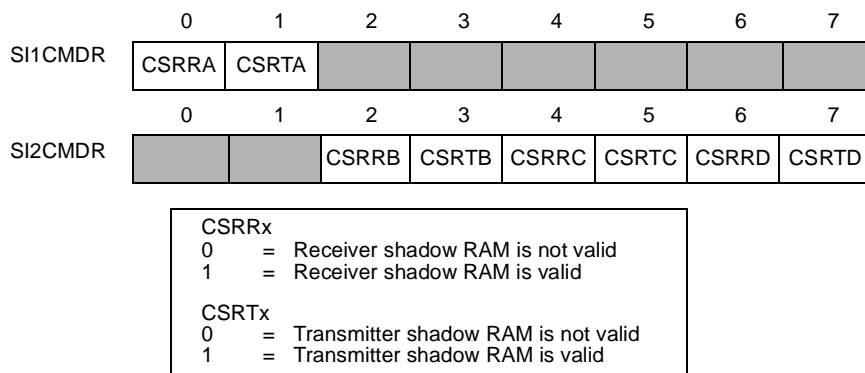


Figure 12. SI Command Registers

Figure 13 shows the SI Status Registers (SI1STR and SI2STR), which can monitor the entries in use at any time. These registers identify whether the current-route entries are the first entries used or the entries originally defined as shadow RAM entries. The status bits are valid only when the corresponding bits in the SI_xCMDR are cleared; that is, when the CPM is programmed to transfer control from one set of entries to the other. The SI RAM entries can be read at any time, but for proper SI operation, do not attempt to write the current-route RAM.

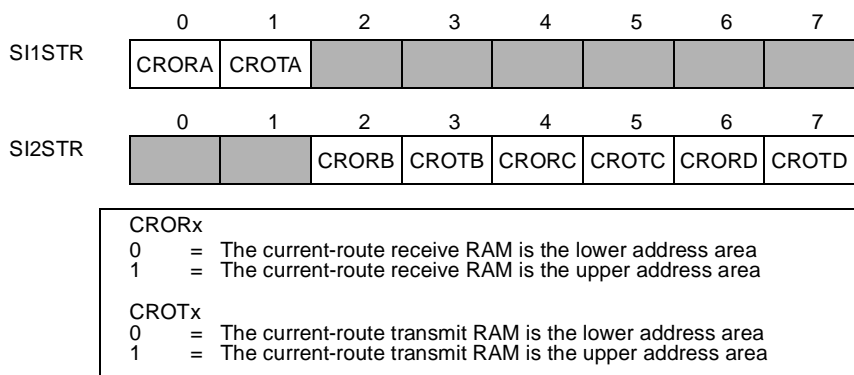
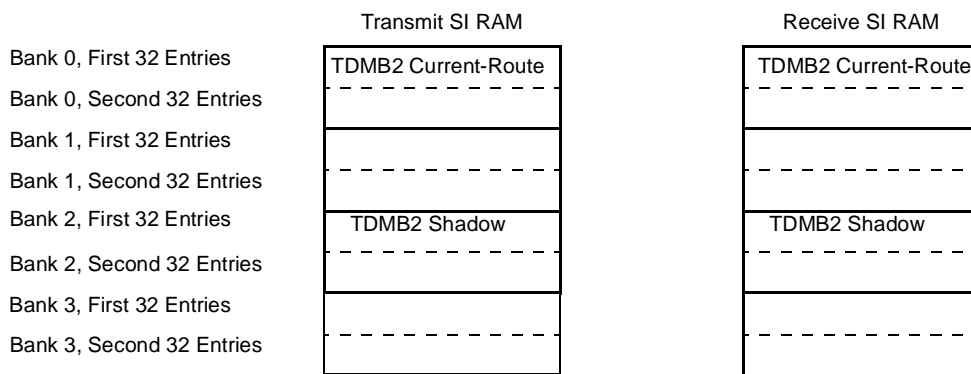


Figure 13. SI Status Registers

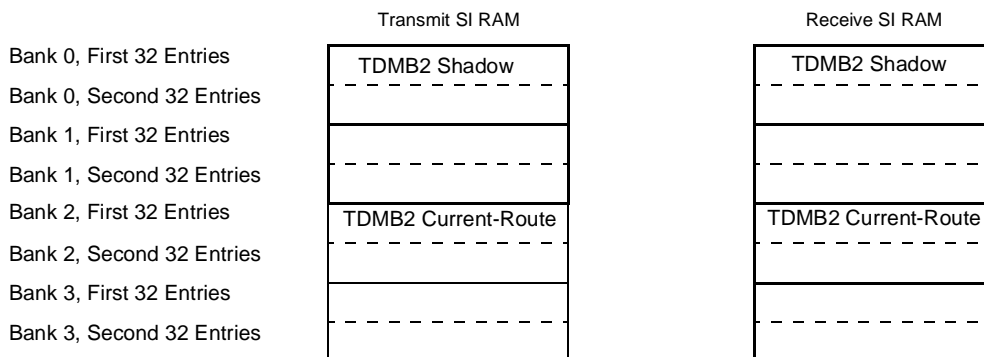
3.3 Dynamic Switching Example

This section presents an example of dynamic frame switching. Initially, Bank 0 and Bank 1 are occupied by the current-route RAM for TDMB2. Bank 2 and Bank 3 are occupied by the shadow RAM. The switch command can be applied at any time within a frame period by setting the SI2CMDR[CSRRB, CSRTB] bits. When the next frame sync arrives, the shadow RAM entries become the current-route entries. The CPM automatically resets the SI2CMDR[CSRRB, CSRTB] bits. The steps in this process are as follows:

1. In the initial state, set the following entries:
 - The first 32 entries for current-route SI RAM: SI2BMR[SADB] = 000 for Bank 0
 - The first 32 entries for shadow SI RAM: SI2RSR[SSADB] = 100 for Bank 2



2. Issue the switch command: SI2CMDR[CSRRB, CSRTB] = 1.
3. Shadow RAM becomes the current-route RAM, and the SI resets SI2CMDR[CSRRB, CSRTB] = 0.



4 SI RAM Entries

Each 16-bit SI RAM entry defines the number of bits or bytes to route to the serial controllers and determines when the four strobes are asserted and deasserted. Since the maximum number of SI RAM entries is 256 and each entry can define up to 8 bytes of data, the maximum frame length that can be supported is:

$$(8 \text{ bytes/entry}) \times (256 \text{ entries}) = 2048 \text{ bytes} = 16384 \text{ bits}$$

The definition of the SI RAM entry depends on whether an MCC channel or a non-MCC channel is sent or received on the TDM. For the FCC, SCC, or SMC channels, the SI RAM entry with the most significant bit cleared is used, as shown in **Figure 14**. However, for MCC channels, the MCC SI RAM with the most significant bit set is used, as shown in **Figure 16**.

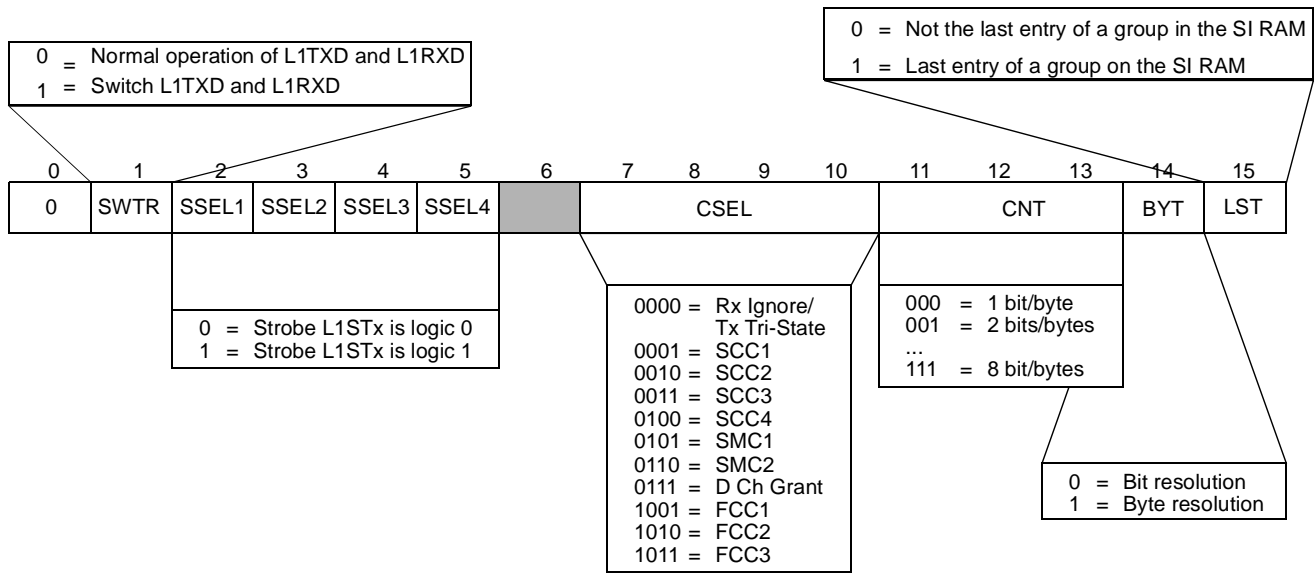


Figure 14. SI RAM Entry for Non-MCC Channels

Definitions of the bits shown in **Figure 14** are as follows:

- SWTR.** Valid only in the receive SI RAM entries and ignored in the transmit SI RAM entries. Normally, data is sent on L1TXD and received on L1RXD. When SWTR is cleared, stations A and B cannot communicate with each other over a TDM as shown in **Figure 15**. Both stations receive the same data on L1RXD and transmit on the same L1TXD signal. When the SWTR bit is set, the transmit and receive signals are switched so that receive data is received on L1TXD and transmit data is sent on L1RXD. Station B can transmit data to station A by setting the SWTR bit in its receive SI RAM entry.

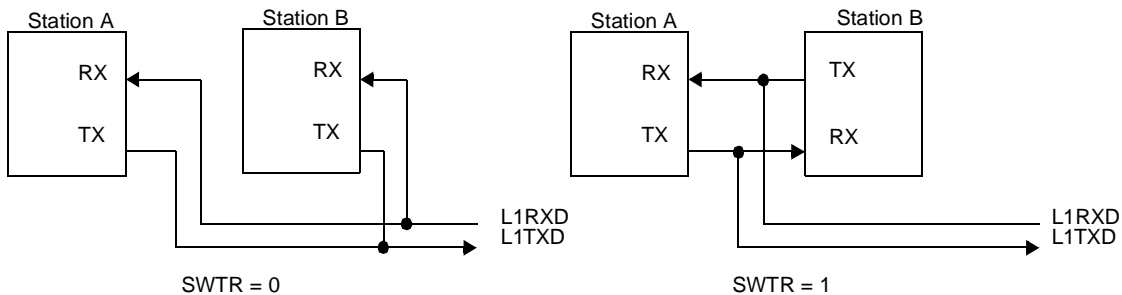


Figure 15. Switching Transmit and Receive Signals

- *SSEL[1–4]*. The L1ST[1–4] strobes are asserted and deasserted according to these bits. The value of a strobe signal is the logical OR of the corresponding SSELx bit of the receive and the transmit SI RAM. Multiple strobes can be asserted simultaneously. A strobe asserted on the last entry, that is, LST = 1, is deasserted after the last entry is processed.
- *CSEL*. Selects the serial controller to which the entry routes. This field selects the FCCs, SCCs, and SMCs.
- *CNT*. Indicates the number of bits or bytes minus one that are controlled by the entry. The *BYT* field indicates whether the *CNT* field the number of bits or bytes. For example an entry with *CNT*=000 and *BYT*=1 indicates 1 byte and entry with *CNT* = 111 and *BYT* = 0 indicates 8 bits. A maximum of eight bytes is allowed per entry.
- *LST*. Set in the last entry in this SI RAM. The *LST* bit of all other entries is cleared. *LST* allows the SI to wait for the frame sync signal to start the next frame. Because *LST* is active only in odd-numbered entries, assuming the entry count starts with zero, there must be an even number of entries.

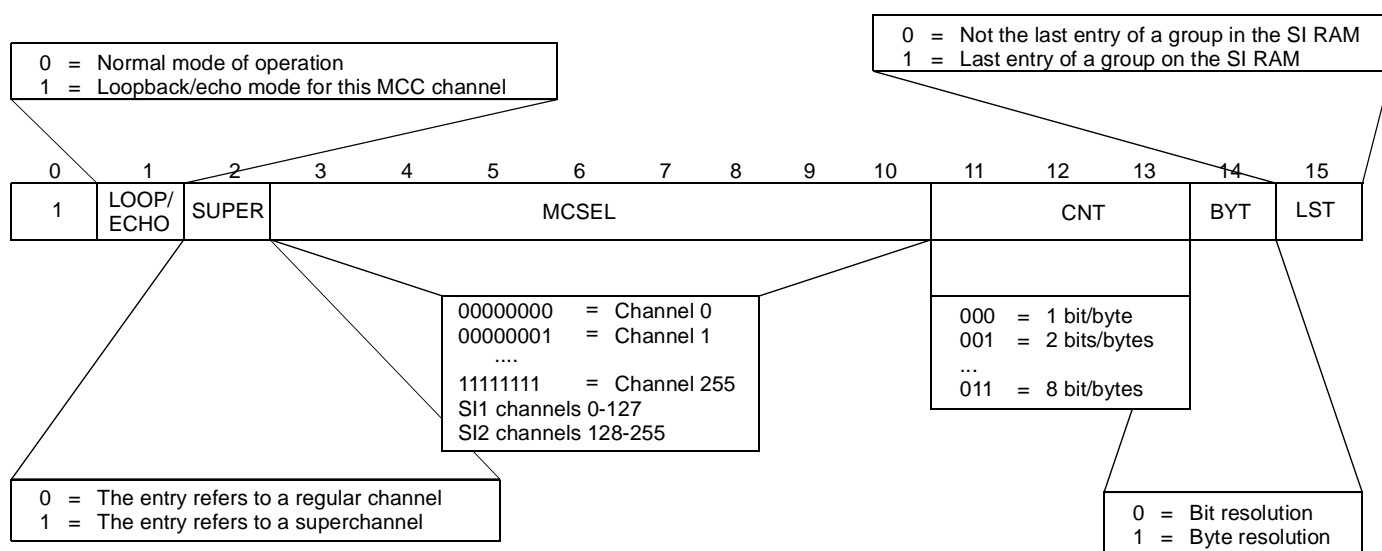


Figure 16. SI RAM Entry for MCC Channels

Definitions of the bits shown in **Figure 16** are as follows:

- *LOOP/ECHO*. Enables channel loopback in the receive SI RAM or echo mode in the transmit SI RAM. When this bit is set in the receive SI RAM entry, the channel’s transmit data is looped back to the receive data signal. When this bit is set in the transmit SI RAM, the channel receive data is echoed to the transmit data signal.
- *SUPER*. Defines whether the channel is a regular channel or a superchannel. Typically, one timeslot is assigned to one channel. However, a channel may require multiple timeslots. A superchannel is a channel that is allocated more than one timeslot—for example, a T1 frame has 24 timeslots. **Figure 17** shows a T1 frame with superchannels 2 and 8. Channel 2 is allocated four timeslots and channel 8 is allocated two timeslots per frame.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	2	2	2	2	4	5	6	7	8	9	8	10	11	12	13	14	15	16	17	18	19	20	21

Figure 17. Superchannel Example

A superchannel table (SCT) must be created for superchannels in the transmit SI RAM but not for superchannels in the receive SI RAM. A regular channel uses four bytes of FIFO on the transmit side, but a superchannel uses only half that number of bytes. The SCT redirects a superchannel's timeslot to a different (virtual) channel number so that the superchannel can use more FIFO than the allocated two bytes. It essentially increases the FIFO size to two times the number of timeslots in the superchannel. In **Figure 17**, superchannel 2 uses four timeslots, so the transmit FIFO is 2 bytes \times 4 = 8 bytes FIFO. Similarly, superchannel 8 uses two timeslots, so its transmit FIFO size is 4 bytes. In the receive SI RAM, transparent superchannels that require slot synchronization must be programmed as superchannels. Slot synchronization ensures that a channel's receive data is aligned in the receive buffer starting from the first timeslot after a sync pulse. When a new frame begins, the first timeslot of a superchannel is stored at the beginning of the buffer. One byte of FIFO is allocated for each superchannel in the receive SI RAM. Transparent superchannels that do not require slot synchronization and HDLC channels can be programmed in the receive SI RAM as regular channels. Clearing the SUPER bit for these channels is more efficient since the number of channels allocated for each superchannel is two bytes.

- *MCSEL*. Indicates the MCC channel to which the bits or byte is routed. For SI1, the possible MCSEL field channels are 0 through 127. For SI2, the possible MCSEL field channels are 128 through 255. For superchannel entries in the transmit SI RAM, MCSEL provides an offset from the base of the SCT into the SCT containing the actual channel number. **Section 4.2.2** provides an example of how MCSEL is used in the transmit SI RAM with superchannels.
- *CNT and BYT*. For regular channels, these fields indicate the number of bits or bytes minus one that are controlled by the entry. BYT indicates whether CNT holds the number of bits or bytes. For superchannels, CNT:BYT not only indicate the count size but also define whether the SI RAM entry is for the first timeslot of a superchannel. For the first timeslot of a superchannel, CNT:BYT = 0001. For subsequent timeslots of a superchannel, CNT:BYT = 1110. These combinations are the only two valid settings for superchannels. Note that they both indicate a count size of 8 bits or 1 byte.
- *LST*. Sets the last entry in this SI RAM. The LST bit of all other entries is cleared. LST allows the SI to wait for the frame sync signal to start the next frame. Because LST is active only in odd-numbered entries, assuming the entry count starts with zero, there must be an even number of entries.

4.1 SI RAM Programming Example 1

When the SI RAM is programmed for a user-defined frame and a frame sync pulse occurs, the data is routed as follows (see **Figure 18**):

- First 10 bits to the SCC1
- Next bit to the SMC1
- Next 8 bits to the SCC2
- Next four bits to the FCC3
- Last 8 bits to a device enabled by LIST3

The example shown in **Figure 18** involves non-MCC channels, so the SI RAM entry structure with bit 0 cleared is used as shown. The routing proceeds as follows:

- The first timeslot requires that 10 bits be routed to SCC1. Since the maximum number of bits or bytes per entry is eight, this timeslot requires two entries, as follows:
 - The first entry defines the first eight bits of SCC1. The CSEL field is programmed with a value of 0001 to specify SCC1. CNT is programmed with a value of 111 to indicate a count of 8. BYT is cleared to indicate that the CNT field specifies the number of bits.
 - The second entry defines the next two bits of SCC1 and is the same as the first entry with the exception of CNT. To specify a count of two bits, CNT is programmed with a value of 001.
- The second timeslot requires one bit to be routed to SMC1.
 - In the third SI RAM entry, CSEL is programmed with a value of 0101 to specify SMC1. CNT and BYT are cleared to indicate a count of 1 bit.
- In the third timeslot:
 - The fourth SI RAM entry routes eight bits to SCC2. CSEL is programmed with a value of 0010 to indicate SCC2. CNT is cleared to indicate a count of 1, and BYT is set to indicate that the count is the number of bytes.
- In the fourth timeslot:
 - The fifth SI RAM entry routes four bits to FCC3. CSEL is programmed with a value of 1011 to indicate FCC3. CNT is programmed with a value of 011 to specify a count of 4, and BYT is cleared to indicate that the count is the number of bits.
- In the fifth timeslot:
 - The sixth SI RAM entry routes eight bits to strobe L1ST3. CSEL is cleared so that the transmit signal is tri-stated and the receive signal stops receiving data. The SSEL3 bit is set to assert L1ST3. CNT is programmed with a value of 111 to specify a count of 8, and BYT is set to indicate that the count is the number of bits. LST is set to indicate that this entry is the last entry to be executed.

The transmit and receive could have different routing, depending on the application requirements. If the same routing is required for the receiver and the transmitter, then the receive and transmit SI RAM entries must be assigned with the same values.

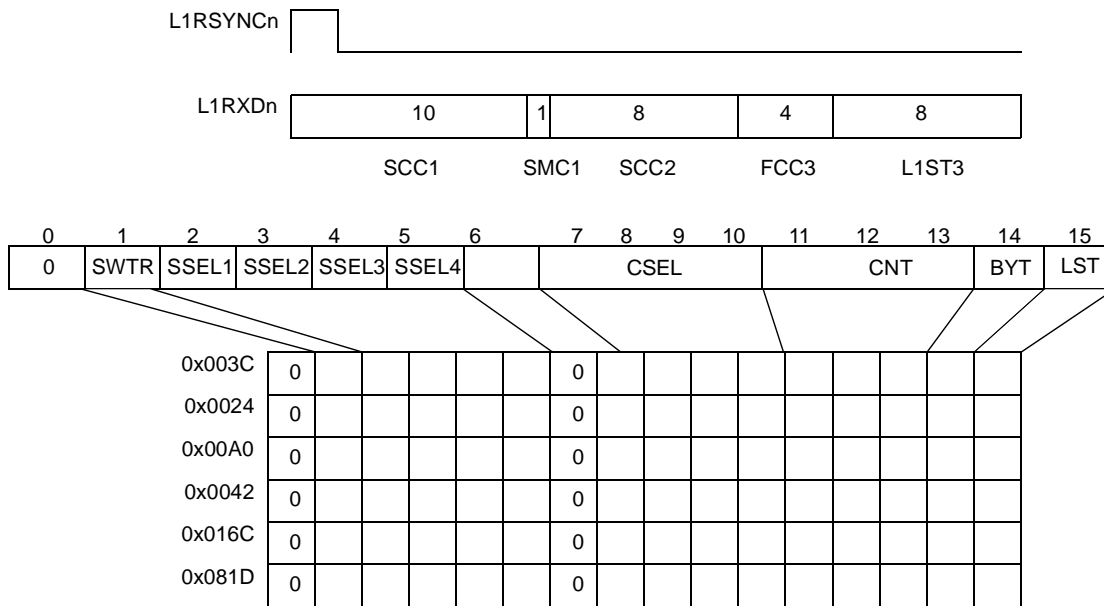


Figure 18. SI RAM Programming Example

4.2 SI RAM Programming Example 2

When the SI RAM is programmed to use superchannels on a T1 frame and a frame sync pulse occurs, transparent channels requiring slot synchronization are routed as shown in **Figure 19**. The channels are transparent with slot synchronization, and channels 2 and 5 are superchannels.

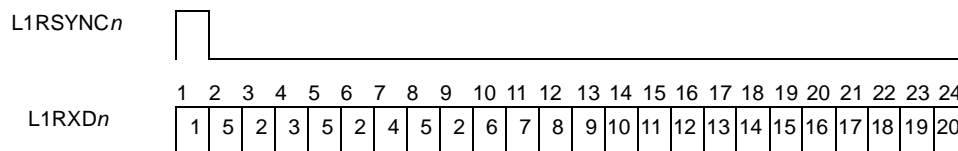


Figure 19. SI RAM Programming Example 2

4.2.1 Receive SI RAM

Since the example shown in **Figure 20** uses a T1 frame, each of the 24 timeslots is one byte wide. Timeslots 3, 6, and 9 are assigned to superchannel 2. Timeslots 2, 5, and 8 are assigned to superchannel 5. All other timeslots are occupied by regular channels. Slot synchronization ensures that the data is aligned in the receiver buffer, starting from the first timeslot after a frame sync pulse. The first byte of a superchannel is received at the beginning of a buffer. When slot synchronization is required, the SUPER bit must be set, but a superchannel table is not required. In this example, the MCC bit is set in all entries to indicate that all channels are MCC. The LOOP/ECHO bit is cleared in all entries to specify that there is no loopback. The routing is as follows:

- The first entry is for timeslot 1 and is routed to channel 1, which is not a superchannel, so SUPER = 0. The channel number is MSEL = 1. CNT = 0 to indicate a count of 1 and BYT = 1 to indicate that the CNT value is the number of bytes. Entries for regular channels 3, 4, and 6–20 are programmed the same way.
- The second entry is for timeslot 2 and is routed to channel 5, which is a superchannel, so SUPER = 1. The channel number is MSEL = 5. Since this timeslot is the first byte of superchannel 5, CNT:BYT = 0001. Since slot synchronization is required, this data is received at the beginning of a receive buffer.

- Timeslot 5 belongs to superchannel 5. The next available SCT entry is entry 5, which corresponds to channel 5. Virtual channel 5 is written into MCSEL. The SCT entry 5 is written with the real channel number, which is 5. Since this byte is not the first entry for superchannel 5, CNT:BYT = 1110.
- Timeslot 6 belongs to superchannel 2. The next available SCT entry is entry 21, which corresponds to channel 21. Virtual channel 21 is written into MCSEL. The SCT entry 21 is written with the real channel number, which is 2. Since this byte is not the first entry for superchannel 2, CNT:BYT = 1110.
- Timeslot 8 belongs to superchannel 5. The next available SCT entry is entry 22, which corresponds to channel 22. Virtual channel 22 is written into MCSEL. The SCT entry 22 is written with the real channel number, which is 5. Since this byte is not the first entry for superchannel 5, CNT:BYT = 1110.
- Timeslot 9 belongs to superchannel 2. The next available SCT entry is entry 23, which corresponds to channel 23. Virtual channel 23 is written into MCSEL. The SCT entry 23 is written with the real channel number, which is 2. Since this byte is not the first entry for superchannel 2, CNT:BYT = 1110.

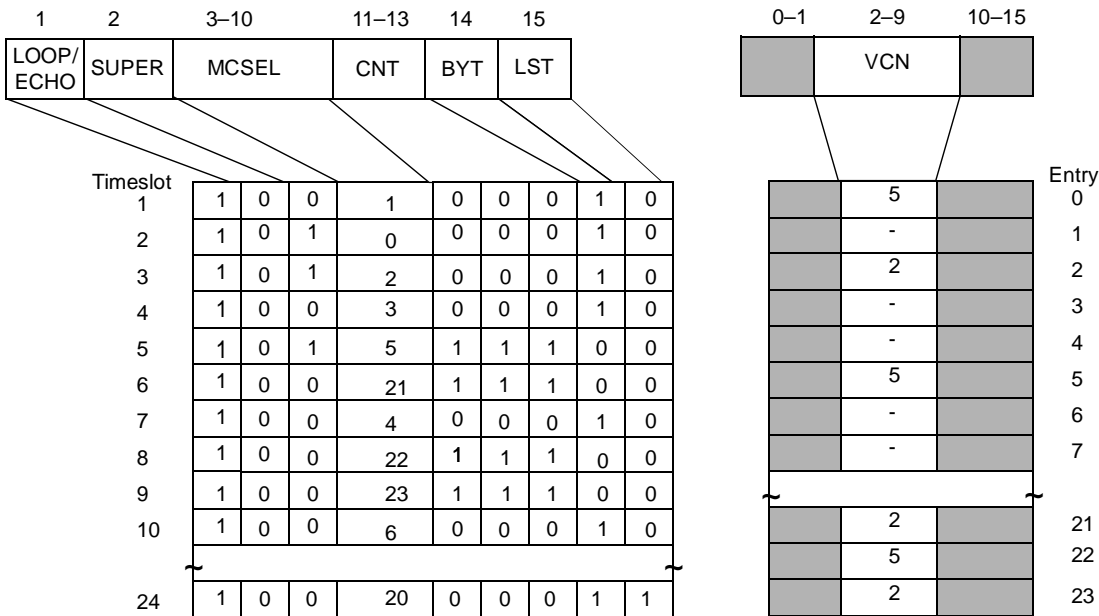


Figure 21. Transmit SI RAM Programming Example 2

5 SI RAM Programming Example 3

The example shown in **Figure 22** uses the same routing as the previous example, except that the channels are in HDLC format and channels 2 and 5 are superchannels.

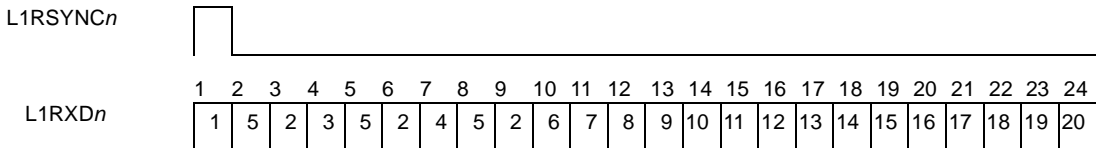


Figure 22. SI RAM Programming Example 3

5.1 Receive SI RAM

HDLC superchannels and transparent superchannels that do not require slot synchronization are programmed as regular channels in the receive SI RAM. It is efficient to program these channels as regular channels since the FIFO allocated for each channel is two bytes. The MCC bit is set in all entries to indicate that all channels are MCC. LOOP/ECHO is cleared in all entries to indicate no loopback. SUPER is cleared to program all channels, including superchannels, as regular channels. Routing is as follows:

- All timeslots belonging to superchannel 2 are programmed with MCSEL = 2; all timeslots belonging to superchannel 5 are programmed with MCSEL = 5.
- CNT:BYT in each entry is written with a value of 0001 to indicate a count of one byte.
- LST in timeslot 24 is set to indicate that the current entry is the last entry for the TDM used.

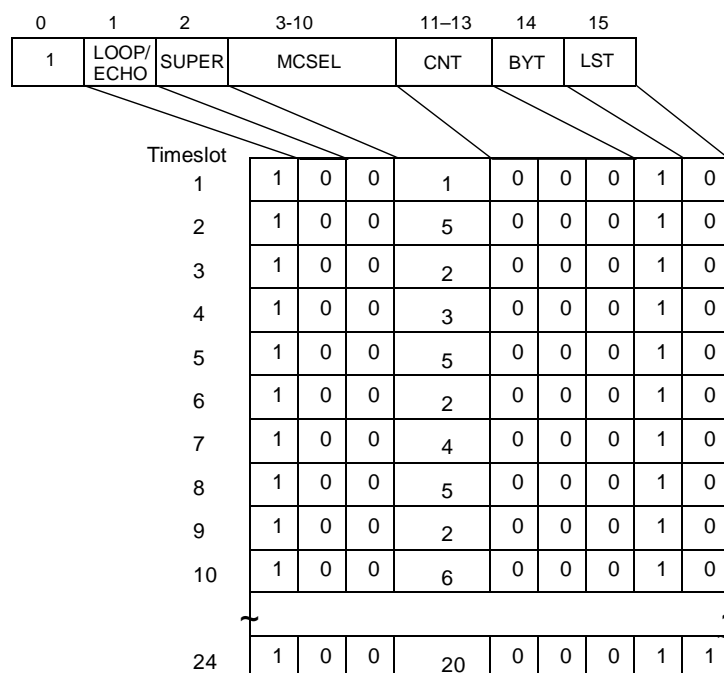


Figure 23. Receive SI RAM Programming Example 3

5.1.1 Transmit SI RAM

The transmit SI RAM for HDLC superchannels is programmed the same way as the transmit SI RAM for transparent superchannels with slot synchronization in **Section 4.2.2**. Since the SUPER bit is set for the superchannels, an SCT must be created.

5.2 Dynamic Switching with Superchannels

The SCT cannot be changed dynamically, so both the primary and shadow SI RAM configuration must conform to the SCT configuration. The example in **Figure 24** shows how to create a primary and shadow RAM configuration when dynamic switching with superchannels is used. The primary SI RAM is configured for frame n , which is the same channel assignment as in the previous examples. The shadow SI RAM is configured for frame $n + 1$, as shown in **Figure 24**.

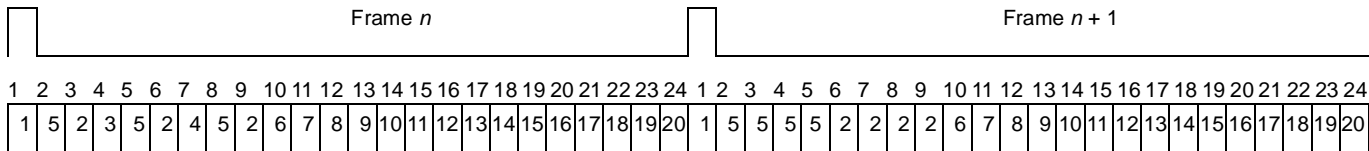


Figure 24. SI RAM Programming Example 4

5.2.1 Primary Transmit SI RAM

The channel assignment for frame *n* is the same as for the previous examples, so the primary transmit SI RAM and the SCT in this example are programmed the same way (see Section 4.2). Note that the SCT shown in Figure 25 is not the final SCT, which must be modified to accommodate the shadow transmit SI RAM configuration.

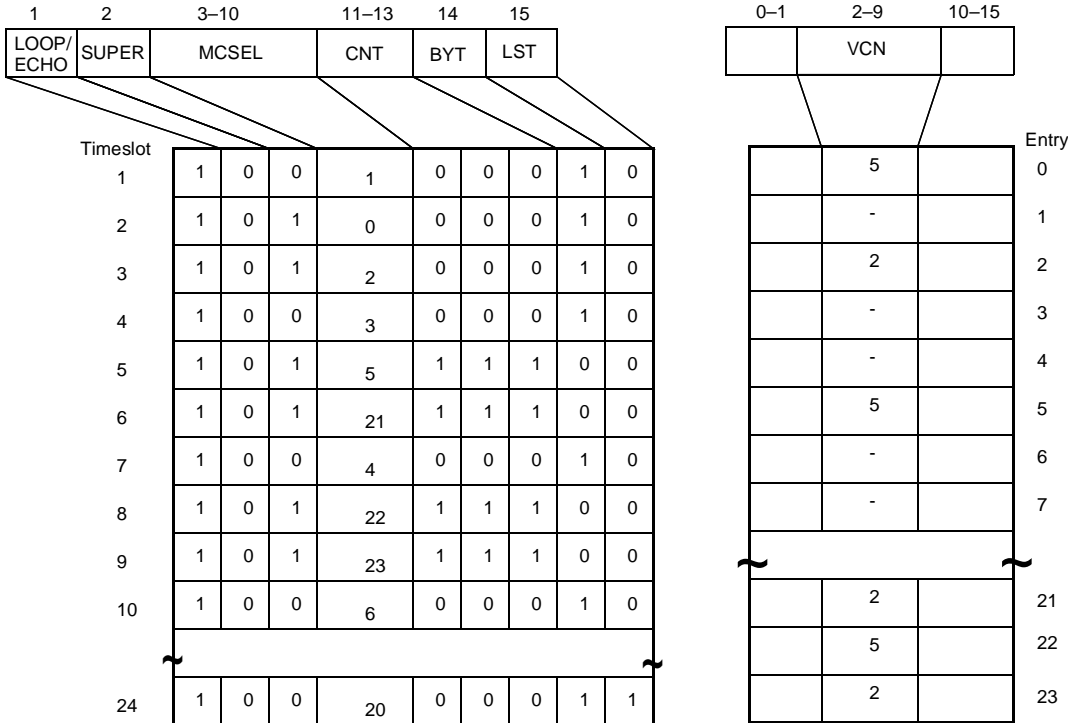


Figure 25. Primary Transmit SI RAM and SCT Example 4

5.2.2 Shadow Transmit SI RAM

Frames *n* and *n + 1* have different channel assignments, as shown in Figure 26. The shadow RAM is configured for frame *n + 1*, which allocates four consecutive timeslots each to channels 2 and 5. The timeslots that differ from those of the previous frame are 3, 4, 7, and 8 (marked with asterisks). All other timeslots have the same channel assignments as the previous frame.

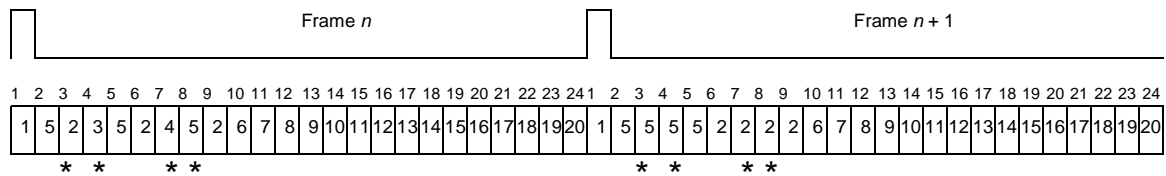


Figure 26. SI RAM Programming Example 4

The timeslots with the same channel assignments as the previous frame contain the same MCSEL setting, so the SCT remains the same. Only timeslots 3, 4, 7, and 8 contain new MCSEL values. In the primary transmit SI RAM, channels 0–23 are used in MCSEL. These channels correspond to entries 0–23 in the SCT, which should not be modified. Channels 24–127 are available for use as virtual channels, so entries 24 and higher in the SCT can be used to redirect these channels to superchannels 2 and 5.

- Timeslot 3 belongs to superchannel 5. The next available SCT entry is entry 24, which corresponds to channel 24. Virtual channel 24 is written into MCSEL. SCT entry 24 is written with the real channel number, which is 5. Since this byte is not the first entry for superchannel 5, CNT:BYT = 1110.
- Timeslot 4 also belongs to superchannel 5. The next available SCT entry is entry 25, which corresponds to channel 25. Virtual channel 25 is written into MCSEL. SCT entry 25 is written with the real channel number, which is 5. Since this byte is not the first entry for superchannel 5, CNT:BYT = 1110.
- Timeslot 7 belongs to superchannel 2. The next available SCT entry is entry 26, which corresponds to channel 26. Virtual channel 26 is written into MCSEL. SCT entry 26 is written with the real channel number, which is 2. Since this byte is not the first entry for superchannel 2, CNT:BYT = 1110.
- Timeslot 8 belongs to superchannel 2. The next available SCT entry is entry 27, which corresponds to channel 27. Virtual channel 27 is written into MCSEL. SCT entry 27 is written with the real channel number, which is 2. Since this byte is not the first entry for superchannel 2, CNT:BYT = 1110.

The shadow transmit SI RAM and SCT entries are shown in **Figure 27**. SCT entries 24–27 are added to support the channel assignment in the shadow SI RAM. All other entries remain the same to support the channel assignment in the primary SI RAM.

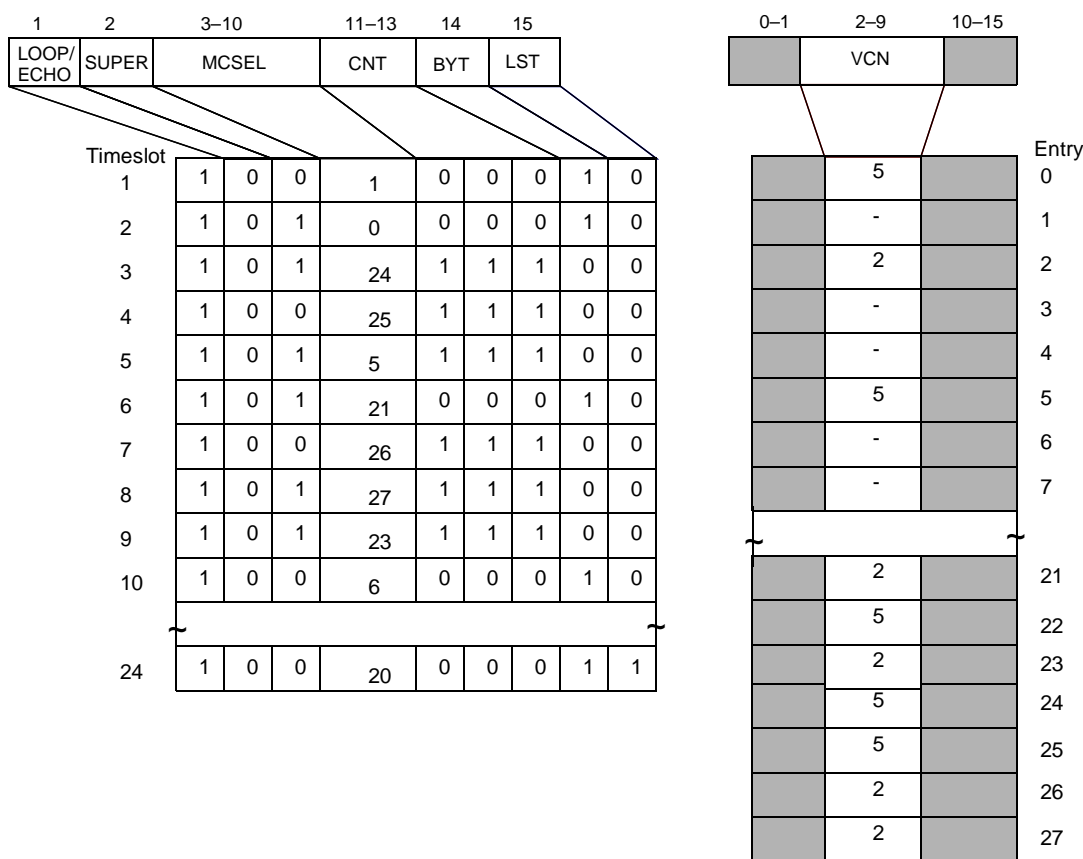


Figure 27. Shadow Transmit SI RAM and SCT Example 4

6 Summary

This section summarizes the main points for SI RAM bank assignment. These rules apply to both current-route and shadow RAM:

- The starting bank address of a TDM in the SI RAM must be a multiple of 32 entries.
- Multiple TDMs cannot share the same bank.
- The starting bank address of a TDM in the transmit and receive SI RAM must be the same.
- There must be an even number of SI RAM entries.
- For regular channels, the CNT:BYT fields indicate the number of bits or bytes minus one that are controlled by the entry.
- For superchannels:
 - CNT:BYT = 0001 indicates that the entry is the first timeslot of the superchannel.
 - CNT:BYT = 1110 indicates that the entry is not the first timeslot of the superchannel.
- An SCT must be created when superchannels are defined in the transmit SI RAM. The SCT cannot be changed dynamically.
- Transmit channel FIFO size:

- A regular channel uses four bytes of FIFO.
- A superchannel uses $2 \times n$ bytes of FIFO, where n is the number of timeslots assigned to the superchannel.
- In the transmit SI RAM entries with $\text{SUPER} = 1$, MCSEL indicates the virtual channel number and provides an offset from the base of the SCT into the SCT, which contains the actual channel number.
- In the receive SI RAM entries:
 - Transparent superchannels that require slot synchronization must be programmed as superchannels. An SCT is not required.
 - Transparent superchannels that do not require slot synchronization and HDLC channels can be programmed in the receive SI RAM as regular channels.

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