

Application Note

AN2415/D
Rev. 0, 04/2003

MC9328MX1/MXL
Programming the LCD
Controller for Sharp TFT
Panel



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1 Introduction

The MC9328MX1/MXL processor's LCD Controller can directly interface with Sharp HR-TFT panel. In addition to the standard signals, four special signals dedicated for the Sharp panels are:

Table 1.

| Signal | Remarks |
|---------|------------------------------|
| SPL/SPR | Sampling Start Signal |
| CLS | Clock signal for gate driver |
| PS | Power save signal |
| REV | reverse control control |

In the MC9328MX1/MXL processor 1.0 , the rising edge of CLS, positive and negative edge of REV is hard coded. PS is an inversion of CLS. The delay of the falling edge of CLS is programmable and relative to the falling edge of SPL. REV toggle on the same timing relative to the last LD of the line, on every line.

In the MC9328MX1/MXL processor 2.0, both the rising and falling edge of CLS and transition edge of REV is programmable.



1.1 MC9328MX1/MXL – 1.0

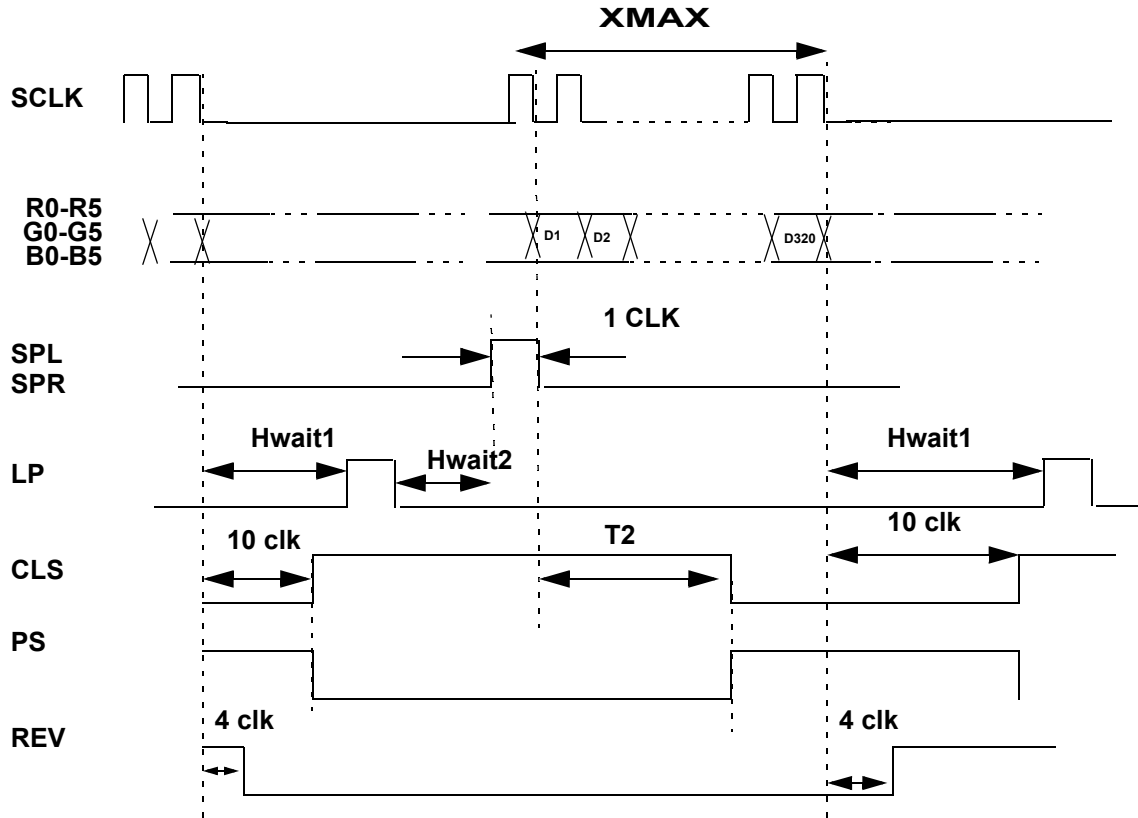


Figure 1.

- The pulse width of LP is programmable from 1 - 256, as controlled by register value hwidth
- PS as an inverted version of CLS
- T2 is equal to $pwm_scr0 * 256 + pwm_width$ in units of SCLK.
- SPL/SPR pulse width is fixed and aligned to the first data of the line.

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1.2 MC9328MX1/MXL - 2.0

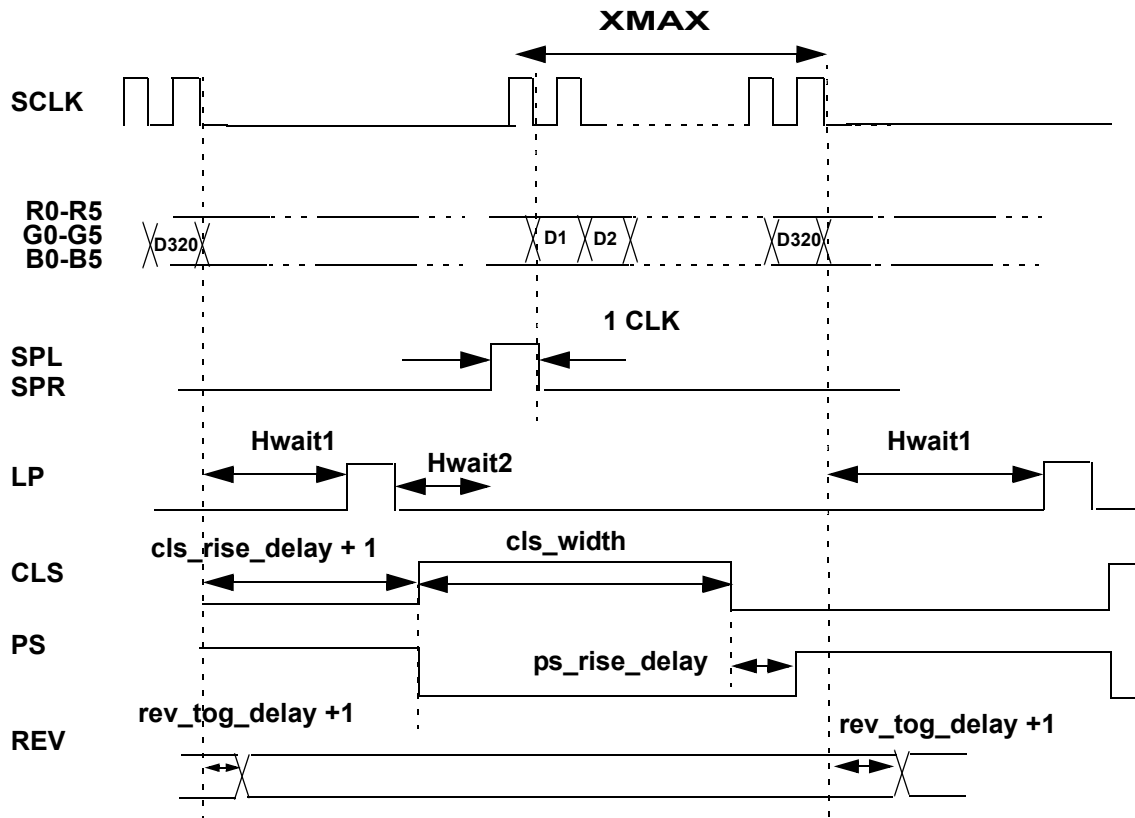


Figure 2.

- falling edge of PS aligns with rising edge of CLS
- delay of rising edge of PS is programmed by ps_rise_delay
- CLS_WIDTH is equal to $pwm_scr0 * 256 + pwm_width$ in units of SCLK.
- SPL/SPR pulse width is fixed and aligned to the first data of the line.
- REV toggles every LP period.

1.3 Programming for Sharp HR 240 x 320 TFT

For MC9328MX1/MXL – 1.0

Table 2.

| Address | Setting |
|------------|------------|
| 0x00205018 | 0xF8008B42 |
| 0x0020501C | 0x4000f06 |
| 0x00205020 | 0x04000907 |

1.4 Programming for Sharp HR 320x 240 TFT

For MC9328MX1/MXL – 1.0

Table 3.

| Address | Setting |
|------------|------------|
| 0x00205018 | 0xF8008B42 |
| 0x0020501C | 0x4000f06 |
| 0x00205020 | 0x04000b03 |

1.5 LCDC DMA Setting

For SDRAM access, a fixed burst length of 8 is preferred.

Table 4.

| DMA Register | Setting |
|--------------------|---------|
| fixed burst length | 1 |
| high mark | 8 |
| low mark | 4 |

For heavy loaded bus, and SDRAM access a dynamic burst length is recommended.

Table 5.

| DMA Register | Setting |
|--------------------|--------------------|
| fixed burst length | 0 |
| high mark | 4<= high mark <= 8 |
| low mark | 8 |

1.6 LCDC Clock Setting

In the MC9328MX1/MXL processor, the `lcdc_clk`, which is derived from the same clock source as `hclk` must follow the following relationship in order to make LCDC work properly:

$$\text{lcdc_clk} = \text{PLL_output} / \text{PCLK_DIV2}$$

$$\text{hclk} = \text{PLL_output} / \text{BCLK_DIV}$$

(Please refer to manual for `PCLK_DIV2` and `BCLK_DIV`)

When `BCLK_DIV = 0` (i.e. clock out = clock in), `PCLK_DIV2` can be any value

When `BCLK_DIV = 1` (i.e. CLK out freq. is clock input freq. divided by 2) , `PCLK_DIV` must be 3, 7, or 15 etc.

This is to ensure the rising clock edge of `LCK_clk` is sync. with the rising edge of `hclk`. Otherwise timing problem will occur, and the output is un-predictable.



NOTES

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