

**Application Note**

AN2422/D  
Rev. 0, 04/2003

MC9328MX1/MXL  
DTACK Signal



Freescale Semiconductor, Inc. 2005  
ARCHIVED BY FREESCALE SEMICONDUCTOR, INC. 2005

ARCHIVED BY FREESCALE SEMICONDUCTOR, INC. 2005

By Angus Lai

1	DTACK Signal Description	1
2	Pin Configuration for DTACK	1
3	Note when Using DTACK	2
4	MC9328MX1 DTACK Signal Timing	3
5	MC9328MXL DTACK Signal Timing	7

## 1 DTACK Signal Description

The DTACK signal is the external input data acknowledge signal that only supported by CS[5]. When the external DTACK signal is used as a data acknowledge signal, the access cycle will terminate after the DTACK signal is asserted. This is useful for external device connected to Chip Select 5 use WAIT signal to indicate the end of wait state.

The maximum wait state supported by DTACK is 1022 clock cycle. The bus time-out monitor generates a bus error when a bus cycle is not terminated by the external DTACK signal after 1022 clocks counts have elapsed.

The maximum wait state supported by the DTACK signal at 96 MHz is 10.645us. This can be calculated by dividing the number of maximum wait state cycles (1022) by the system clock frequency (HCLK). For designs requiring a longer wait state time greater than 10.645us, it is necessary to reduce the system clock frequency HCLK to an appropriate value that is less than 96 MHz. The system clock HCLK can be divided by setting the BLCK\_DIV bits in the Clock Source Control Register to the desired value. For more detailed information about setting the BCLK\_DIV bits, see Chapter 12, “Phase-Locked Loop and Clock Controller.”

## 2 Pin Configuration for DTACK

DTACK input pin is the primary function of GPIO Port A17. To configura GPIO Port A17 as DTACK function:

1. Clear bit 17 of Port A GPIO In Use Register (GIUS\_A)
2. Clear bit 17 of Port A General Purpose Register (GPR\_A)

DTACK can be configured to use either a falling edge to indicate the end of wait state, or follow the wait signal protocol of PCMCIA/Compact Flash specification. To configure DTACK to use PCMCIA/Compact Flash wait signal protocol, the DTACK Select bit (DTACK\_SEL) in CS5U register should be set. The DTACK\_SEL bit is clear by default, that is, a falling edge is configured as end of wait state.

To enable DTACK for controlling the wait state in CS5, the Wait State Control bit (WSC) in CS5U register should be set as 111111.





### 3 Note when Using DTACK

1. When CS5 is set as half word access by DSZ bit of Chip Select 5 Lower Control Register and DTACK is enabled, only half word or byte access is valid. The EIM will not separate word access on CS5 into two halfword access cycles, as it will when programmable wait state is used instead.
2. When CS5 is set as byte access by DSZ bit of Chip Select 5 Lower Control Register and DTACK is enabled, only byte access is valid. The EIM will not separate word or half word access into four or two byte access cycles, as it will when programmable wait state is used instead.
3. In MC9328MXL processor, when DTACK is used, either the dtack input pin should be pull high by a external resistor, or the PA17 PUEN bit should be set so as to prevent the dtack input pin having a floating state.

Freescale Semiconductor, Inc.  
ARCHIVED BY FREESCALE SEMICONDUCTOR, INC. 2005

ARCHIVED BY FREESCALE SEMICONDUCTOR, INC. 2005

## 4 MC9328MX1 DTACK Signal Timing

The following figures show the access cycle timing with DTACK enabled used by chip-select 5 for 96MHz system clock. The signal values and units of measure for this figure are found in table below.

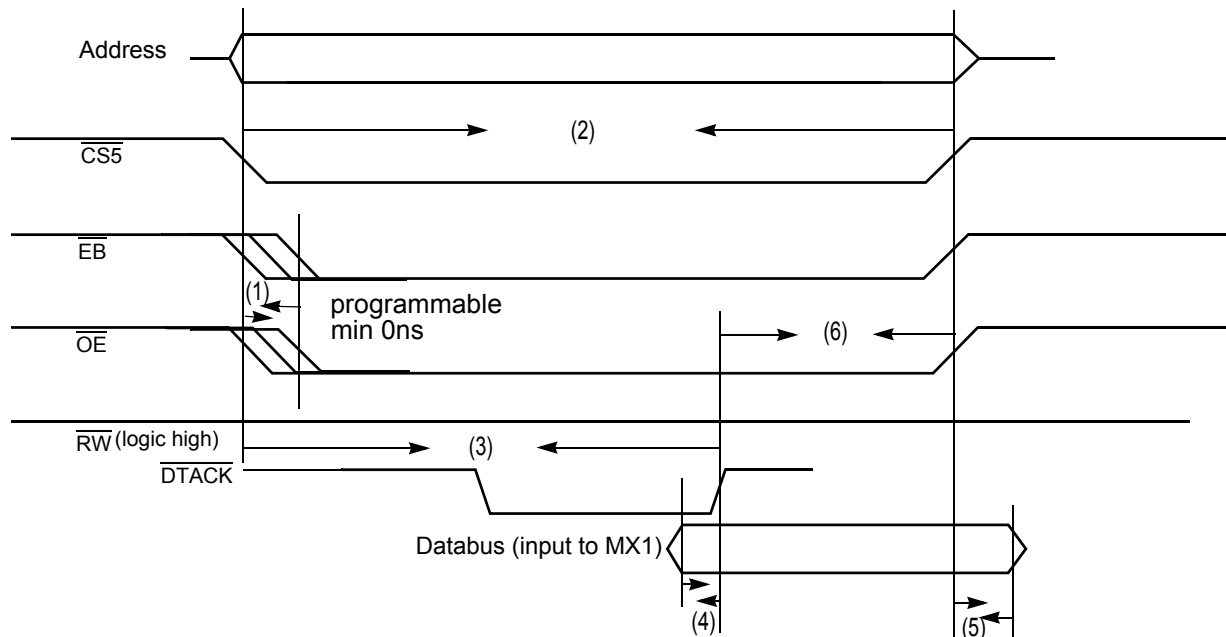


Figure 1.

Table 1. WSC=111111, DTACK\_SEL=1, HCLK = 96MHz, Read Cycle

Number	Characteristic	(3.0 ± 0.3) V		Unit
		Minimum	Maximum	
1	$\overline{OE}$ and $\overline{EB}$ assertion time	0	See note 3	ns
2	$\overline{CS5}$ pulse width	3T	--	ns
3	$\overline{DTACK}$ asserted after $\overline{CS5}$ is asserted	--	1020T	ns
4	data ready to $\overline{DTACK}$ asserted	0	--	ns
5	data hold timing after $\overline{OE}$ negated	0	--	ns
6	$\overline{DTACK}$ asserted to $\overline{OE}$ negated	30	--	ns

**Note:**

1. T is the system clock period. (For 96MHz system clock)
2.  $\overline{Address}$  becomes valid and  $\overline{CS5}$  asserts at the start of read access cycle.
3.  $\overline{OE}$  and  $\overline{EB}$  assertion time is programmable by OEA bit in  $\overline{CS5L}$  register
4. The external  $\overline{DTACK}$  input requirement is eliminated when  $\overline{CS5}$  is programmed to use internal wait state.

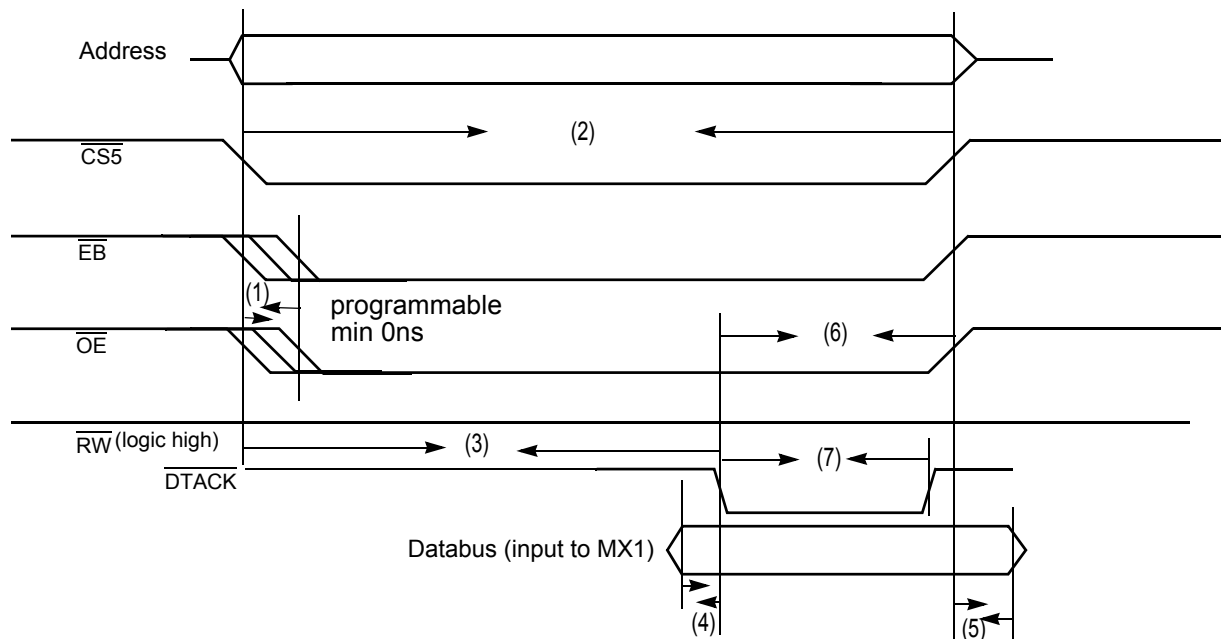


Figure 2.

Table 2. WSC = 111111, DTACK\_SEL=0, HCLK=96MHz, Read Cycle

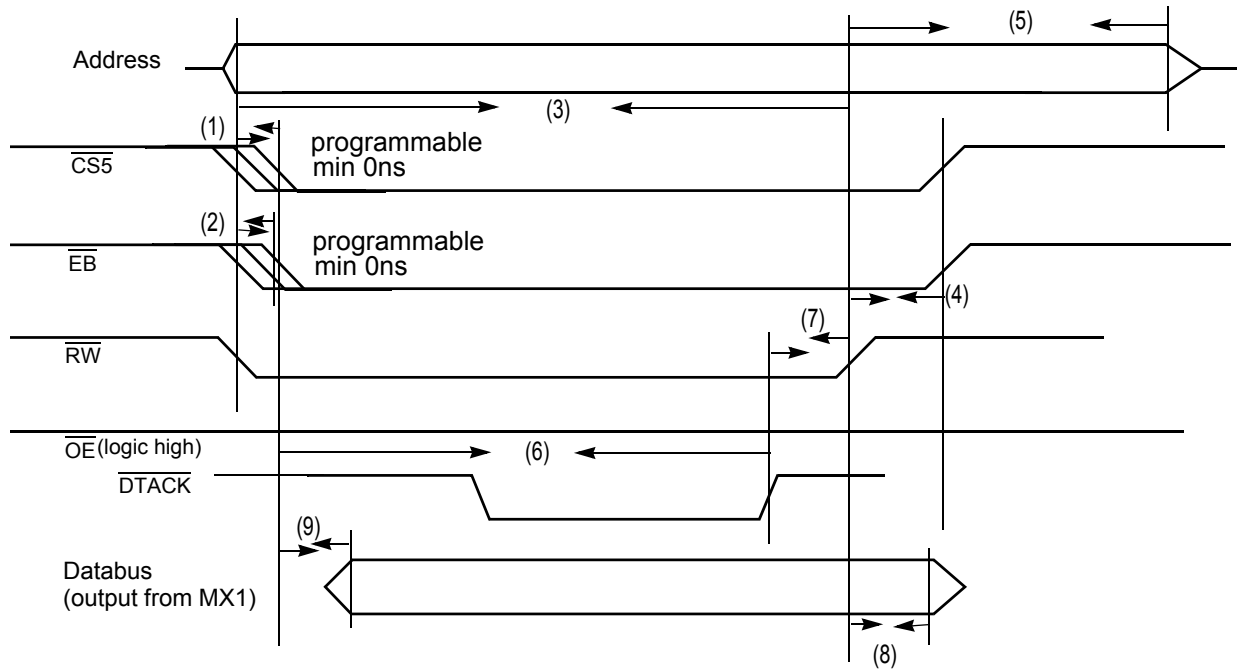
Number	Characteristic	(3.0 ± 0.3) V		Unit
		Minimum	Maximum	
1	OE and EB assertion time	0	See Note 3	ns
2	CS5 pulse width	3T	--	ns
3	DTACK asserted after CS5 is asserted	--	1020T	ns
4	data ready to DTACK asserted	0	--	ns
5	data hold timing after OE negated	0	--	ns
6	DTACK asserted to OE negated	30	--	ns
7	DTACK signal return to negation after asserted	1T	DTACK should get deasserted 1021 T after CS5 assertion.	ns

**Note:**

1. T is the system clock period. (For 96MHz system clock)
2. Address becomes valid and CS5 asserts at the start of read access cycle
3. OE and EB assertion time is programmable by OEA bit in CS5L register
4. The external DTACK input requirement is eliminated when CS5 is programmed to use internal wait state.

Freescale Semiconductor, Inc. ARCHIVED BY FREESCALE SEMICONDUCTOR, INC. 2005

ARCHIVED BY FREESCALE SEMICONDUCTOR, INC. 2005


**Figure 3.**
**Table 3. WSC = 111111, DTACK\_SEL=1, HKCL=96MHz, Write Cycle**

Number	Characteristic	(3.0 ± 0.3) V		Unit
		Minimum	Maximum	
1	$\overline{CS5}$ assertion time	See note 2.	--	ns
2	$\overline{EB}$ assertion time	See note 2	--	ns
3	$\overline{CS5}$ pulse width	3T	--	ns
4	$\overline{RW}$ negated before $\overline{CS5}$ and $\overline{EB}$ is negated	25	--	ns
5	$\overline{RW}$ negated to Address inactive	27	--	ns
6	$\overline{DTACK}$ asserted after $\overline{CS5}$ asserted	--	1020T	ns
7	$\overline{DTACK}$ asserted to $\overline{RW}$ negated	25	--	ns
8	data hold timing after $\overline{RW}$ negated	20	--	ns
9	data ready after $\overline{CS5}$ is asserted		10	ns

**Note:**

1. T is the system clock period. (For 96MHz system clock)
2.  $\overline{CS5}$  assertion can be controlled by CSA bits.  $\overline{EB}$  assertion can also be programmable by WEA bits in CS5L register.
3. Address becomes valid and  $\overline{RW}$  asserts at the start of write access cycle.
4. The external  $\overline{DTACK}$  input requirement is eliminated when  $\overline{CS5}$  is programmed to use internal wait state.

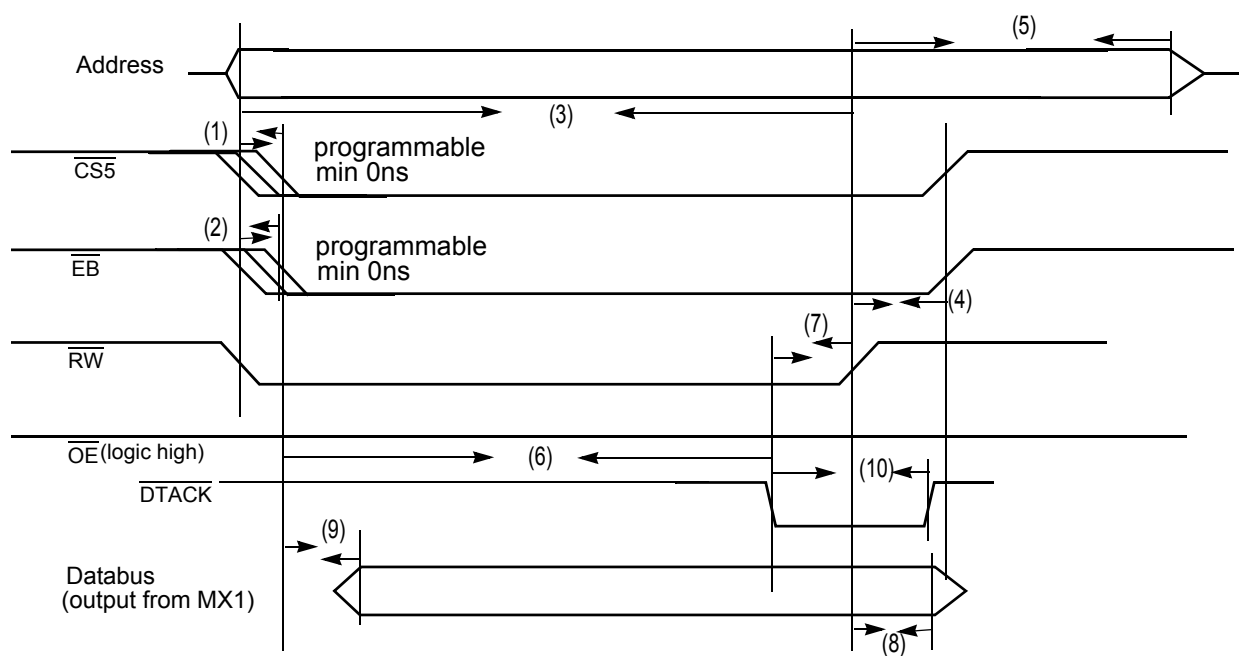


Figure 4.

Table 4. WSC = 111111, DTACK\_SEL=0, HCLK=96MHz, Write Cycle

Number	Characteristic	(3.0 ± 0.3) V		Unit
		Minimum	Maximum	
1	$\overline{CS5}$ assertion time	See note 2	--	ns
2	$\overline{EB}$ assertion time	See note 2	--	ns
3	$\overline{CS5}$ pulse width	3T	--	ns
4	$\overline{RW}$ negated before $\overline{CS5}$ and $\overline{EB}$ is negated	--	25	ns
5	$\overline{RW}$ negated to Address inactive	--	27	ns
6	$\overline{DTACK}$ asserted after $\overline{CS5}$ asserted	--	1020T	ns
7	$\overline{DTACK}$ asserted to $\overline{RW}$ negated	25	--	ns
8	data hold timing after $\overline{RW}$ negated	20	--	ns
9	data ready after $\overline{CS5}$ is asserted	--	10	ns
10	$\overline{DTACK}$ signal return to negation after asserted	1T	should get deasserted 1021 T after CS5 assertion.	ns

**Note:**  
 1. T is the system clock period. (For 96MHz system clock)  
 2. CS5 assertion can be controlled by CSA bits. EB assertion also can be programable by WEA bits in CS5L register.  
 3. Address becomes valid and  $\overline{RW}$  asserts at the start of write access cycle.  
 4. The external  $\overline{DTACK}$  input requirement is eliminated when  $\overline{CS5}$  is programmed to use internal wait state.

Freescale Semiconductor, Inc. ARCHIVED BY FREESCALE SEMICONDUCTOR, INC. 2005

ARCHIVED BY FREESCALE SEMICONDUCTOR, INC. 2005

## 5 MC9328MXL DTACK Signal Timing

The following figures show the access cycle timing with DTACK enabled used by chip-select 5 for 96MHz system clock. The signal values and units of measure for this figure are found in table below.

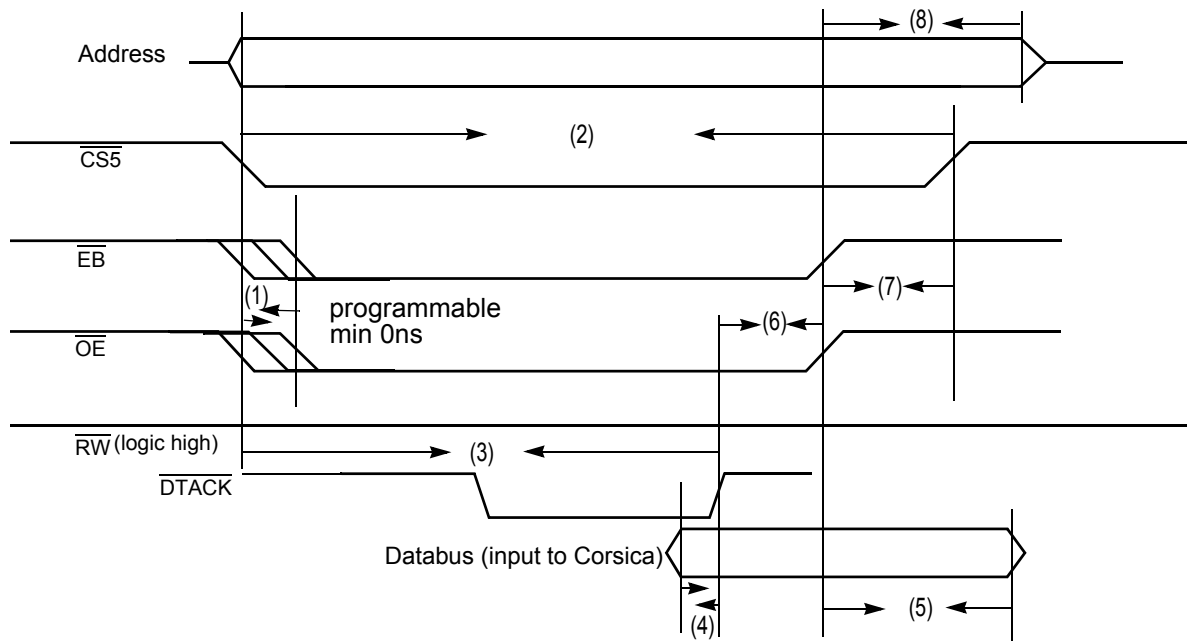


Figure 5.

Table 5. WSC=111111, DTACK\_SEL=1, HCLK=96MHz, Read Cycle

Number	Characteristic	(3.0 ± 0.3) V		Unit
		Minimum	Maximum	
1	$\overline{OE}$ and $\overline{EB}$ assertion time	0	See note 3	ns
2	$\overline{CS5}$ pulse width	3T	--	ns
3	$\overline{DTACK}$ asserted after $\overline{CS5}$ asserted	5	1022T	ns
4	data ready to $\overline{DTACK}$ asserted	0	--	ns
5	data hold timing after $\overline{OE}$ negated	20	--	ns
6	$\overline{DTACK}$ assert to $\overline{OE}$ negate	25	--	ns
7	$\overline{OE}$ negate to $\overline{CS5}$ negate	13	--	ns
8	$\overline{OE}$ negate to address invalid	45	--	ns

**Note:**

1. T is the system clock period. (For 96MHz system clock)
2. Address becomes valid and  $\overline{CS5}$  asserts at the start of read access cycle
3.  $\overline{OE}$  and  $\overline{EB}$  assertion time is programmable by OEA bit in  $\overline{CS5L}$  register
4. The external DTACK input requirement is eliminated when CS5 is programmed to use internal wait state.

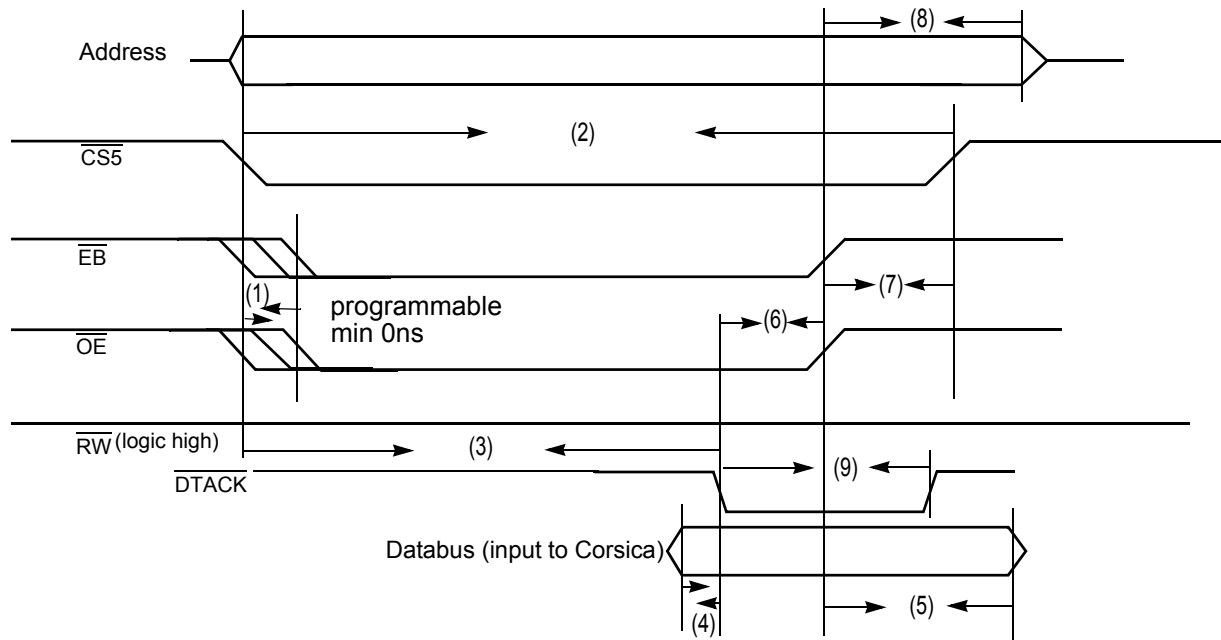


Figure 6.

Table 6. WSC = 111111, DTACK\_SEL=0, HCLK=96MHZ, Read Cycle

Number	Characteristic	(3.0 ± 0.3) V		Unit
		Minimum	Maximum	
1	$\overline{OE}$ and $\overline{EB}$ assertion time	0	See note 3	ns
2	$\overline{CS5}$ pulse width	3T	--	ns
3	$\overline{DTACK}$ asserted after $\overline{CS5}$ asserted	5	1022T	ns
4	data ready to $\overline{DTACK}$ asserted	0	--	ns
5	data hold timing after $\overline{OE}$ negated	20	--	ns
6	$\overline{DTACK}$ assert to $\overline{OE}$ negate	25	--	ns
7	$\overline{OE}$ negated to $\overline{CS5}$ negated	13	--	
8	$\overline{OE}$ negated to address invalid	15	--	
9	$\overline{DTACK}$ signal return to negation after asserted	1T	3T	ns

**Note:**

1. T is the system clock period. (For 96MHz system clock)
2. Address becomes valid and  $\overline{CS5}$  asserts at the start of read access cycle
3.  $\overline{OE}$  and  $\overline{EB}$  assertion time is programmable by OEA bit in  $\overline{CS5L}$  register
4. The external DTACK input requirement is eliminated when CS5 is programmed to use internal wait state.

Freescale Semiconductor, Inc. ARCHIVED BY FREESCALE SEMICONDUCTOR, INC. 2005

ARCHIVED BY FREESCALE SEMICONDUCTOR, INC. 2005

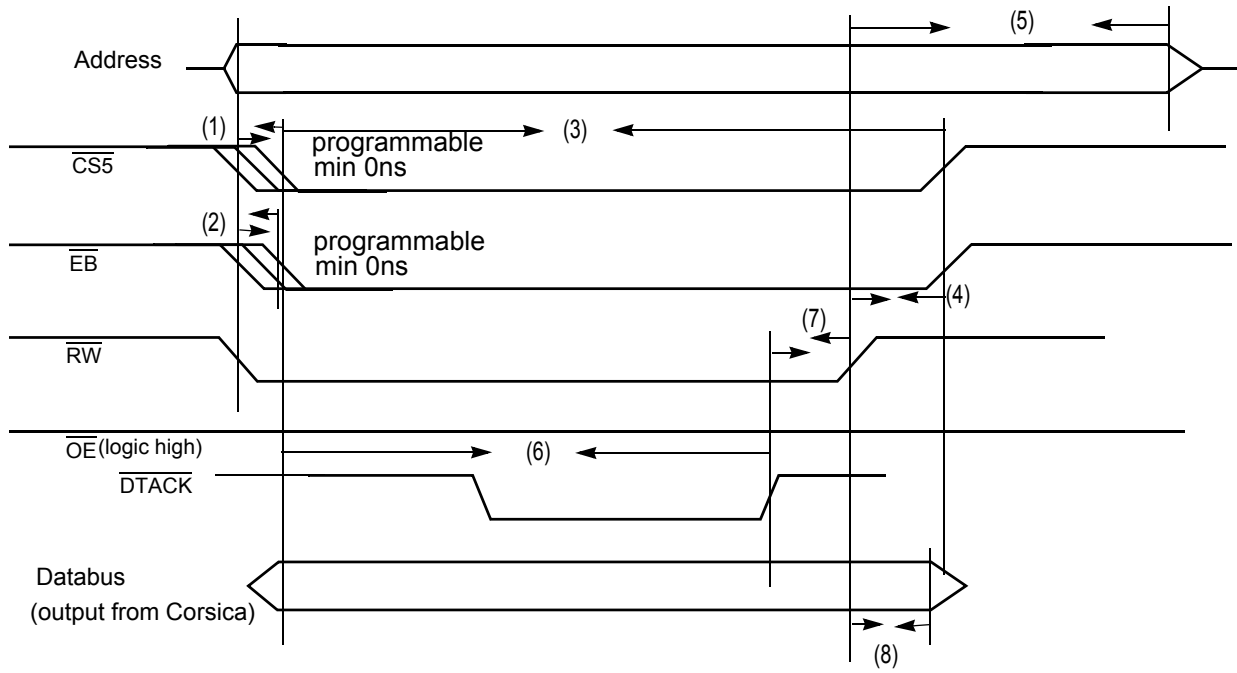


Figure 7.

Table 7. WSC = 111111, DTACK\_SEL=1, HCLK=96MHz, Write Cycle

Number	Characteristic	(3.0 ± 0.3) V		Unit
		Minimum	Maximum	
1	$\overline{CS5}$ assertion time	See note 2.	--	ns
2	$\overline{EB}$ assertion time	See note 2	--	ns
3	$\overline{CS5}$ pulse width	3T	--	ns
4	$\overline{RW}$ negated before $\overline{CS5}$ and $\overline{EB}$ is negated	20	--	ns
5	$\overline{RW}$ negated to Address inactive	50	--	ns
6	$\overline{DTACK}$ asserted after CS asserted		1022T	ns
7	$\overline{DTACK}$ asserted to $\overline{RW}$ negated	25		ns
8	data hold timing after $\overline{RW}$ negated	20		ns

**Note:**

1. T is the system clock period. (For 96MHz system clock)
2.  $\overline{CS5}$  assertion can be controlled by CSA bits.  $\overline{EB}$  also can be programmable by WEA bits in CS5L register.
3. Address becomes valid and  $\overline{RW}$  asserts at the start of write access cycle.
4. The external  $\overline{DTACK}$  input requirement is eliminated when CS5 is programmed to use internal wait state.

Freescale Semiconductor, Inc. ARCHIVED BY FREESCALE SEMICONDUCTOR, INC. 2005

ARCHIVED BY FREESCALE SEMICONDUCTOR, INC. 2005

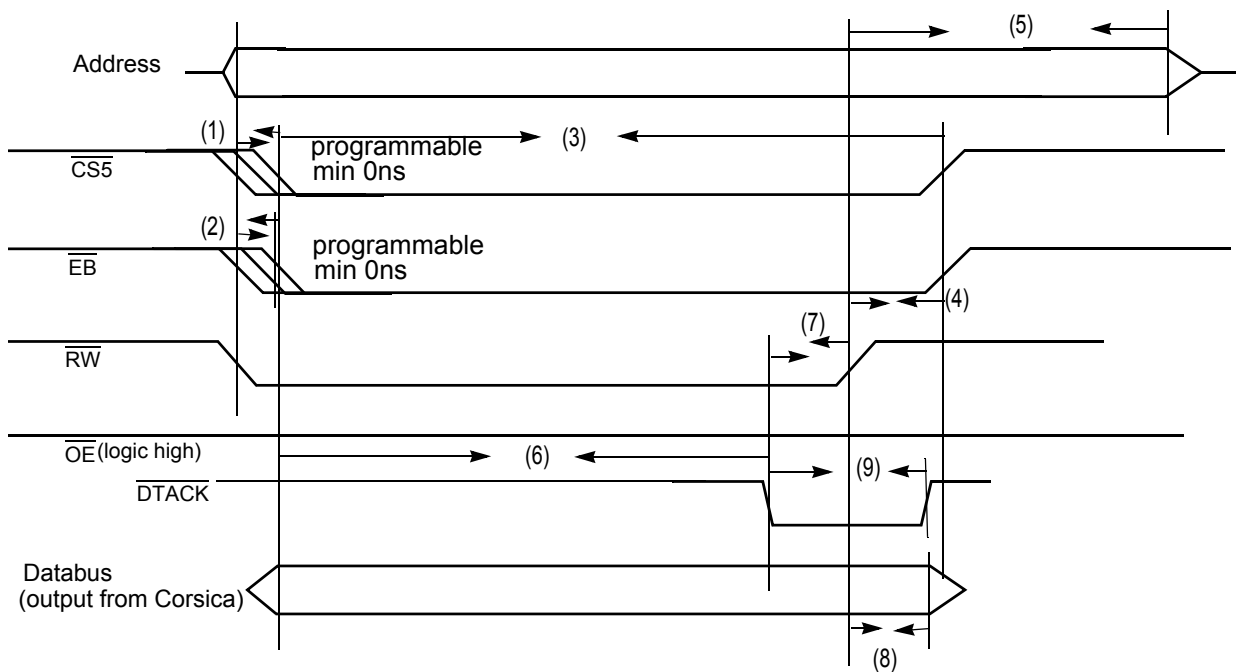


Figure 8.

Table 8. WSC = 111111, DTACK\_SEL=0, HCLK=96MHz, Write Cycle

Number	Characteristic	(3.0 ± 0.3) V		Unit
		Minimum	Maximum	
1	$\overline{CS5}$ assertion time	See note 2	--	ns
2	$\overline{EB}$ assertion time	See note 2	--	ns
3	$\overline{CS5}$ pulse width	3T	--	ns
4	$\overline{RW}$ negated before $\overline{CS5}$ and $\overline{EB}$ is negated	16	--	ns
5	$\overline{RW}$ negated to Address inactive	35	--	ns
6	$\overline{DTACK}$ asserted after CS asserted	5	1022T	ns
7	$\overline{DTACK}$ asserted to $\overline{RW}$ negated	25	--	ns
8	data hold timing after $\overline{RW}$ negated	20	--	ns
9	$\overline{DTACK}$ signal return to negation after asserted	1T	3T	ns

**Note:**

1. T is the system clock period. (For 96MHz system clock )
2.  $\overline{CS5}$  assertion can be controlled by CSA bits .  $\overline{EB}$  also can be programmable by WEA bits in CS5L register.
3. Address becomes valid and  $\overline{RW}$  asserts at the start of write access cycle.
4. The external DTACK input requirement is eliminated when CS5 is programmed to use internal wait state.



NOTES

**Freescale Semiconductor, Inc.**  
**ARCHIVED BY FREESCALE SEMICONDUCTOR, INC. 2005**

**ARCHIVED BY FREESCALE SEMICONDUCTOR, INC. 2005**

**HOW TO REACH US:**

**USA/EUROPE/LOCATIONS NOT LISTED:**

Motorola Literature Distribution  
P.O. Box 5405, Denver, Colorado 80217  
1-800-521-6274 or 480-768-2130

**JAPAN:**

Motorola Japan Ltd.; SPS, Technical Information Center,  
3-20-1, Minami-Azabu, Minato-ku, Tokyo 106-8573, Japan  
81-3-3440-3569

**ASIA/PACIFIC:**

Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre,  
2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T.,  
Hong Kong  
852-26668334

**HOME PAGE:**

<http://motorola.com/semiconductors>

Information in this document is provided solely to enable system and software implementers to use Motorola products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part.



Motorola and the Stylized M Logo are registered in the U.S. Patent and Trademark Office. All other product or service names are the property of their respective owners. ARM and the ARM POWERED logo are the registered trademarks of ARM Limited. ARM Developer Suite is the trademarks of ARM Limited. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.  
© Motorola, Inc. 2003

AN2422/D

Engineering Draft / Preliminary

**For More Information On This Product,  
Go to: [www.freescale.com](http://www.freescale.com)**