

APPLICATION NOTE

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**PCA8550 4-bit multiplexed/1-bit latched
5-bit I²C EEPROM**

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OVERVIEW

The PCA8550 enables single chip P6 (Pentium Pro or Pentium II) jumperless processor frequency configuration. This application note describes such configuration by presenting an outline, a block diagram, and a usage model of the PCA8550 in comparison with alternative solutions. Disadvantages of these alternatives are also addressed.

INTRODUCTION

As the block diagram in Figure 1 illustrates, the PCA8550 consists of eight stages which are conveniently grouped into one integrated circuit. These 8 stages are listed below.

The PCA8550's Eight Stages:

1. Nine internal pull-ups (10– 150 Ω) on the four pass-through inputs to avoid floats
2. I²C interface logic to communicate between the two I²C inputs and the 5-bit E²PROM
3. A 5-bit E²PROM to store the packets transferred through the I²C inputs SCL and SDA
4. Five AND gates to drive the E²PROM outputs (Q0 – Q4) low upon override
5. A 4-bit mux to select between E²PROM outputs (Q0–Q3) and the pass-through inputs
6. A 1-bit latch to retain the value of the 5th E²PROM output, NON_MUXED_OUT (Q4)
7. A 1-bit inverter to enable this latch upon request (of the MUX_SELECT pin)
8. A 4-bit buffer to convert the 3.3V CMOS multiplexer outputs into 2.5V outputs

As the block diagram in Figure 2 illustrates, alternatives to the PCA8550 are inferior with regards to real estate cost, component cost, utilization, functionality and reliability.

Disadvantages of Using Alternative Solutions to the PCA8550:

1. Real estate cost: required motherboard area triples due to 8 separate parts
2. Component cost: total price doubles due to non-integrated implementation
3. Utilization: jumpers are much less user-friendly than the E²PROM writable via the I²C
4. Reliability: mechanical systems will wear out while E²PROM is rated at 10,000+ cycles
5. Functionality: no latched output provided (e.g., the non-muxed-out, NMO)
6. Protection: no write protect or override to automatically clear jumpers provided

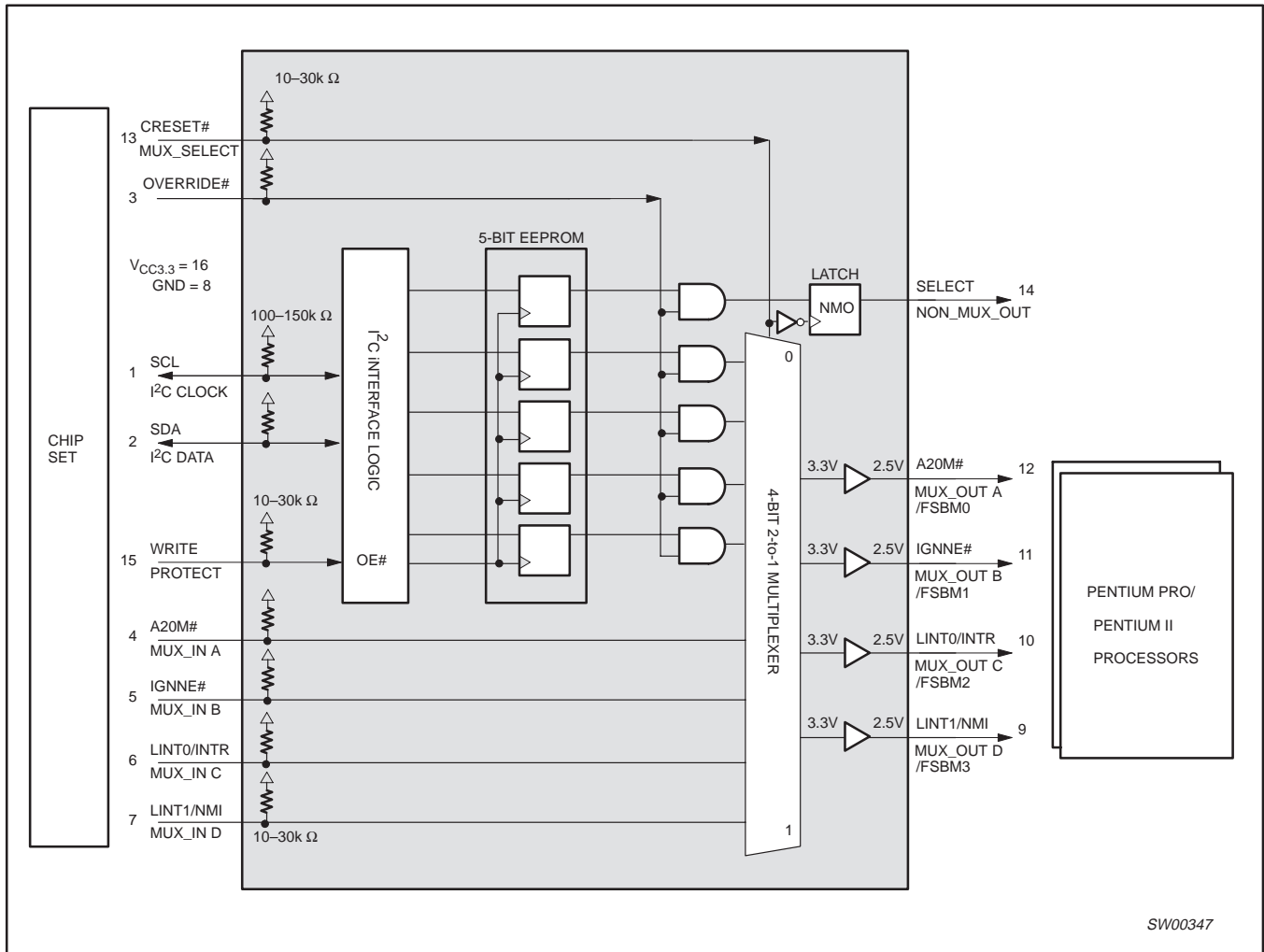
Alternatives to the PCA8550 vary but they all face the same limitations described above. One possible alternative includes the following stages.

The PCA8550 Alternative's Possible Stages:

- A four line jumper bank to retain four fixed values
- Four pull-ups (4.7 k Ω) on the jumper bank lines to assert logic high levels
- Four pull-ups (2.7 k Ω) on the pass-through inputs to avoid floats
- An 8-bit buffer (74LVC3244) to enable the jumper lines or the pass-through inputs
- A 6-bit buffer inverter to generate active high/low nibble enables for the 8-bit buffer (74HCT14)
- Two pull-ups (10 k Ω) on the two (inverted and non-inverted) nibble enables
- A 4-bit buffer to wire-AND the 8-bit buffer nibble outputs together (74F07)
- Four pull-ups (330 Ω) on the 4-bit buffer to drive the outputs to 2.5V levels

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Figure 1. The PCA8550 Block Diagram

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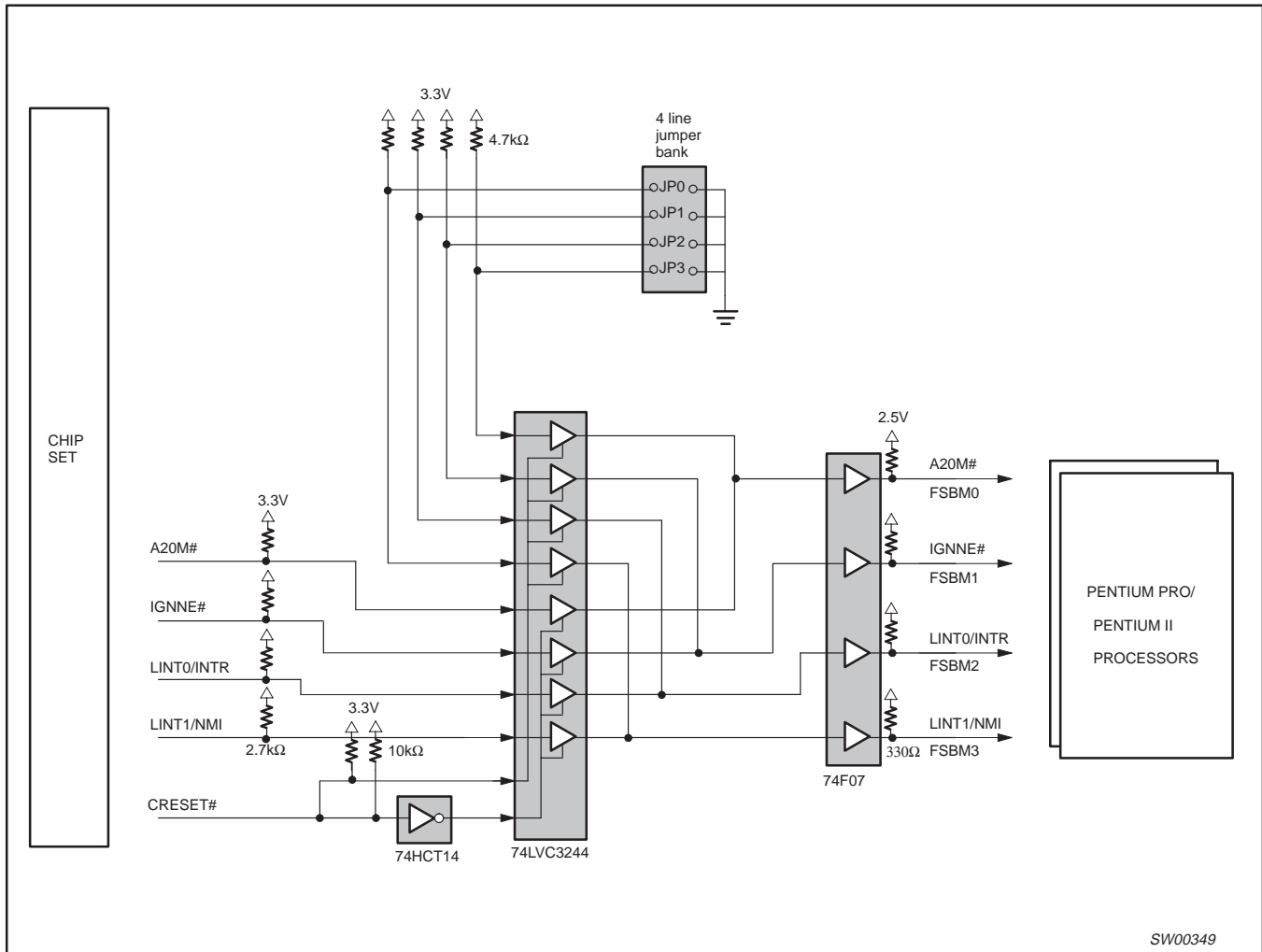


Figure 2. Block Diagram of A Possible Alternative to the PCA8550 (Alternatives to the PCA8550 are bulky and expensive)

GENERAL USAGE

The PCA8550 allows a P6 motherboard to run processors at different frequencies as follows. Each processor core (internal) frequency is a multiple of the front-side system bus (FSB) frequency. To logically represent this FSB multiple (FSBM) requires four pins (labeled pins 3:0 below) that were not defined in the original Pentium pinout.

Consequently, four processor pins should be multiplexed to double up in functionality depending on the state of reset. Intel has traditionally used the pins A20M#, IGNNE#, LINT0/NMI, and LINT1/INTR. Upon reset these four signals represent the FSBM (see Table 1). After reset these four signals default to their original functionalities (see Table 2).

Furthermore, P6 processors do not possess unique tags to identify their frequencies. As a result, OEMs/end users need to configure processor frequencies manually. The brute force method to do this is to use three glue logic parts (74HCT14, 74LVC3244, 74F07 and their corresponding pull-ups) and four jumpers that pull up/down the FSBM pins.

A cleaner, integrated solution implements the PCA8550's E²PROM to allow on the fly reprogrammability of the four FSBM pins using the I²C System Management Bus. The E²PROM moves the hassle of processor frequency configuration from hardware (jumper bank) to software (BIOS) simplifying production testing and end user upgrades.

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Table 1. Front-Side System Bus Multiple Function table

FSBM For	Pentium Pro/FSB	FSBM For	Pentium II/FSB	Pentium II/FSB	FSBM Pin 3	FSBM Pin 2	FSBM Pin 1	FSBM Pin 0
Pentium Pro	Frequencies (MHz)	Pentium II	Frequencies (MHz)	Frequencies (MHz)	(INTR/ LINT[1])	(NMI/ LINT[0])	(IGNNE#)	(A20M#)
2 (default)	133/66	2 (default)	133/66	200/100	0	0	0	0
3	200/66	3	200/66	300/100	0	0	1	0
4	266/66	4	266/66	400/100	0	0	0	1
Reserved		5	333/66	500/100	0	0	1	1
2½	166/66	2½	166/66	250/100	0	1	0	0
3½	233/66	3½	233/66	350/100	0	1	1	0
Reserved		4½	300/66	450/100	0	1	0	1
Reserved		5½	366/66	550/100	0	1	1	1
Reserved		6	400/66	600/100	1	0	0	0
Reserved		7	466/66	700/100	1	0	1	0
Reserved		8	533/66	800/100	1	0	0	1
Reserved		Reserved			1	0	1	1
Reserved		6½	433/66	650/100	1	1	0	0
Reserved		7½	500/66	750/100	1	1	1	0
Reserved		1½	100/66	150/100	1	1	0	1
2	133/66	2	133/66	200/100	1	1	1	1

Table 2. Processor Signals Multiplexed for Frequency Configuration

SIGNAL	DEFINITION	USAGE
INTR/ LINT[1]	Maskable interrupt when APIC disabled/ Local (processor) Interrupt 1 when APIC enabled	Advanced Programmable Interrupt Controller (APIC)
NMI/ LINT[0]	Non-Maskable Interrupt when APIC disabled/ Local (processor) Interrupt 0 when APIC enabled	Advanced Programmable Interrupt Controller (APIC)
IGNNE#	Ignore Numeric Non-Control Floating Point Error	8086 Compatibility
A20M#	Address 20 Wrap Around 1Mb Real Mode Boundary Mask	8086 Compatibility

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GENERAL IMPLEMENTATION

As the block diagram in Figure 3 illustrates, the BIOS initiates the transfer of the FSBM from the keyboard to the processor (listed below). The I/O controller, chipset, and PCA8550 serve as the bridges between these two devices as listed below. Note that the BIOS and I/O controller are ISA agents with an X-bus between them while the chipset and PCA8550 are I²C agents.

The FSBM transfer's 4 transactions:

1. The BIOS prompts the I/O controller for the FSBM during system setup via the X-bus
2. The I/O controller transfers these keyboard strokes to the chipset via the ISA-bus
3. The chipset transfers this data to the PCA8550 via the I²C system management bus
4. The PCA8550 stores this data and sends it to the processor upon reset (reboot)

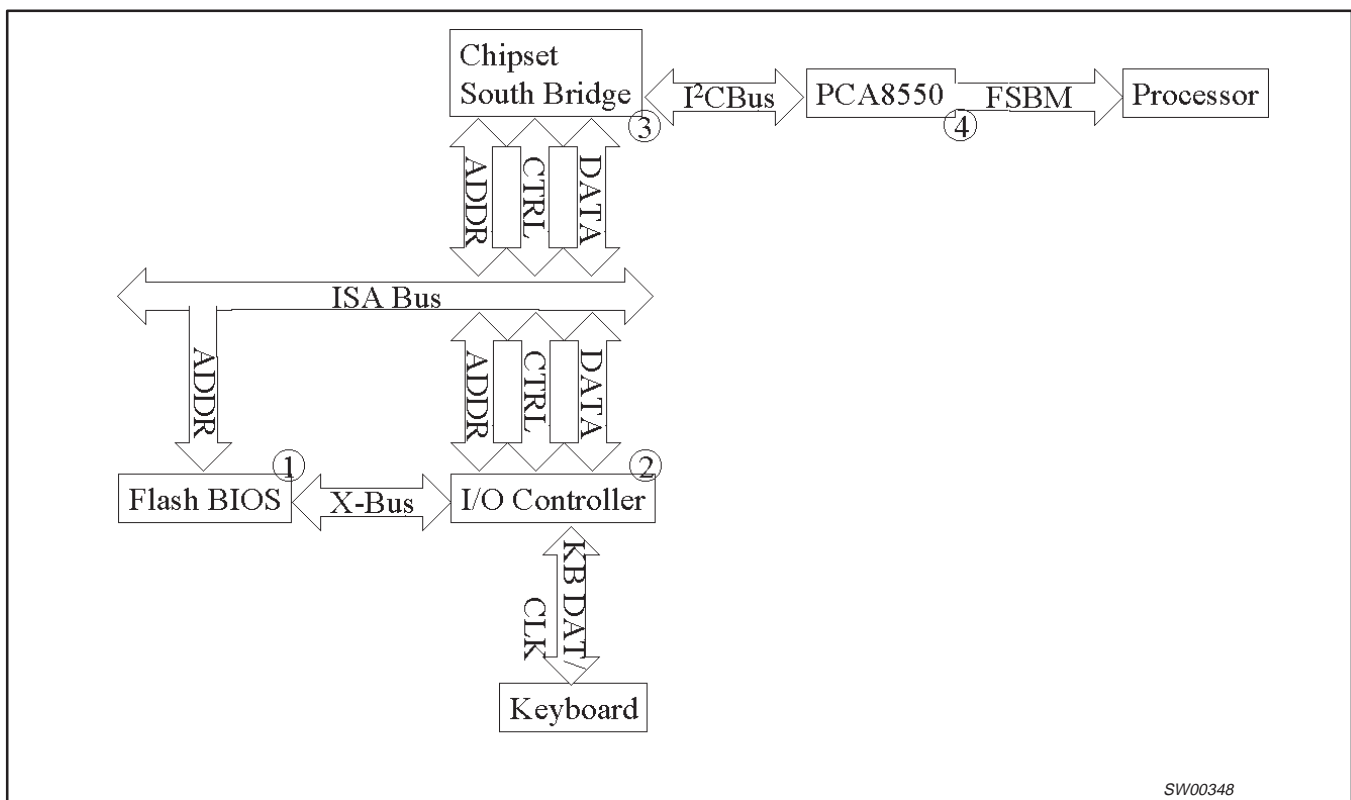


Figure 3. Transfer of the FSBM from the Keyboard to the Processor

Unlike the X-bus (8-bit data) and ISA bus (20-bit address, 16-bit data), the I²C bus is packet-based (7-bit address, 8-bit data). Philips developed this bi-directional 2-wire bus for efficient inter-IC (I²C) control. A serial clock (SCL) and active low serial data (SDA) make up this open drain serial interface that can run at 400kHz fast mode (100kHz standard).

Moreover, the two I²C pins, SCL and SDA, are Schmitt triggers with hysteresis to filter jitter between the high and low voltage ranges. They are not fixed in voltage level and can be wire-ANDed with other agents. To see how multiple agents interact during arbitration and synchronization, check out <http://www.semiconductors.philips.com/i2c>.

Figures 4 and 5 show transfers of the FSBM from the chipset to the PCA8550 and vice versa. The PCA8550's 7 bit address is binary 1001110 while its 8 bit data is binary 000xxxxx. The PCA8550's three most significant bits are always low while the remaining bits represent the 1 non-muxed-output (indicated in the figures as "n") and 4 FSBM pins.

The non-muxed-output (NMO) can be used as an output whose value is defined while the mux-select input is low (e.g. upon reset#) and fixed (latched) when the mux-select input goes high (reset# de-asserted). One application of the NMO could be a select bit that chooses between two known modes of an independent hardware vendor device.

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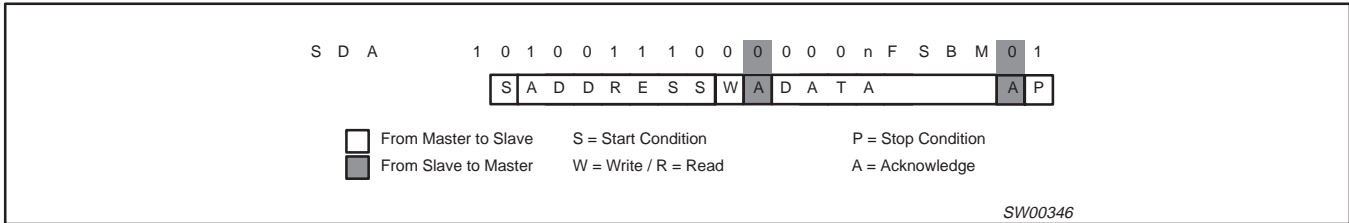


Figure 4. FSBM Write from Chipset to PCA8550



Figure 5. FSBM Read from PCA8550 to Chipset

CONCLUSION

The PCA8550 is a 4-bit 2-to-1 multiplexer with I²C E²PROM that enables jumperless P6 processor frequency configuration. Contact pc@sv.sc.philips.com for PCA 8550 technical support or check out <http://www.semiconductors.philips.com/logic> on the World Wide Web.

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Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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