Application Note

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MC9328MX1 Power Performance

Freescale Semiconductor, Inc.
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Contents

1 Power Performance of MC9328MX1

1.1 Power Modes

There are three different power modes supported by MC9328MX1 (MX1), they are: run, doze and stop. These modes, when combined with the easily configurable clocking system on-chip, provide developers with high flexibility to manage the power consumption of their target system to achieve maximum power efficiency. Figure 1 shows the MC9328MX1 system clocking scheme.

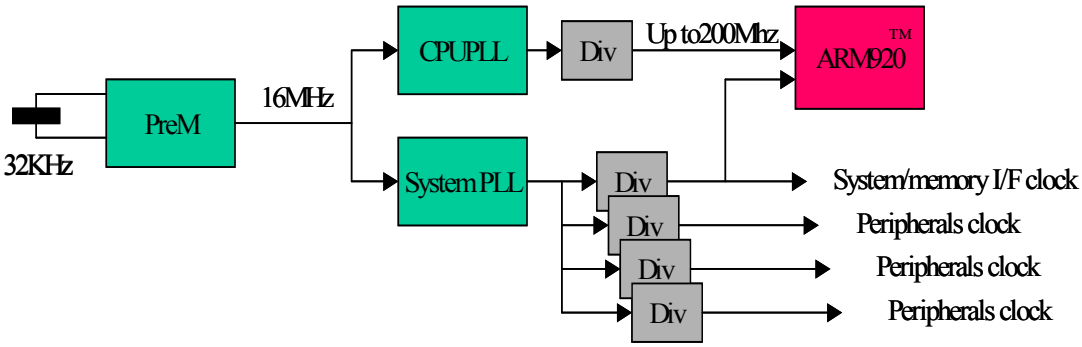

Figure 1. MC9328MX1 System Clocking Scheme

1.1.1 Run Mode

During Run mode, the MC9328MX1 core runs at full speed (up to 200 MHz).

Typical condition in PDA application:

Whenever there is one or more active tasks the PDA enters this mode to complete the tasks and return to other low power mode.

Clock configuration:

- CPU clock—async mode, max speed up to 200MHz. configurable.
- System and memory interface clock—max speed up to 96Mhz.
- Peripherals—Preset divider to provide lower clock per peripheral requirement.

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1.1.2 Doze Mode (Standby Mode)

During Doze mode, the MC9328MX1 core enters a low power state (WFI state), while all other system peripherals are keep running.

Typical condition in PDA application:

The system enters this mode whenever there is no active task pending.

Clock configuration:

- CPU clock—stopped. CPUPLL is also stopped.
- System and memory interface clock—Set to minimum frequency to keep other bus masters alive, such as LCD controller refreshes data from memory, DMA moving data between I/O and memory etc. For a QVGA system the system clock can be as low as 24MHz.
- Peripherals—Preset divider to provide lower clock per peripheral requirement. Clock rate does not change in doze mode, so the system enter/exit doze will not impact LCD or peripheral data rate.

1.1.3 Stop Mode (Sleep Mode)

In Stop mode, all clocks of MC9328MX1 are stopped (except the 32kHz clock) to achieve the lowest power consumption.

Typical condition in PDA application:

The system enters this mode when there is no active task for a preset number of seconds.

Clock configuration:

The system will do some housekeeping and then shut off both system and CPU PLLs. Only the 32KHz clock is running for Real Time Clock. Any interrupt event captured will wake the system automatically.

1.2 Doze Mode Operation

In doze mode, the CPU core of MC9328MX1 will stop execution and enter a low power state by executing a "wait for interrupt" instruction. It will stay in the low power state until an eligible interrupt wakes it up. The MCUPLL can be shut down during doze mode to provide further power saving. Example 1 on page 3 illustrates a typical sequence to enter doze mode.

The System PLL will continue to generate clock in doze mode to keep the required peripheral modules, such as the LCD controller, in operation. Additional power saving can be obtained during doze mode through lowering the system clock speed by setting the system clock divider (BCLKDIV) to a higher value. Adjusting the system clock will not affect the other peripherals such as UART or USB since they are driven by different clock paths.

As an example, a system might have its CPU running at 200MHz and its system clock at 96MHz while in run mode. When switched into doze mode, the CPU will stop execution and the system clock can be lowered to, say, 32MHz to minimize power consumption while maintaining the necessary operations (e.g. keeping the LCD on) in doze mode. The system clock is required to maintain the data throughput for refreshing the LCD display during doze mode. For LCD of smaller size or color depth, a lower system clock may suffice for maintaining the display.

When the system enters doze mode, the SDRAM controller by default will continue to operate as if it is in run mode. However, by programming the Clock Suspend Time-out (CLKST) bits of the SDRAM Control Register, the SDRAM can be put into clock suspend or power-down mode to provide further power saving. Please refer to the Chapter on SDRAM Memory Controller of the MC9328MX1 Reference Manual for the detailed description on the CLKST bits.

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Code Example 1. Doze Mode Example Sequence

```
;disable MCUPLL by clearing the MPEN bit
             mov r1, #0x0021B000
             mov r2, #0xFFFFFFFE
             ldr r3,[r1,#0x0]
             and r2,r2,r3
             str r2,[r1,#0x0]

;put CPU to "wait for interrupt" state
             mcr p15,0,r1,c7,c0,4
```

1.3 Stop Mode Operation

MC9328MX1 attains the lowest power consumption in stop mode with both the MCU PLL and the System PLL shut down. Only the 32kHz clock is running. The CPU core and all the peripheral modules except the Real Time Clock (RTC) module will be stopped to maximize the power saving.

The MCU PLL and the System PLL can be shut down by clearing the MPEN and UPEN bits of the Clock Source Control Register (CSCR). Upon clearing these bits, the MCU PLL will be shut down immediately. Whereas, there will be a delay before the System PLL is shut down. When the UPEN bit is cleared, the clock controller will invoke a shut down counter, which is configurable through the SD_CNT bits of CSCR. At the same time, it will inform the SDRAM controller that the system will be going into Stop Mode. The SDRAM controller will then start the self-refresh sequence once any in-progress SDRAM access has completed. After the SDRAM has safely entered self-refresh mode, the SDRAM controller will acknowledge the system clock controller that it is ready to enter Stop Mode. Only after receiving the acknowledgement and after the shut down counter times out will the clock controller shut down the System PLL. Example 2 illustrates a typical sequence to enter stop mode.

Code Example 2. Stop Mode Example Sequence

```
;disable both MCU and System PLLs by clearing MPEN & UPEN bits
             mov r1, #0x0021B000
             mov r2, #0xFFFFFFFC
             ldr r3,[r1,#0x0]
             and r2,r2,r3
             str r2,[r1,#0x0]

;MCU PLL will be shut down immediately while the System PLL will only
;shut down after the shut-down count times out (duration determined by
;shut-down Control (SD_CNT) setting of the Clock Source Control Register)

;put CPU to "wait for interrupt" state
             mcr p15,0,r1,c7,c0,4
```

2 Typical Power Performance

Some of the typical power consumption data of MC9328MX1 will be provided in this section. Please be aware that the data presented here is only typical data intended to provide developers with a feeling on the typical power consumption of MC9328MX1 under different operating conditions. Please refer to the Electrical Specification of MC9328MX1 for the guaranteed electrical characteristics of MC9328MX1.

Unless specified otherwise, the data presented below was obtained on the MC9328MX1 ADS board with NVDD, BTRFVDD and AVDD set to 3.0V and QVDD set to 1.8V. For the sake of simplicity, NVDD, BTRFVDD and AVDD are grouped together as "3V VDD" in the measurement. And "1.8V VDD" is equivalent to QVDD.

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2.1 Run Mode Power Consumption Data

Table 1. Run Mode with CPU in Fastbus Mode Using eSRAM

Measurement Conditions
• CPU core in fastbus mode (i.e. System clock = MCU clock = BCLK) • MCU PLL disabled; • System PLL = 96MHz; • PERCLK1 = PERCLK2 = 6MHz; • PERCLK3 = 750kHz; • All modules disabled except RTC and LCD controller; • Sharp 320x240 16-bit TFT panel with picture data stored in on-chip embedded SRAM (incomplete picture due to the size limit of eSRAM); • (refresh rate = 60Hz); • A Memory read/write program running on eSRAM;

System Clock	3V VDD (mA)	1.8V VDD (mA)	Power (mW)
16MHz	2.1	13.7	31.0
32MHz	2.1	23.4	48.4
48MHz	2.1	33.5	66.6
96MHz	2.1	62.7	119.2

Table 2. Run Mode with CPU in Fastbus Mode Using SDRAM

Measurement Conditions
• CPU core in fastbus mode (i.e. System clock = MCU clock = BCLK) • MCU PLL disabled; • System PLL = 96MHz; • PERCLK1 = PERCLK2 = 6MHz; • PERCLK3 = 750kHz; • All modules disabled except RTC, LCD controller and SDRAM controller; • Sharp 320x240 16-bit TFT panel with picture data stored in eSRAM • (refresh rate = 60Hz); • A Memory read/write program running on SDRAM;

System Clock	3V VDD (mA)	1.8V VDD (mA)	Power (mW)
16MHz	11	14	57
32MHz	14	29	95
48MHz	17	37	119
96MHz	30	66.0	209

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2.2 Doze Mode Power Consumption Data

Table 3. Doze Mode with LCD Displaying Data from Embedded SRAM

Measurement Conditions
• Sharp 320x240 16-bit TFT panel with picture data stored in on-chip • embedded SRAM (incomplete picture due to the size limit of eSRAM); • (refresh rate = 60Hz) • All modules disabled except RTC and LCD controller; • MCU PLL disabled; • System PLL = 96MHz; • PERCLK1 = 6MHz; • PERCLK2 = 16MHz; • PERCLK3 = 750kHz;

System Clock	3V VDD (mA)	1.8V VDD (mA)	Power (mW)
16MHz	1.9	10.9	25.3
32MHz	1.9	17.4	37.0
48MHz	1.9	23.5	48.0
96MHz	1.9	42.3	81.8

Table 4. Doze Mode with LCD Displaying Data from SDRAM

Measurement Conditions
• Sharp 320x240 16-bit TFT panel with picture data stored in SDRAM • (refresh rate = 60Hz) • All modules disabled except RTC, LCD controller & SDRAM controller; • MCU PLL disabled; • System PLL = 96MHz; • PERCLK1 = 6MHz; • PERCLK2 = 16MHz; • PERCLK3 = 750kHz;

System Clock	3V VDD (mA)	1.8V VDD (mA)	Power (mW)
16MHz	10.2	12.0	52.2
32MHz	12.8	19.0	72.6
48MHz	15.3	25.9	92.5
96MHz	20.2	46.5	144.3

2.3 Stop Mode Power Consumption Data

Table 5. Stop Mode (with No External Loading)

Measurement Conditions
• Measurement done on a special evaluation board with no memories and other external components. • MCU PLL and System PLL disabled; • All GPIO pins set to input with pull-up or pull-down resistors enabled. • 32kHz clock still running

3V VDD (mA)	1.8V VDD (mA)	Power (mW)
0.001	0.025	0.0480

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