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MC9S08AW60 and MC68HC908AZ60A MCUs Compared

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Introduction

This document compares the various modules of the MC9S08AW60 with equivalent modules of the MC68HC908AZ60A and is intended to be used as a guide in conjunction with the appropriate device data sheets. In the document, these devices are referred to as the 9S08AW60 and 908AZ60A, respectively.

It is structured (where possible) to align with the chapter section of the 9S08AW60 data sheet.

NOTE

With the exception of mask set errata documents, if any other Freescale document contains information that conflicts with the information in the device data sheet, the data sheet should be considered to have the most current and correct data.

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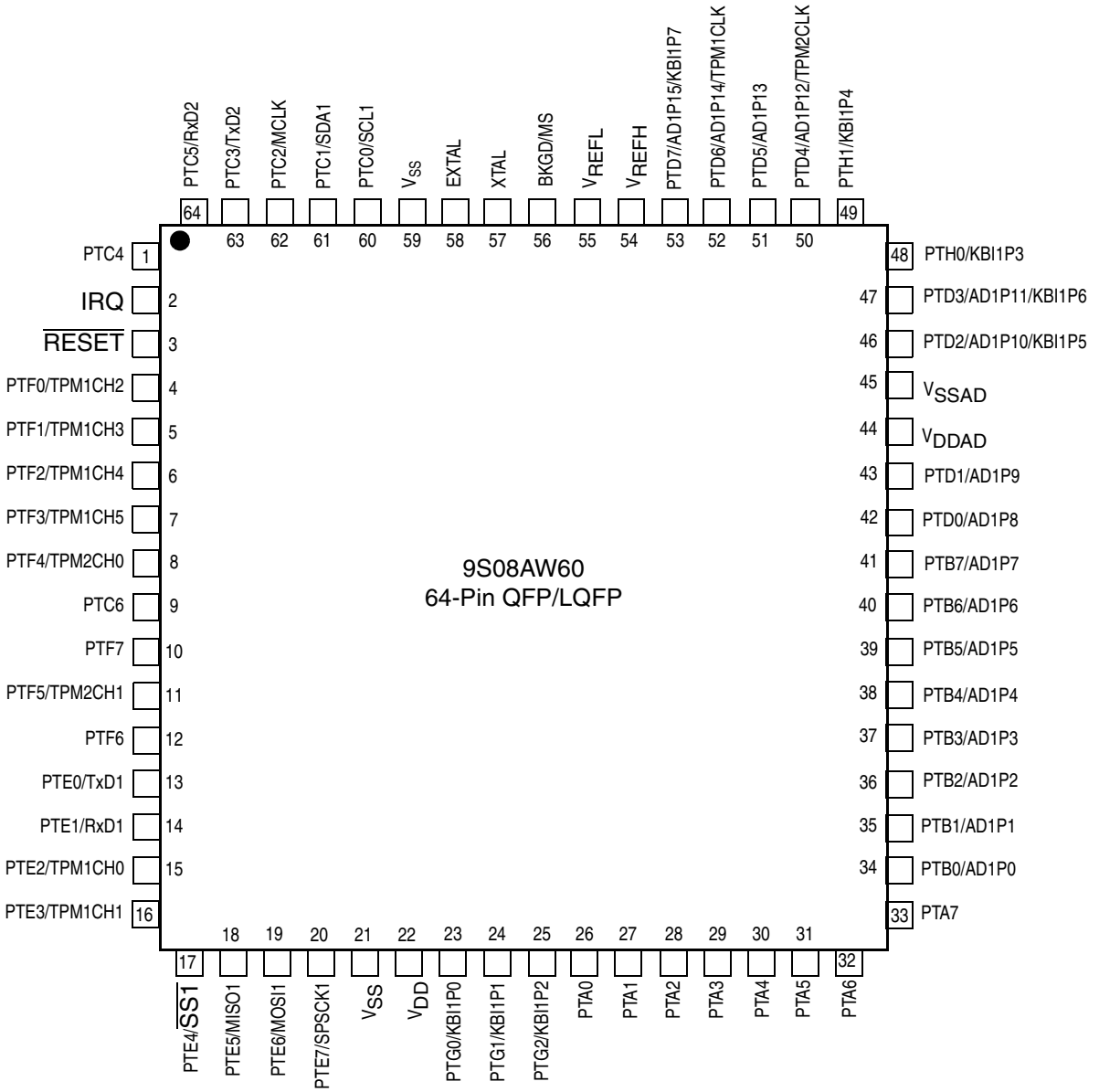
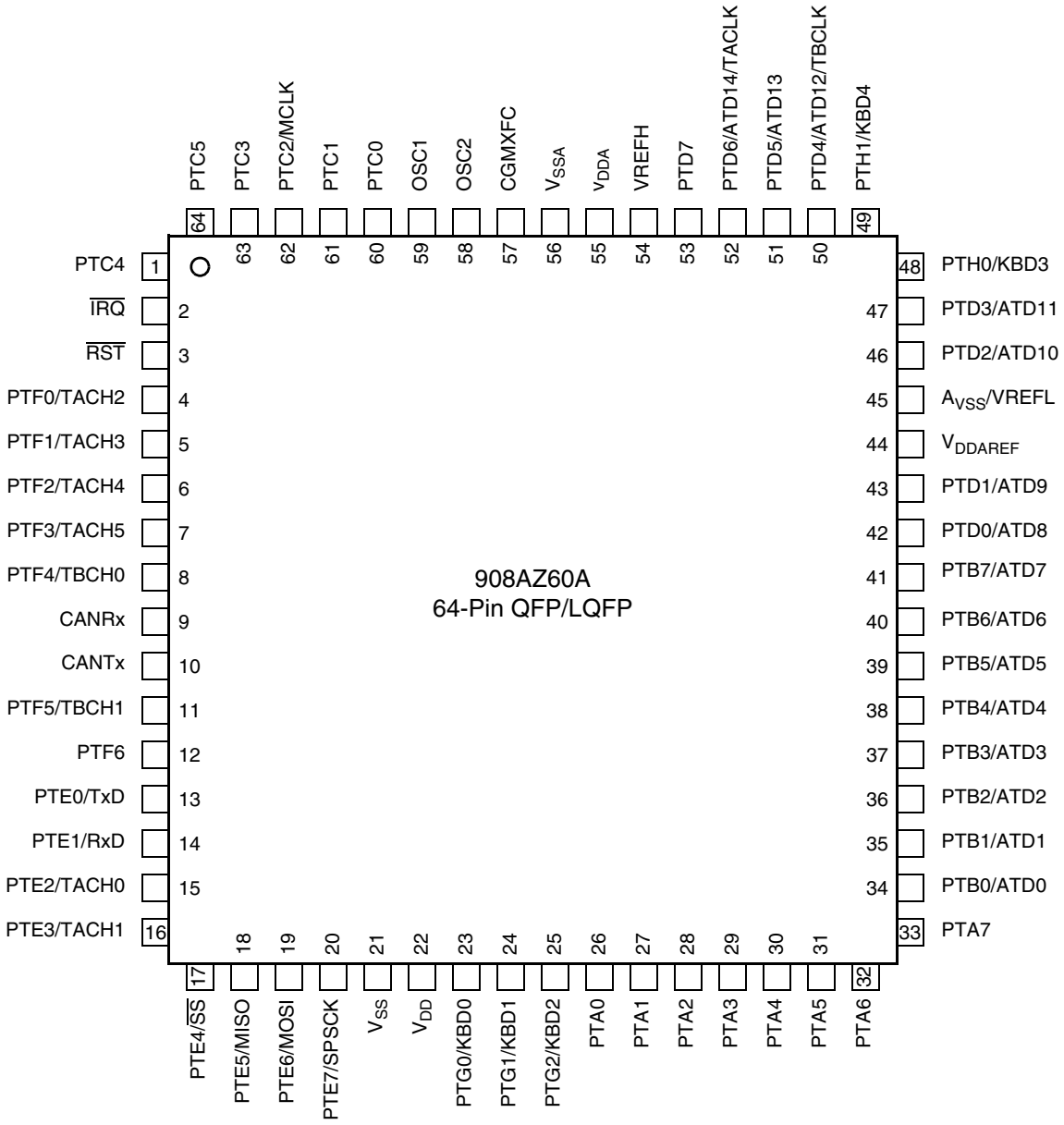
Pins and Connections

This section describes the signals that connect to the package pins. It covers the additional functionality that exists on the 9S08AW60 and differences between the pin assignments.

9S08AW60 Pin Assignment (64-Pin QFP)



908AZ60A Pin Assignment (64-Pin QFP)



Pin Compatibility

Table 1 illustrates the pin-for-pin compatibility of the 908AZ60A versus 9S08AW60. Differences in functionality have been shaded and are described in Additional Functionality on 9S08AW60.

Table 1. Pin Compatibility

Pin	908AZ60A	9S08AW60
1	PTC4	PTC4
2	$\overline{\text{IRQ}}$	IRQ
3	$\overline{\text{RST}}$	$\overline{\text{RESET}}$(1)
4	PTF0/TACH2	PTF0/TPM1CH2(1)
5	PTF1/TACH3	PTF1/TPM1CH3(1)
6	PTF2/TACH4	PTF2/TPM1CH4(1)
7	PTF3/TACH5	PTF3/TPM1CH5(1)
8	PTF4/TBCH0	PTF4/TPM2CH0(1)
9	CANRx	PTC6
10	CANTx	PTF7
11	PTF5/TBCH1	PTF5/TPM2CH1(1)
12	PTF6	PTF6
13	PTE0/TxD	PTE0/TxD1(1)
14	PTE1/RxD	PTE1/RxD1(1)
15	PTE2/TACH0	PTE2/TPM1CH0(1)
16	PTE3/TACH1	PTE3/TPM1CH1(1)
17	PTE4/$\overline{\text{SS}}$	PTE4/$\overline{\text{SS1}}$(1)
18	PTE5/MISO	PTE5/MISO1(1)
19	PTE6/MOSI	PTE6/MOSI1(1)
20	PTE7/SPSCK	PTE7/SPSCK1(1)
21	V_{SS}	V_{SS}
22	V_{DD}	V_{DD}
23	PTG0/KBD0	PTG0/KBIP0(1)
24	PTG1/KBD1	PTG1/KBIP1(1)
25	PTG2/KBD2	PTG2/KBIP2(1)
26	PTA0	PTA0
27	PTA1	PTA1
28	PTA2	PTA2

Table 1. Pin Compatibility (Continued)

Pin	908AZ60A	9S08AW60
29	PTA3	PTA3
30	PTA4	PTA4
31	PTA5	PTA5
32	PTA6	PTA6
33	PTA7	PTA7
34	PTB0/ATD0	PTB0/AD1P0(1)
35	PTB1/ATD1	PTB1/AD1P1(1)
36	PTB2/ATD2	PTB2/AD1P2(1)
37	PTB3/ATD3	PTB3/AD1P3(1)
38	PTB4/ATD4	PTB4/AD1P4(1)
39	PTB5/ATD5	PTB5/AD1P5(1)
40	PTB6/ATD6	PTB6/AD1P6(1)
41	PTB7/ATD7	PTB7/AD1P7(1)
42	PTD0/ATD8	PTD0/AD1P8(1)
43	PTD1/ATD9	PTD1/AD1P9(1)
44	V_{DDAREF}	V_{DDAD}(1)
45	AV_{SS}/V_{REFL}	V_{SSAD}(1)
46	PTD2/ATD10	PTD2/AD1P10/KBI1P5
47	PTD3/ATD11	PTD3/AD1P11/KBI1P6
48	PTH0/KBD3	PTH0/KBI1P3(1)
49	PTH1/KBD4	PTH1/KBI1P4(1)
50	PTD4/ATD12/TBCLK	PTD4/AD1P12/TPM2CLK(1)
51	PTD5/ATD13	PTD5/AD1P13(1)
52	PTD6/ATD14/TACLK	PTD6/AD1P14/TPM1CLK(1)
53	PTD7	PTD7/AD1P15/KBI1P7
54	V_{REFH}	V_{REFH}
55	V_{DDA}	V_{REFL}(2)
56	V_{SSA}	BKGD/MS(2)
57	CGMXFC	XTAL(2)

Table 1. Pin Compatibility (Continued)

Pin	908AZ60A	9S08AW60
58	OSC2	EXTAL[2]
59	OSC1	V_{SS}[2]
60	PTC0	PTC0/SCL1
61	PTC1	PTC1/SDA1
62	PTC2/MCLK	PTC2/MCLK
63	PTC3	PTC3/TxD2[1]
64	PTC5	PTC5/RxD2

NOTES:
1. The names of these pins have changed, but not their functionality.
2. The difference in functionality of these pins makes the 9S08AW60 not pin compatible with the 908AZ60A.

Additional Functionality on 9S08AW60

- Controller area network (CAN)
  - 9S08AW60 — does not feature a CAN module (CAN pins of the 908AZ60A have been replaced on the 9S08AW60 with extra I/O port pins)
  - 908AZ60A — does feature a CAN module

Table 2. CAN Pins Replaced with I/O Port Pins

Pin	AZ60A	AW60
9	CANRx	PTC6
10	CANTx	PTF7

- Port C
  - 9S08AW60 — 7-bit port (PTC6–PTC0)
  - 908AZ60A — 6-bit port (PTC5–PTC0)
- Port F
  - 9S08AW60 — 8-bit port (PTF7–PTF0)
  - 908AZ60A — 7-bit port (PTF6–PTF0)
- Keyboard interrupt module (KBI)
  - S908AW60 — 8-bit KBI
  - 908AZ60A — 5-bit KBI

Table 3. PTD Pins Multiplexed with Added KBD channels

Pin	AZ60A	AW60
46	PTD2/ATD10	PTD2/AD1P10/KBI1P5
47	PTD3/ATD11	PTD3/AD1P11/KBI1P6
53	PTD7	PTD7/AD1P15/KBI1P7

- Analog-to-digital converter (ATD)
  - S908AW60 — 16 channel, 10-bit ATD
  - 908AZ60A — 15 channel, 8-bit ATD

Table 4. PTD7 Pin, Multiplexed with Sixteenth ATD Channel

Pin	AZ60A	AW60
53	PTD7	PTD7/AD1P15/KBI1P7

- The 908AZ60A analog power supply VDDA has been replace with VREFL, the voltage reference low input for the ADC module on the 9S08AW60. The 908AZ60A analog ground pin has been replace with BKGD/MS, the background/mode select pin of the 9S08AW60.

Table 5. Power Supplies Replaced

Pin	AZ60A	AW60
55	V_{DDA}	V_{REFL}
56	V_{SSA}	BKGD/MS

- The 908AZ60A CGMXFC pin is replaced on the 9S08AW60 with an XTAL pin. This is because the 9S08AW60 has a different clock module from the 908AZ60A and pin 57 CGMXFC is no longer required as an output.

Table 6. Pin 57

Pin	AZ60A	AW60
57	CGMXFC	XTAL

- The 908AZ60A oscillator pins have changed function. This is because the 9S08AW60 has a different clock module from the 908AZ60A and a different pinout is required to accommodate the new oscillator pins.

Table 7. Oscillator Pins Renamed

Pin	AZ60A	AW60
58	OSC2	EXTAL
59	OSC1	V_{SS}

- The 9S08AW60 has an inter-IC bus (IIC). The IIC serial data line (SDL) and serial clock line (SCL) are shared with two port C pins.

Table 8. PTC Pins Multiplexed with IIC Module

Pin	AZ60A	AW60
60	PTC0	PTC0/SCL1
61	PTC1	PTC1/SDA1

- Serial communications interface (SCI)
  - 908AZ60A — one SCI
  - 9S08AW60 — two SCIs (second SCI shares its pins with port C)

Table 9. PTC Pins Multiplexed with the Second SCI

Pin	AZ60A	AW60
63	PTC3	PTC3/TxD2
64	PTC5	PTC5/RxD2

Modes of Operation

The 9S08AW60 features several new modes of operation, which are not available on HC08 Family MCUs. These include an extra stop mode and a background debug mode, which provides the means to monitor the MCU functionality during software development.

Stop Modes

On the 9S08AW60, the stop enable bit is located in the system options register (SOPT) instead of the configuration register (CONFIG1) of the 908AZ60A.

The user can determine which stop mode is entered by configuring bit PPDC in the system power management status and control 2 register (SPMSC2).

There is only one stop mode on the 908AZ60A; this is equivalent to stop3 mode on the 9S08AW60.

Table 10 summarizes the behavior of the 9S08AW60 in each of the stop modes.

Table 10. Summary of Stop Modes

MODE	SPMSC2 Bits		CPU, Digital Peripherals, FLASH	RAM	ICG	ATD	Regulator	I/O Pins	RTI
	PDC	PPDC							
Stop2	1	1	Off	Standby	Off	Standby	Standby	States held	Optionally on
Stop3	0	Don't care	Standby	Standby	Standby	Standby	Standby	States held	Optionally on

Background Debug Mode (BDM)

The active background mode functions are managed through the background debug controller (BDC) in the HCS08 core. The BDC, together with the on-chip debug module (DBG), provides the means for analyzing MCU operation during software development.

The 9S08AW60 BDM replaces monitor mode on the 908AZ60A. A comparison of the two modes can be found in application note AN2497/D: *HCS08 Background Debug Mode versus HC08 Monitor Mode*.

The BDC provides a single-wire debug interface to the 9S08AW60. This interface provides a convenient means for programming the on-chip FLASH and other nonvolatile memories.

The BDC, in conjunction with the on-chip debug module (DBG), provides the means for analyzing MCU operation and is the primary debug interface for software development. It allows non-intrusive access to memory data and traditional debug features such as CPU register modify, breakpoints, and single instruction trace commands.

In the HCS08 Family, address and data bus signals are not available on external pins. The debug module provides a means to selectively trigger and capture bus information so an external development system can reconstruct what happened inside the MCU on a cycle-by-cycle basis without having external access to the address and data signals.

A full description of BDM, the BDC, and the on-chip debug module is available in the 9S08AW60 data sheet, Freescale document *MC9S08AW60/D*.

Background Debug Mode Features

Features of the background debug mode include:

- Ability to analyze MCU functionality during software development
- Programming a bootloader or user software into FLASH
- Erasing and re-programming of FLASH after it has been previously programmed

Background Debug Controller (BDC) Features

A full description of the BDC is available in the development support section of the 9S08AW60 data sheet.

Features of the BDC include:

- Single dedicated pin for mode selection and background communications
- BDC registers not located in memory map
- SYNC command to determine target communications rate
- Non-intrusive commands for memory access
- Active background mode commands for CPU register access
- GO and TRACE1 commands
- BACKGROUND command can wake CPU from stop or wait modes
- One hardware address breakpoint built into BDC
- Oscillator runs in stop mode if BDM is enabled

Debug Module Features

A full description of the on-chip debug module is available in the development support chapter of the 9S08AW60 data sheet.

Features of the debug module (DBG) include:

- Two trigger comparators:
  - Two address and read/write (R/W)
    or
  - One full address and data and R/W
- Flexible 8-word by 16-bit FIFO (first-in, first-out) for capture information:
  - Change-of-flow addresses
    or
  - Event-only data
- Two types of breakpoints:
  - Tag breakpoints for instruction opcodes
  - Force breakpoints for any address access
- Nine trigger modes:
  - A only
  - A OR B
  - A then B
  - A AND B data (full mode)
  - A AND NOT B data (full mode)
  - Event-only B (store data)
  - A then event-only B (store data)
  - Inside range (A _ address _ B)
  - Outside range (address < A or address > B)

Memory

RAM

Both the 908AZ60A and the 9S08AW60 have 2K bytes of on-chip random access memory (RAM).

For compatibility with the 908AZ60A, HCS08 MCUs reset the stack pointer to $00FF.

When using the 9S08AW60, it is usually best to reinitialize the stack pointer to the top of the RAM so the direct page RAM can be used for frequently accessed RAM variables and bit-addressable program variables.

Include the following two-instruction sequence in the reset initialization routine (where RamLast is equated to the highest address of the RAM in the 9S08A60).

```
LDHX #RamLast+1 ;point one past RAM
TXS ;SP<-(H:X-1)
```

When the stack pointer is moved from its reset location at $00FF, direct addressing mode instructions can still access all page zero RAM locations efficiently.

The 9S08AW60 includes circuitry to prevent unauthorized access to the contents of RAM memory. For further detail please refer to the 9S08AW60 data sheet.

FLASH

A new FLASH technology has been implemented on the 9S08AW60. To simplify program and erase operations in the FLASH block, a command state machine has been introduced.

The 60K byte FLASH module is composed of 124 pages of 512 bytes. Each page is made up of eight rows of 64 bytes each. An erased byte reads $FF.

It is recommended that the appropriate sections of the 9S08AW60 data sheet be read and understood before attempting any code conversion.

9S08AW60 Versus 908AZ60A

- New register block in the 9S08AW60
- Single 60K byte block of FLASH versus two blocks of 32K bytes
- Command interface for fast, automated program and erase operations including blank check operation
- Byte programmable and sequential byte programmable compared to row programming only
- Page erase sector size 512 bytes compared to 128 bytes (bulk erase still available)

- FCLKDIV register used to supply the command state machine with a clock reference between 150 and 200 kHz, from the bus rate clock (this register must be written to before any program or erase command can be executed)
- Security feature to prevent unauthorized access to FLASH memory contents
- Status and error flags are available to the user and indicate when FLASH operations are complete

EEPROM

There is no EEPROM on the 9S08AW60, but this functionality can be easily emulated using a small portion of the FLASH memory. Examples of how this can be achieved may be found in the documentation listed in the References section.

Reset and Interrupts

For compatibility with the 908AZ60A, the 9S08AW60 has retained many of the basic reset and interrupt mechanisms. A result of maintaining the basic compatibility is that the H register is not automatically saved and restored during interrupt requests. It is good programming practice to push H onto the stack at the start of the interrupt service routine (ISR) and restore it just before the RTI instruction that is used to return from the ISR.

This section summarizes some of the features which have changed.

For a full description of the interrupt sources please refer to the relevant peripheral modules chapter of the 9S08AW60 data sheet.

9S08AW60 Versus 908AZ60A

- The 9S08AW60 has three new reset sources:
  - Stop2 wakeup
  - Serial command from a background debug host
  - Clock generator loss of lock and loss of clock
- The 9S08AW60 does not have an illegal address reset source (the 908AZ60A does)
- The 9S08AW60 low voltage detect circuit has extra functionality including:
  - LVD early warning flag
  - LVD interrupt
  - User-selectable thresholds
- The 9S08AW60 COP counter is cleared by writing to the system reset status register; writing to the high byte of the reset vector clears the 908AZ60A COP counter
- On the 9S08AW60, the COP counter is driven by the bus rate clock; the oscillator output clock, CGMXCLK, drives the COP counter on the 908AZ60A
- The 908AZ60A programmable interrupt timer (PIT) has been replaced on the 9S08AW60 with a real-time interrupt (RTI)

- On the 9S08AW60, the RTI counter can be driven by either the external clock source or a 1 kHz self-clocked time reference (the 908AZ60A PIT uses the internal bus clock only)
- The RTI can be configured to bring the 9S08AW60 out of wait or stop mode; the 908AZ60A PIT can bring the MCU only out of wait mode

Reset and Interrupt Vectors

Table 11 provides a comparison of the Reset and Interrupt vectors of the 9S08AW60 and the 908AZ60A.

Table 11. Comparison of Reset and Interrupt Vectors

		9S08AW60	908AZ60A
Lowest	$FFCC:FFCD	RTI	TIMA Channel 5
		IIC	TIMA Channel 4
	$FFD0:FFD1	ADC	ATD
	$FFD2:FFD3	Keyboard	Keyboard
	$FFD4:FFD5	SCI2 Transmit	SCI Transmit
	$FFD6:FFD7	SCI2 Receive	SCI Receive
	$FFD8:FFD9	SCI2 Error	SCI Error
	$FFDA:FFDB	SCI1 Transmit	CAN Transmit
	$FFDC:FFDD	SCI1 Receive	CAN Receive
	$FFDE:FFDF	SCI1 Error	CAN Error
	$FFE0:FFE1	SPI	CAN Wakeup
	$FFE2:FFE3	TPM2 Overflow	SPI Transmit
	$FFE4:FFE5	TPM2 Channel 1	SPI Receive
	$FFE6:FFE7	TPM2 Channel 0	TIMB Overflow
	$FFE8:FFE9	TPM1 Overflow	TIMB Channel 1
	$FFEA:FFEB	TPM1 Channel 5	TIMB Channel 0
	$FFEC:FFED	TPM1 Channel 4	TIMA Overflow
	$FFEE:FFEF	TPM1 Channel 3	TIMA Channel 3
	$FFF0:FFF1	TPM1 Channel 2	TIMA Channel 2
	$FFF2:FFF3	TPM1 Channel 1	TIMA Channel 1
	$FFF4:FFF5	TPM1 Channel 0	TIMA Channel 0
	$FFF6:FFF7	ICG	PIT
	$FFF8:FFF9	Low Voltage Detect	PLL
	$FFFA:FFFB	IRQ	IRQ
	$FFFC:FFFD	SWI	SWI
Highest	$FFFE:FFFF	RESET	RESET

Parallel Input/Output

The 9S08AW60 has an extremely flexible I/O structure providing a high level of multiplexed functionality on pins.

In addition to the standard data register and data direction register associated with each port, a pullup enable register and a slew rate control enable register has been added for each I/O port.

Summary of Additional Functionality on 9S08AW60

- Up to 54 general-purpose input/output (GPIO) pins
- All GPIO pins have input hysteresis input buffers to improve noise immunity
- Software selectable pullups on input port pins (selection is on an individual pin basis)
- Software selectable slew rate control on output port pins for improved EMI emission
- Software selectable output drive strength on all pins for improved EMI
- 10 mA sink/source capability on all ports

Central Processing Unit

Introduction

The HCS08 CPU executes all HC08 instructions, as well as a background (BGND) instruction and additional addressing modes on the LDHX, STHX, and CPHX instructions to improve compiler efficiency.

- Identical programmer's model
- Instruction queue (or pipeline) to improve instruction throughput
- All instructions implemented using the same mnemonics and opcodes
- Further detail can be found in HCS08RMV1/D: *HCS08 Family Reference Manual*

New Instructions/ Addressing Modes

LDHX	EXT, IX, IX2, IX1, SP1
CPHX	EXT, SP1
BGND	INH
STHX	EXT, SP1

Instructions with Cycle Count Reduced by 1

DIV	INH
DAA	INH
TAP	INH

CLI	INH
SEI	INH

Instructions with Cycle Count Reduced by 2

NSA	INH

Instructions with Cycle Count Increased by 1

NOTE

The increase in the HCS08 core speed compensates for the extra cycle required by these instructions.

BSETn	DIR
BCLRn	DIR
NEG	DIR, IX1, IX, SP1
COM	DIR, IX1, IX, SP1
LSR	DIR, IX1, IX, SP1
ROR	DIR, IX1, IX, SP1
ASR	DIR, IX1, IX, SP1
LSL	DIR, IX1, IX, SP1
ROL	DIR, IX1, IX, SP1
DEC	DIR, IX1, IX, SP1
INC	DIR, IX1, IX, SP1
TST	DIR, IX1, IX, SP1
DBNZA	INH
MOV	DD, DIX+, IMD, IX+D
CBEQ	IX+
CPHX	DIR
PULA	INH
PULX	INH
PULH	INH
BSR	REL
JSR	DIR, EXT, IX
JMP	EXT, IX
SUB	IX
CMP	IX
SBC	IX
CPX	IX
AND	IX
BIT	IX
LDA	IX
STA	IX
EOR	IX
ADC	IX
ORA	IX
ADD	IX
LDX	IX
STOP	INH
WAIT	INH

Instructions with Cycle Count Increased by 2

NOTE

The increase in the HCS08 core speed compensates for the extra cycles required by these instructions.

DBNZ	DIR, IX1, IX, SP1
CLR	IX1, IX, SP1
RTI	INH
RTS	INH
SWI	INH

Internal Clock Generator Module (ICG)

The ICG provides multiple options for clock sources. This offers a user great flexibility when balancing cost, precision, current draw, and performance. The module is intended to be user friendly with many of the features occurring automatically without user intervention.

The ICG module provides system clock generation and controls the oscillator, frequency-locked loop (FLL), real-time interrupt (RTI), and computer operating properly (COP) watchdog.

The ICG replaces the clock generator module (CGM) found on the 908AZ60A. Although they both provide similar functionality, the ICG should be considered a new module.

This section is intended to highlight the additional features of the 9S08AW60 ICG, but it is recommended that the appropriate sections of the 9S08AW60 data sheet be read and understood.

More information on initializing the ICG is available in application notes AN2494/D: *Configuring the System and Peripheral Clocks in the MC9S08GB/GT* and AN2496/D: *Calibrating the MC9S08GB/GT Internal Clock Generator*.

Summary of Additional Functions on 9S08AW60

Features of the ICG and clock distribution system:

- Several options for the primary clock source:
  - 32-kHz – 100-kHz crystal or resonator
  - 1-MHz – 16-MHz crystal or resonator
  - External clock
  - Internal reference generator
  - External oscillator selectable for low power or high gain
- Defaults to self-clocked mode to minimize startup delays
- Frequency-locked loop (FLL) generates 8 MHz to 40 MHz (for bus rates up to 20 MHz)
  - Uses external or internal clock as reference frequency
  - No external components required
- Automatic lockout of non-running clock sources

- Reset or interrupt on loss of clock or loss of FLL lock
- Digitally-controlled oscillator (DCO) preserves previous frequency settings, allowing fast frequency lock when recovering from stop mode
- DCO will maintain operating frequency during a loss or removal of the reference clock
- Post-FLL divider selects one of eight bus rate divisors (1 through 128)
- Separate self-clocked source for real-time interrupt
- Trimmable internal clock source supports SCI communications without additional external components
- Automatic FLL engagement after lock is acquired

Keyboard Interrupt Module (KBI)

The revised KBI of the 9S08AW60 offers increased functionality. This section compares the KBI of the 9S08AW60 with that of the 908AZ60A.

9S08AW60 Versus 908AZ60A

- The 9S08AW60 has eight keyboard interrupt pins instead of five
  - Four falling edge/low level sensitive
  - Four falling edge/low level or rising edge/high level sensitive
- Optional pullup (pulldown if rising edge/high level sensitive) on all pins
- Capable of waking the MCU from stop 2, stop 3, or wait modes

Timer/PWM Module (TPM)

Like the 908AZ60A, the 9S08AW60 has a 16-bit, 6-channel timer module and a 16-bit, 2-channel timer module.

The TPM replaces the timer interface module (TIM) found on the 908AZ60A. Although they both provide similar functionality, the TPM includes several new features and should be considered a new module.

This section is intended to highlight the additional features of the 9S08AW60 TPM, but it is recommended that the appropriate sections of the 9S08AW60 data sheet should be read and understood.

9S08AW60 Versus 908AZ60A

- The 9S08AW60 offers buffered PWM operation on all channels without the need to link two channels together as on the 908AZ60A, thus more PWM channels are available to the user
- The 9S08AW60 features center-aligned PWM operation which runs the 16-bit counter in up/down counting mode; the 908AZ60A does not have this function
- The 9S08AW60 has selectable polarity on PWM outputs (the 908AZ60A only offers positive polarity)

- Clock source choices
  - 9S08AW60 — three (bus clock, fixed system clock, or an external source).
  - 908AZ60A — two (internal bus clock or an external clock source)
- Maximum external clock frequency
  - 9S08AW60 — bus rate clock ÷ 4
  - 908AZ60A — either 4 MHz or bus frequency ÷ 2 (whichever is lower)
- Prescalers
  - 9S08AW60 — eight (1, 2, 4, 8, 16, 32, 64, 128)
  - 908AZ60A — seven (1, 2, 4, 8, 16, 32, 64)
- The 9S08AW60 and the 908AZ60A have two 16-bit timer modules with six channels and two channels, respectively
- The 9S08AW60 and the 908AZ60A have an interrupt for the main counter overflow plus an interrupt for each channel
- The 9S08AW60 and the 908AZ60A feature rising, falling, or any edge input capture
- The 9S08AW60 and the 908AZ60A offer set, clear, or toggle output compare
- The 9S08AW60 provides unbuffered output compare only; the 908AZ60A has unbuffered and buffered output compare (at the expense of linking two channels together)
- the 9S08AW60 does not feature a timer stop bit (TSTOP) or a timer reset bit (TRST); the 908AZ60A has both of these features

Serial Communications Interface (SCI)

Introduction

The 9S06AW60 has two identical SCI modules identified as SCI1 and SCI2, respectively. This section compares the SCI module of the 9S08AW60 with that of the 908AZ60A.

Summary of Additional Functions on 9S08AW60

- SCI clock source is the bus clock, compared to the crystal on the 908AZ60A
- Baud rate prescaler divisor and baud rate divisor are replaced with a 13-bit baud rate modulo divisor (BR). The SCI baud rate is given by:

$$\text{SCI baud rate} = \text{bus clock} \div (16 \times \text{BR})$$

- The baud rate generator is disabled if BR = 0
- Optional 13-bit or 14-bit break character for LIN system compatibility
- SCI stop in wait mode enable
- Control of the SCI power utilization in wait mode has been added. (If this function is enabled, all clocks to the module will be disabled and the module will be in its lowest power state.)
- Transmitter pin data direction in single-wire mode (transmitter pin direction is now controlled via the SCI module registers instead of the port control registers)

Serial Peripheral Interface (SPI)

The 9S08AW60 has a revised SPI module to improve efficiency and ease of use. This section compares the SPI module of the 9S08AW60 with that of the 908AZ60A.

9S08AW60 Versus 908AZ60A

- Single-wire bidirectional option
- Programmable transmit bit rate on the 9S08AW60, instead of only four baud rates on the 908AZ60A
- Selectable MSB-first or LSB-first shifting available on the 9S08AW60.
- SPI stop in wait mode enable
- Slave select output enable on the 9S08AW60 allows the $\overline{SS}$ pin to function as a general-purpose I/O in master mode
- On the 9S08AW60, the SPI receiver full interrupt and SPI transmitter empty interrupt share the same interrupt vector (the 908AZ60A uses two separate vectors)
- There is no overflow indicator on the 9S08AW60
- There is no programmable wired-or mode on the 9S08AW60

Inter-IC Bus (IIC)

This is a new module on the 9S08AW60 with no equivalent on the 908AZ60A. The inter-IC bus (IIC) is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange between devices. Being a two-wire device, the IIC bus minimizes the need for large numbers of connections between devices and eliminates the need for an address decoder.

The interface is designed to operate up to 100 kbps with maximum bus loading and timing. The device is capable of operating at higher baud rates, up to a maximum of clock/20, with reduced bus loading. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF.

For a full description of the inter-IC bus, please refer to the relevant chapter of the 9S08AW60 data sheet.

Analog-to-Digital Convertor (ATD)

The 9S08AW60 ATD module has a 16-channel, 10-bit, multiplexed input, successive approximation analog to digital converter. The ATD module has been enhanced to provide increased accuracy, faster conversion rates, higher maximum ATD clock frequencies, and extra functionality. Further details on the ATD module are available in the 9S08AW60 data sheet.

This section compares the ATD module of the 9S08AW60 with that of the 908AZ60A.

Summary of Additional Functionality on 9S08AW60

- 16 channels with multiplexed input
- 10-bit or 8-bit resolution (the ATD has 10-bit accuracy, but 8-bit is selectable if compatibility is required)
- Increased maximum ATD clock frequency of 8 MHz versus 1 MHz on 908AZ60A
- 3.2 μs, 10-bit single conversion time at a conversion frequency of 8 MHz, 16 MHz bus frequency vs 16.0 μs, 8-bit single conversion time at a conversion frequency of 1 MHz on the 908AZ60A
- Input CLK selectable from up to four sources: BUSCLK, BUSCLK/2; ALTCLK, ASYNC CLK
- Selectable asynchronous hardware conversion trigger
- Four selectable input clock sources including an asynchronous clock source for lower noise operation
- Operation in stop3 mode for lower noise performance
- Automatic compare with interrupt for comparison against a programmable value
- Power down mode — the ADCH bits offer a module disable feature, reducing power consumption when the ATD is not being used
- ATD pin control registers have been added to configure pins for ATD usage

References

AN2183/D: *Using FLASH as EEPROM on the MC68HC908GP33*

AN2346/D: *EEPROM Emulation Using FLASH in MC68HC908QY/QT MCUs*

AN2302/D: *EEPROM Emulation for the MC9S12C32*

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