Freescale Semiconductor
Application Note

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MPC8260 PowerQUICC™ II Family Power Distribution Trends: A Survey

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This application note surveys power distribution circuits that deliver sufficient quiet supply to the MPC8260 PowerQUICC™ II family of integrated communications processors. It highlights issues that arise with systems based on a high performance processor such as the MPC8260. This document is intended as a guideline for new designs as well as a reference for debugging existing designs. The MPC8260 PowerQUICC II family consists of the devices shown in Table 1.

Contents

Table 1. MPC8260 Family Devices and Silicon Revisions

Device	Silicon							
Process	0.29 µm (HiP3)					0.25 µm (HiP4)		
Revision	A.1	B.1	B.2	B.3	C.2	A.0	B.1	C.0
MPC8260(A) [1]	÷	÷	÷	÷	÷	÷	÷	
MPC8250 [2]						÷	÷[2]	÷[2]
MPC8255(A)[1]	÷	÷	÷	÷	÷	÷	÷	
MPC8264						÷	÷	
MPC8265						÷	÷	÷
MPC8266						÷	÷	÷

[1] “A” designates HiP4 revisions of a device that was originally available in a HiP3 version.
[2] Also available in 516 PBGA (VR or ZQ) package in HiP4 Rev B.1 and Rev C.0 only.

1 Power Distribution Strategy

One important step in designing a high speed digital system is to plan the power distribution strategy, which should include the following:

- Power supply circuit design
- Power supply delivery network
- IC decoupling networks
- Noise and EMI issues

For the power supply circuit, designers should plan for an efficient supply that can provide the following:

- Accurate output voltage levels at different loads
- Protection to the load from the main conducted emissions and surges
- Protection to the load from shorts and surges
- Stability under various overall supply network, i.e., no oscillations, minimum drift, and so on
- Enough bypass circuit for sudden demand from the load
- Capability to sense loads when the loads are remote from the supply
- Isolation of the main from the load
- Fast dynamic response to load changes to stay within limit of the specified output levels

This document does not discuss power supply circuit design. The main assumption is that the supply circuit is a nearly ideal DC source. This assumption simplifies the analysis by de-correlating supply circuit dynamics from the network dynamics. Instead, our focus is the supply delivery network and use of capacitors to bypass the supply network. Designers must plan for placement of this circuit relative to the loads. It is generally preferable to have the supply circuit closer to the load. When that is difficult, a power delivery circuit is needed to reach far loads. The study of delivery network characteristics and interaction with the processor load, for instance, is vital to understand and to design a minimum noise delivery system. To see the whole picture of our power network, we must include most of the parasitics in the power distribution network as well as in the load chip packages. In addition, we should include all the bypass caps in the model. Figure 1 shows the power circuit of a single-chip load.

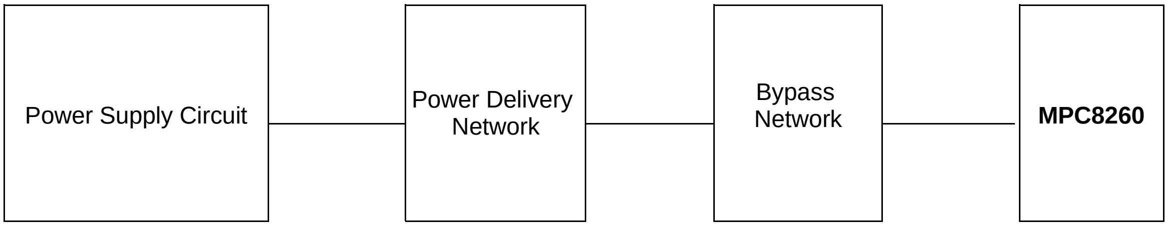


Figure 1. Power Circuit

2 Statement of the Problem

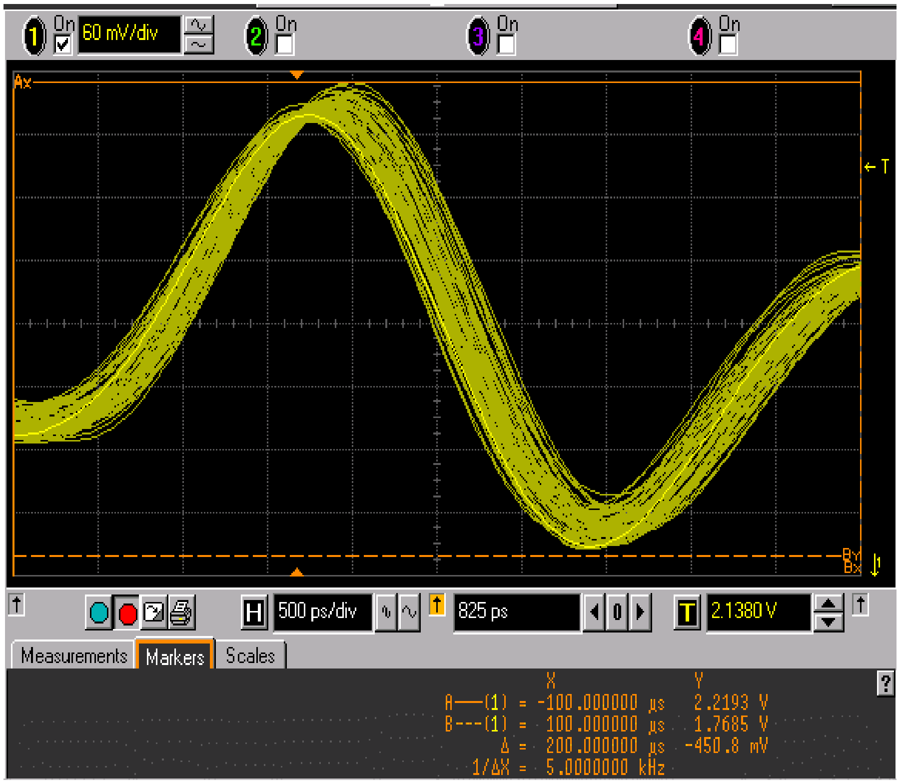
From the perspective of the decoupling capacitor, the problem is that the following characteristics of the bypass capacitor are not known:

- Capacitor count
- Type
- Location
- Orientation
- Connection to load

Also, the following characteristics of the power delivery network are unknown:

- The optimal topology of the supply and ground layers, given a set of physical constraints.
- The nature of the interaction of this network with the load package.
- How to minimize the noise and EMI while meeting the power demand requirement.

This document addresses these topics. Figure 2 shows a scope capture of MPC8260 power input from a non-optimized system.



```
                    X                Y
A——(1) = -100.000000 µs   2.2193 V
B---(1) =  100.000000 µs   1.7685 V
     Δ =  200.000000 µs  -450.8 mV
  1/ΔX =  5.0000000 kHz
```

Figure 2. MPC8260 Power Input from a Non-optimized Source

The MPC8260 supply power dropped to below 1.9 V. The measurement is taken as close to the MPC8260 pin as possible. We can conclude that early planning is important for the distribution network as well as bypass capacitor network.

3 Previous Work

Because the design challenge is a circuit optimization problem, we must address it in a way that covers most of the characteristics set forth in Section 2, “Statement of the Problem.” We must consider how to perform the following tasks:

- Estimate the load
- Model the load
- Model the BCP delivery network
- Optimize the response with non-ideal caps
- Incorporate EMI reduction to our effort

In approaching these tasks, we need to summarize what others have achieved so far.

3.1 How to Estimate Bypass Capacitors

Different systems consume different amounts of power even if they use the same processor. For many reasons, it may be difficult to predict the amount of power a new system will consume. It is hard to have a clear idea of the complexity of the user software in the early stages of the project. For example, [11] (see

Section 4, “References”) describes a project that correlates measurements of system processor power consumption with periodic events estimating system usage and performance monitors. Other similar techniques are used to produce an energy-aware computing system. Modern superscaler processors such as the MPC8260 603e core perform computations with many units running in parallel. Thus, the amount of power consumed by the processor is directly related to the sequence of code that is fed to it. Although there are simulation techniques to estimate the power that processes consume, these simulation-estimation efforts are still tied to the sequence of instructions fed to the simulator. This may be why the project reported in [11] directly measures the power consumption rather than simulating the micro-architectural detailed power consumption. What matters is the ability to predict the code and estimate how much the processor is used in the following ways:

- Data cache hit/miss ratio
- Instruction cache hit/miss ratio
- Register file usage
- Branch prediction unit events
- Integer/floating unit

We can assume worst-case power consumption when the processor runs at its extreme power limit as well. However, this approach has shortcomings, such as the following:

- Too much expected current demand means undesirably stronger power supply circuit.
- Too much expected current allows adding more generous copper estate, which is expensive.

As in any engineering challenge, there has to be a reasonable compromise and an educated guess. For example, in the MPC8260 core current demand estimation we must first know the speed at which the core operates. Then we can consider the case when the process starts a heavy load execution. We must estimate the number of core clock cycles needed to draw that much current and stay there steadily. The following sets of equations are useful:

- Core frequency = F in Hertz.
- Core single clock cycle time = 1/f in seconds.
- N is the number of cycles needed to fill keep the processes working hard
- I is current in Amps consumed when the processor is working hard

Therefore, the rate of current change can be stated as follows:

$$\frac{dI}{dt} = \frac{I \times F}{N} \qquad \textit{Eqn. 1}$$

In our example, if the MPC8260 runs at 2.0 V, I is estimated 1.2 A, F = 200MH, and N = 2, then:

$$\frac{\Delta I}{\Delta t} = \frac{1.2 \times 200e6}{2} = 1.2e8 \qquad \textit{Eqn. 2}$$

This excessive amount of current change definitely creates a huge stress on the power delivery network, especially if it is not properly designed.

So far we have seen some description of load current consumption and have had a rough estimation of its rate of change. Imagine the current demand curve as it is shown in Figure 3.

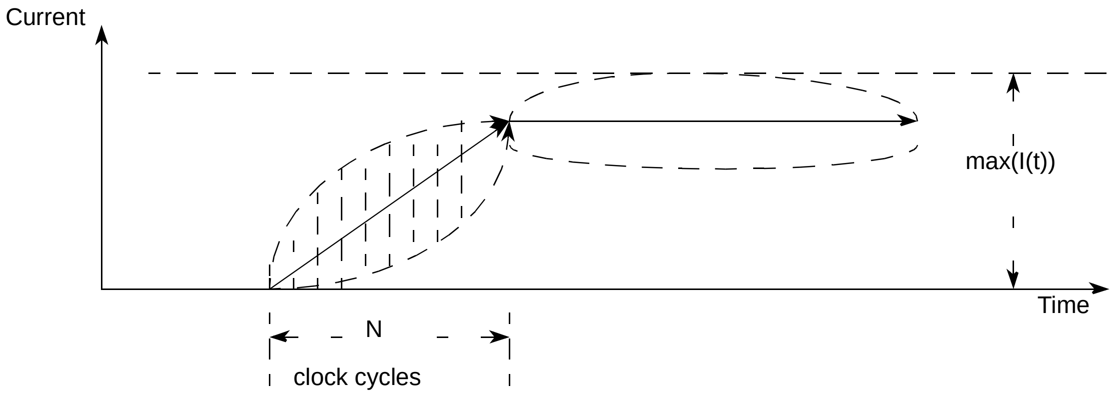


Figure 3. Current Demand Curve

Note that the current exact profile depends on the code. If I(t) is the exact current profile, we assume the following:

$$\left|\frac{\mathbf{dI(t)}}{\mathbf{dt}}\right| \leq \frac{\mathbf{max(I(t)) \times F}}{\mathbf{N}} \qquad \textbf{Eqn. 3}$$

The first technique to roughly estimate the bypass capacitors is based on the following set of equations:

$$\mathrm{Xmax} = \frac{\Delta V}{\Delta I} \qquad \textbf{Eqn. 4}$$

$$\mathrm{Fpsw} = \frac{\mathrm{Xmax}}{2\pi \mathrm{Lpsw}} \qquad \textbf{Eqn. 5}$$

$$\mathrm{Cbypass} = \frac{1}{2\pi \mathrm{FpswXmax}} \qquad \textbf{Eqn. 6}$$

In this case:

$$\Delta V = \mathrm{VCC} \times \mathrm{tolerance} \qquad \textbf{Eqn. 7}$$

Based on our example, if Vcc = 2.0V and tolerance is 5% (also the current assumed is 1.2A), it could be stated as follows:

$$\Delta V = 2.0 \times 0.05 = 100\mathrm{mV} \qquad \textbf{Eqn. 8}$$

The Xmax that is maximum common path impedance we can tolerate at the consumed current is the following:

$$\mathrm{Xmax} = \frac{100\mathrm{mV}}{1.2} = 83\mathrm{m}\Omega \qquad \textbf{Eqn. 9}$$

As shown in the following equation, Fpsw is the frequency below which the power supply wiring is adequate, and Lpsw is the power supply wiring inductance. The supply inductance value is a function of the power track’s geometry. Assume a system with 100nH:

$$\mathrm{Fpsw} = \frac{\mathrm{Xmax}}{2\pi \mathrm{Lpsw}} = \frac{0.083}{2\pi \times 100\mathrm{n}} = 132165 \cong 132\mathrm{kH}$$ **Eqn. 10**

Thus, the bypass first bypass capacitor to add is the following:

$$\mathrm{Cbypass} = \frac{1}{2\pi \mathrm{FpswXmax}} = \frac{1}{2\pi \times 0.083 \times 132\mathrm{k}} = 14.5\mathrm{uF}$$ **Eqn. 11**

Because bypass capacitors have inductance in series, we must estimate a frequency Fbypass after which this bypass capacitor is not adequate. In the following equation, *L* is the series inductance of the bypass capacitor.

$$\mathrm{Fbypass} = \frac{\mathrm{Xmax}}{2\pi \mathrm{L}}$$ **Eqn. 12**

Now, let L = 5nH.

$$\mathrm{Fbypass} = \frac{\mathrm{Xmax}}{2\pi \mathrm{L}} = \frac{0.083}{2\pi \times 5\mathrm{nH}} = 2643312 \cong 2.6\mathrm{Mhz}$$ **Eqn. 13**

This result tells us that the 14.5pF capacitor is adequate from 132 KH to 2.6 MH.

The next step is to add more capacitors to take care of the higher frequency range. In this analysis, the frequency that is proportional to a digital signal rise time frequency is called Fknee, and is defined as the following:

$$\mathrm{Fknee} = \frac{1}{2\mathrm{Trise}}$$ **Eqn. 14**

In our case, let Trise be as follows:

$$\mathrm{Trise} = \frac{2}{200\mathrm{M}} = 0.01\mu\mathrm{s}$$ **Eqn. 15**

Therefore:

$$\mathrm{Fknee} = \frac{1}{2\mathrm{Trise}} = \frac{200\mathrm{M}}{2 \times 2} = 50\mathrm{Mhz}$$ **Eqn. 16**

If we want to add *m* small capacitors with *L* inherent inductance per each, then:

$$\frac{\mathrm{L}}{\mathrm{m}} = \frac{\mathrm{Xmax}}{2\pi \mathrm{Fknee}} = \frac{0.083}{2 \times \pi \times 50\mathrm{M}} = 0.2643\mathrm{nH}$$ **Eqn. 17**

If we use a standard SMT capacitor, the series L is around 2nH, which means we need m as follows:

$$\mathrm{m} = \frac{2\mathrm{nH}}{0.2643\mathrm{nH}} \approx 7.4 \approx 8$$ **Eqn. 18**

This result tells us that we need at least eight capacitors to maintain an adequate bypass till 50MH. Now it is necessary to calculate the capacitance of each of these eight capacitors.

$$\mathrm{C} = \frac{1}{2 \times \pi \times \mathrm{m} \times \mathrm{Xmax} \times \mathrm{Fbypass}} = \frac{1}{2\pi \times 8 \times 0.083 \times 2.6\mathrm{e}6} = 0.922\mathrm{nF}$$ **Eqn. 19**

Also note that the power supply delivery plane has the following capacitance (where *A* is the area and *d* is the separation height all in inches):

$$C_{powersupply} = \frac{0.225\varepsilon rA}{d} \qquad \textbf{Eqn. 20}$$

Let us say Cpower plane = 300pF. The overall circuit model resembles Figure 4.

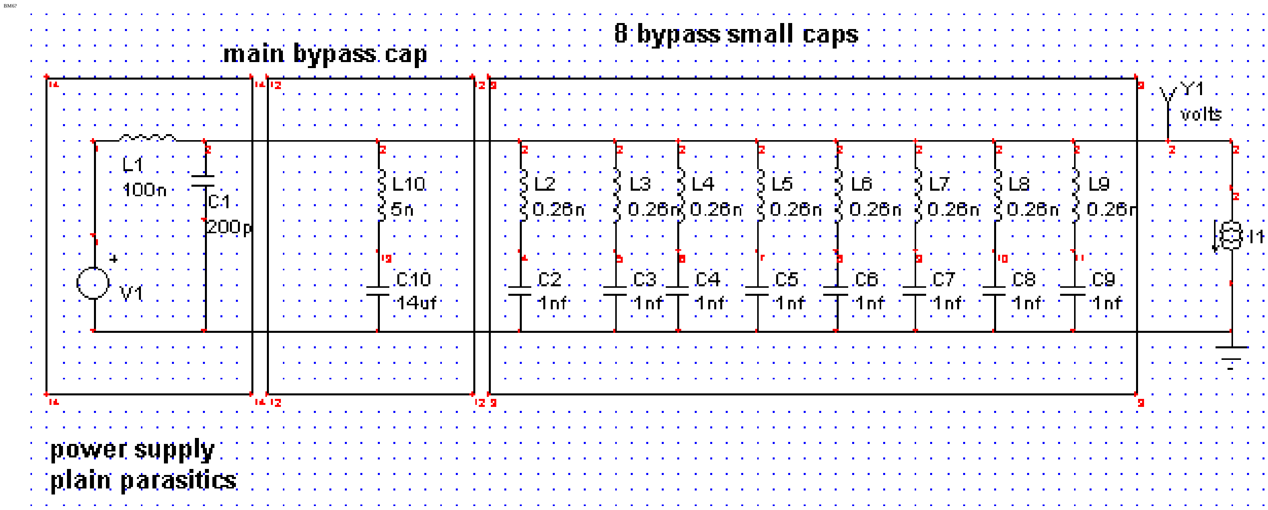


Figure 4. Circuit Model

Using a Intusoft simulator, the following (Figure 5) is the voltage measurement as we sweep the AC current source frequency. Note that the AC amplitude is 1Amp, which makes the curve an impedance reading as well.

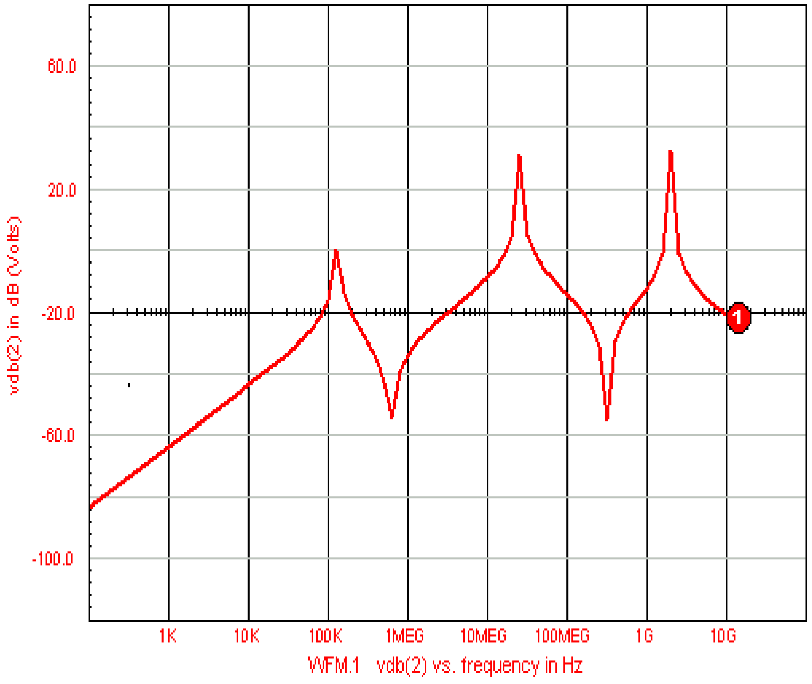


Figure 5.

Now using the same power supply network equivalent circuit let us see (Figure 6) the transient response to a current step pulse with a rise time equal to the following:

$$\mathrm{Trise} = \frac{2}{200\mathrm{M}} = 0.01\mu\mathrm{s} \qquad \textbf{\textit{Eqn. 21}}$$

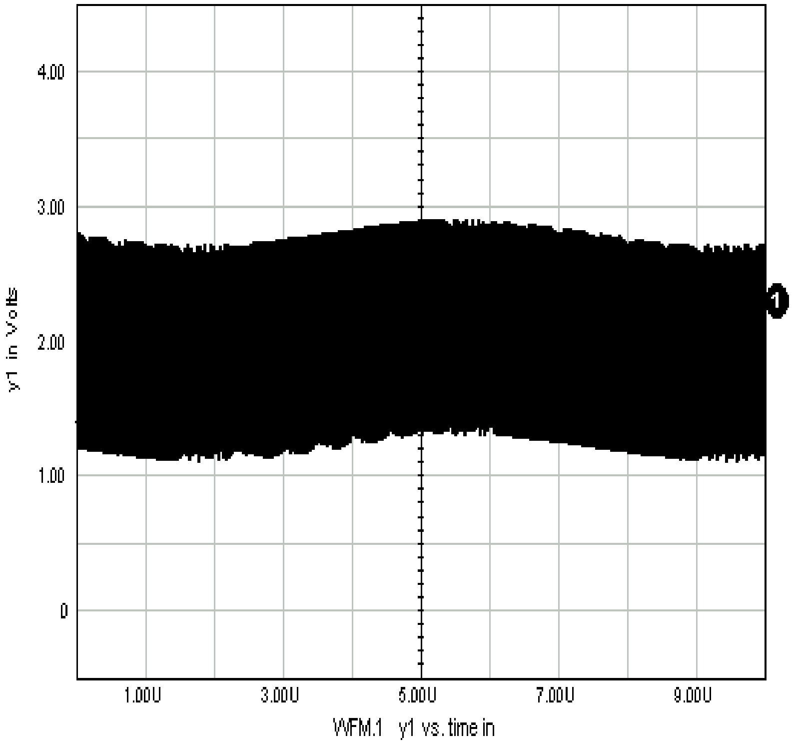


Figure 6. Transient Response to a Current Step Pulse

To increase the accuracy of the circuit model, include the effective series resistance of each capacitor as well as including some wiring resistance, which acts as a damping factor. We expect to see a different transient response from what we have seen so far. For example, if we assume a total resistance of 0.01 Ω for the series of all capacitors as well as for the power plane, the schematic resembles Figure 7.

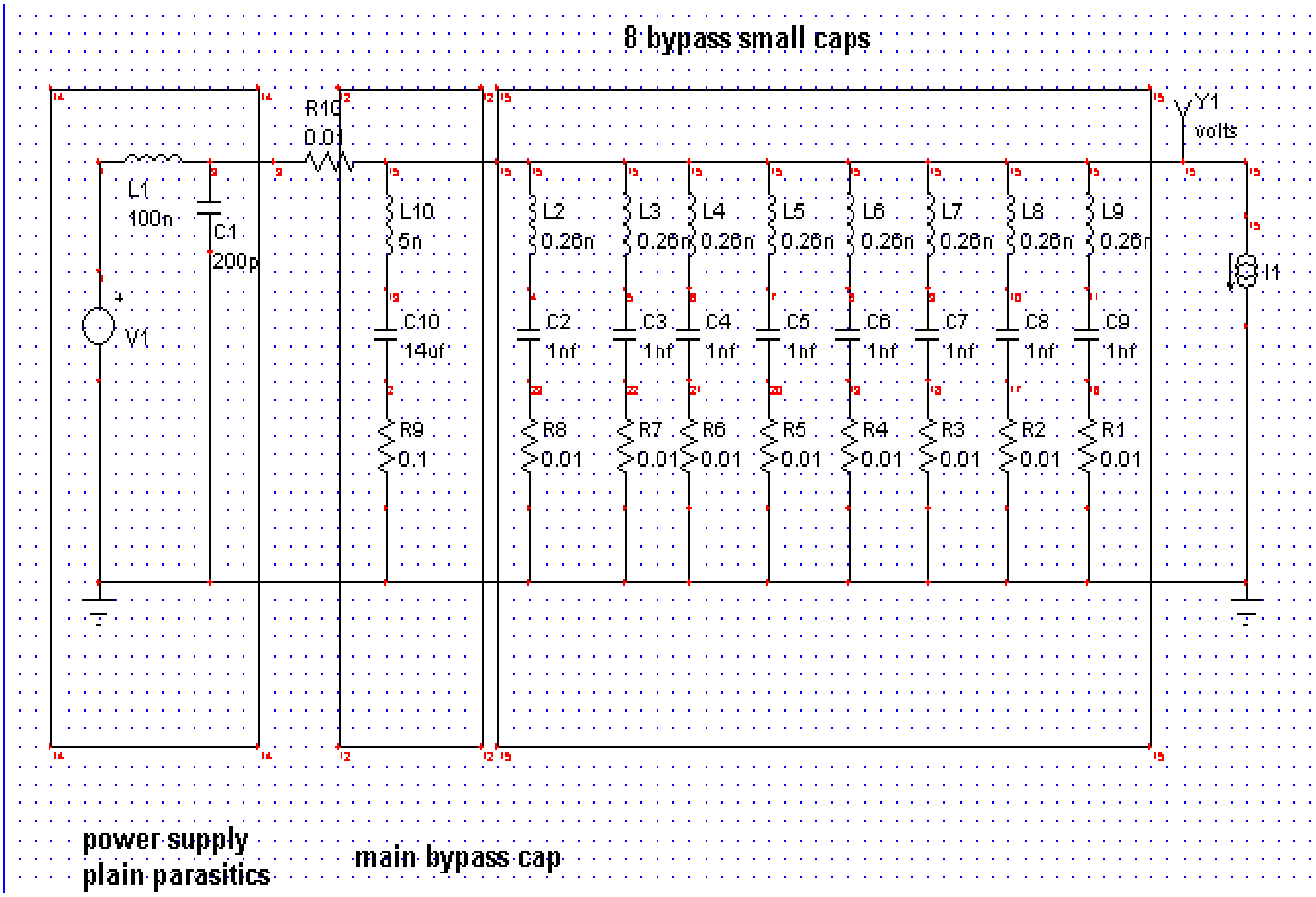


Figure 7.

Figure 8 shows the same circuit model that we have so far, but with additional damping resistors that are inherent in each bypass capacitor as well as the power supply delivery network. The step response resembles Figure 8.

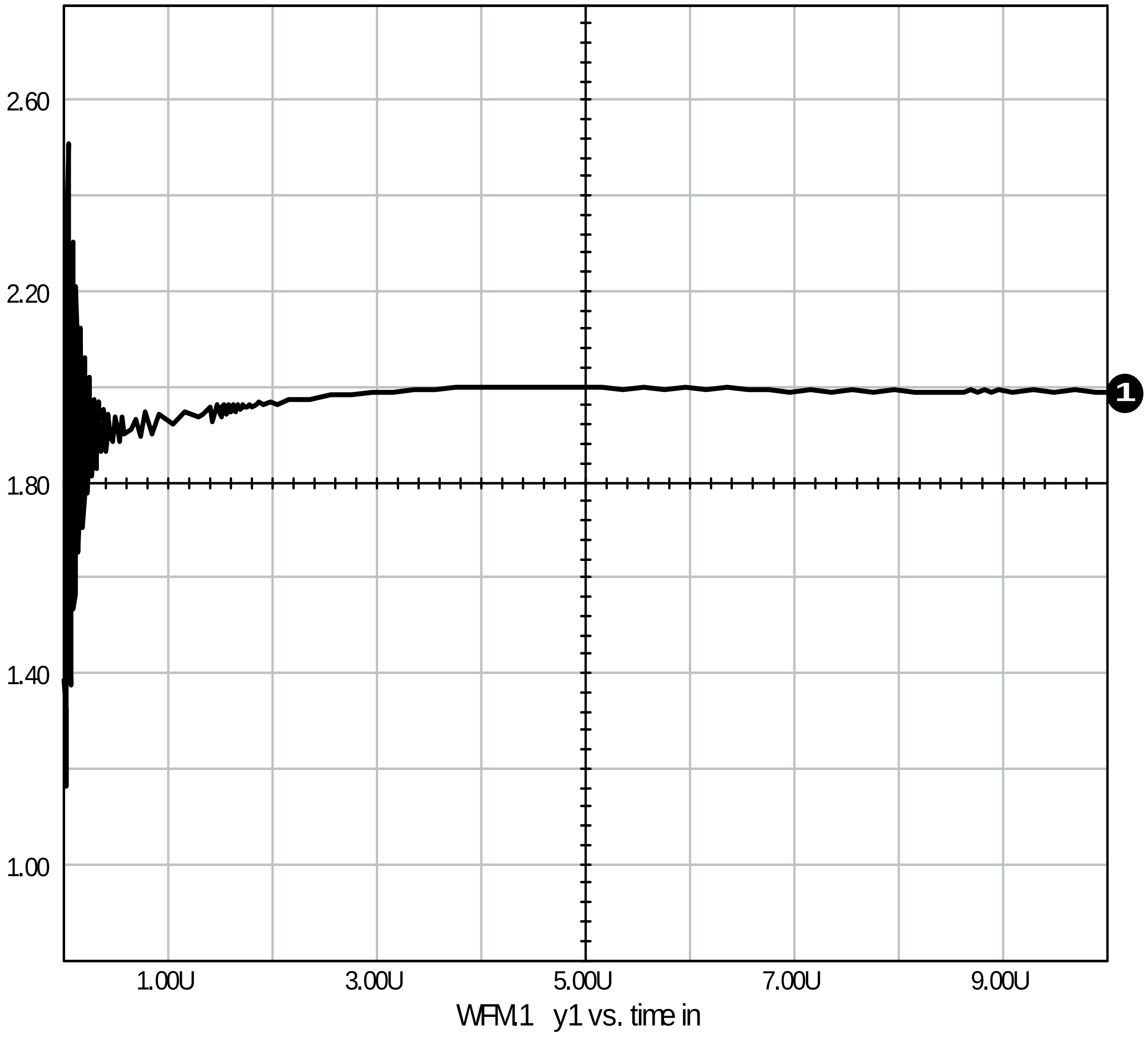


Figure 8. Step Response

Also, the AC response to the 1 Amps sweeping AC at the current source of the load resembles Figure 9. Note how the damping resistance changes the AC response.

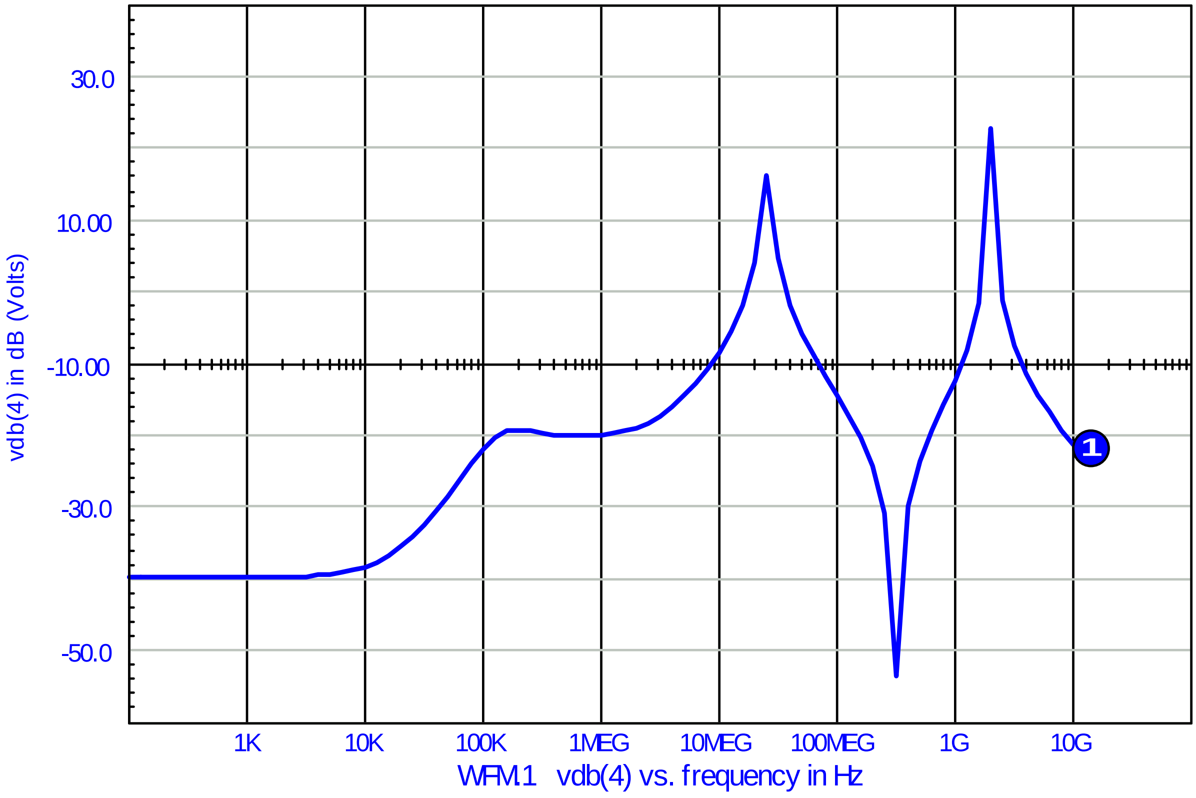


Figure 9.

The analysis of the problem so far can be summarized as follows:

1. DC power drop is not taken into account across the network.
2. All vias models are ignored.
3. Very short power plane is assumed as well as no load, chip, package parasitic are included.
4. The approach of calculating the bypass capacitor did not take into account the accurate model of bypass capacitor.
5. The analysis deals with the system as a pure circuit in terms of AC and transient., which is not accurate because we have an inherent transmission line model that behaves differently for the higher frequency signal transients.
6. The effect of EMI circuit model behavior is not analyzed.

3.2 How to Model the Load

When we design our power system model, we do not care about the details of the internal blocks of a processor. What we care about are the following:

- The number of power levels to provide (I/O, core, Analog, and so on).
- The chip package parasitic.
- Any coupling between different power pins.

- Any coupling inside the die itself between different power blocks.
- The block power demand circuit model.

As stated earlier, the scope of this application note is the core power delivery network, even though the ideas in this application can be extended and applied for the I/O and PLL. The board designer should create an integrated environment for the processor so that all power pins have a good supply with minimum interference between these rails. We started with an attempt to model the power side of the processor so that we can use it in our simulation, analysis, and so on. It is impractical to introduce the complex circuit model of the internal processor blocks in the power model. The most frequent modeling technique is to model the processor power side as a set of the following:

- Current source that switches from min to max, to include the worst case scenarios.
- Internal die capacitance.
- Internal die resistance.
- Package parasitics, inductance resistance and some capacitance.

The simplified power module would resemble Figure 10:

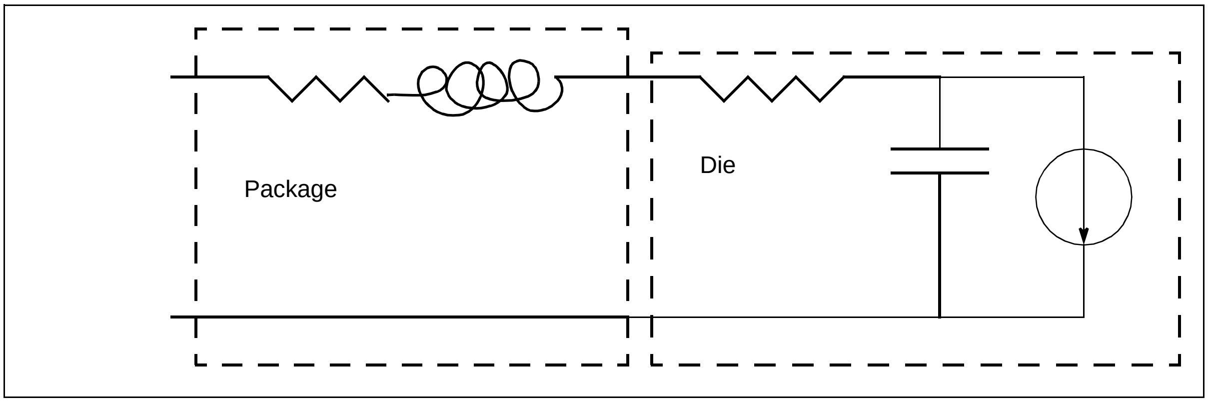


Figure 10. Simplified Power Model

As shown in Figure 11, the MPC8260 has three main power inputs:

- Core supply inputs around 2 V
- I/O supply input around 3.3 V
- PLL supply input less noisy 2 V inputs

For the grounding, the MPC8260 has the following:

- Main ground pins for I/O and core current return
- PLL ground current return pins

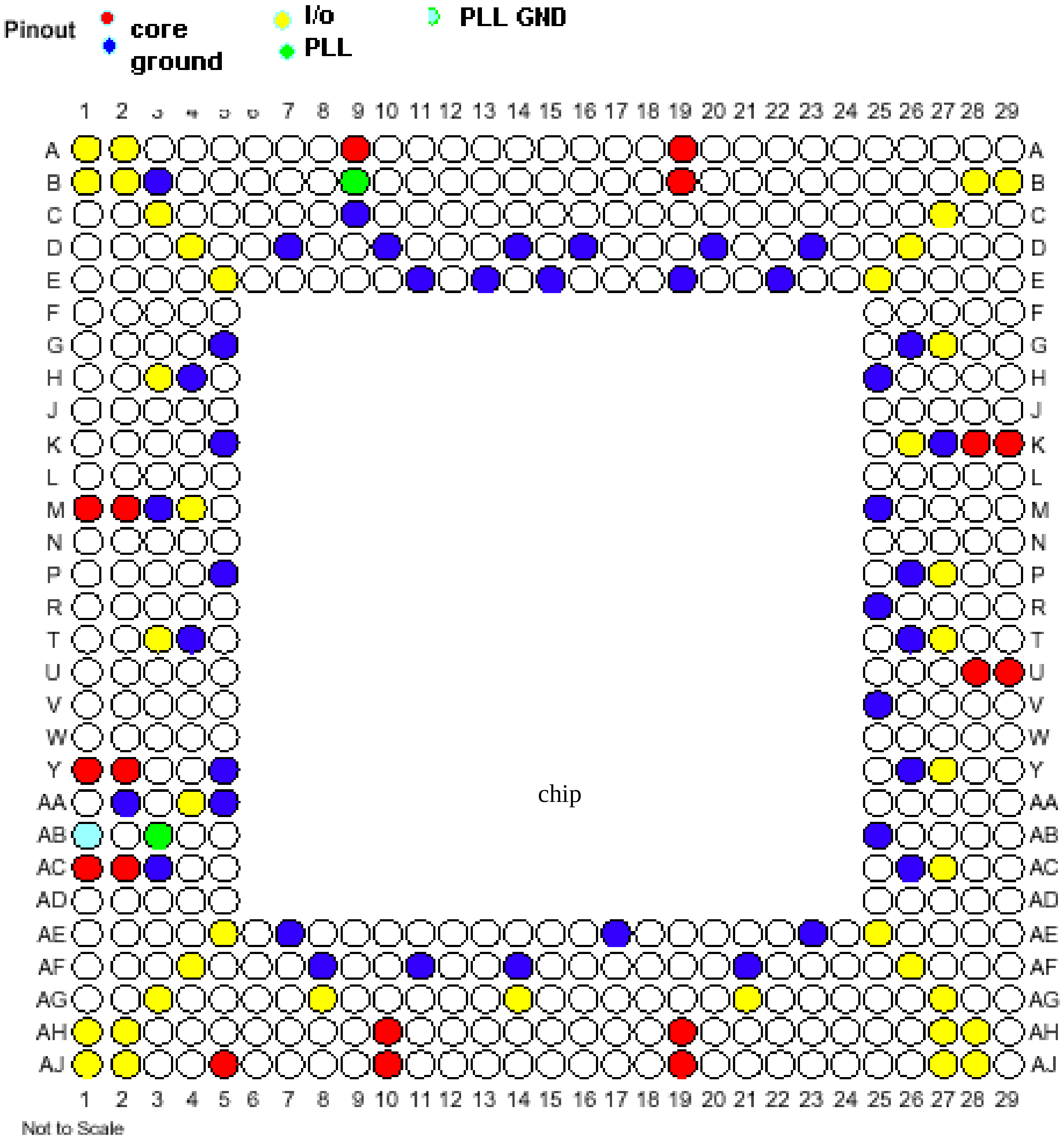


Figure 11. MPC8260 Power and Ground Pins

A fair distribution of power and ground around the processor creates a symmetry in terms of current paths. Note how most of the ground pins are placed inside the rim of the package. This placement is important because in the board layout it is easy to extend routes from these pins towards the center of the processor direction and then to vias to the ground plan, for example. This arrangement makes it easy for the layout engineer to do the bypass coupling pads directly under the processor in the other side of the board, thus locating the capacitors in a very close vicinity to the processor.

3.3 How to Model the Power Distribution Network

Designing, modeling and analyzing the power distribution network involves many considerations, such as the following:

- The number of power planes needed and why.
- Stack up arrangement.
- DC capacity of the power plan. It must handle enough current whithout overstressing.
- Mechanical and physical constraints. There should be enough estate to deliver generous currents.
- Whether to take care of EMI issues up front.
- Coupling; constraints on signal integrities.

Derive a clear view for these issues and an optimal solution that satisfies all the requirements. When the layout is done, verify that it can achieve all the goals. There are several different modeling methods, all dependent on the following:

- Accuracy of the model.
- Computing capacity.
- Results desired.

Two main methods can simulate the 3D structures:

- Full wave analysis, such as the following:
  - Finite element Method FEM
  - Method of Moments MoM
  - Finite difference time domain method, FDTD
- Partial element equivalent circuit method, PEEC

Many available commercial tools can accommodate all of these methods. The main idea is based on Maxwell’s equations that deals with E, D, H, B in real time. Then an attempt is made to put constraints, boundary values, based on the 3D geometry provided by the layout engineer. These equations are made discrete in both time and space, with an accuracy level that is consequently lost. When the tools have the discrete equation that can be represented in a matrix format, the tools attempt to solve these matrices given an input and a desired output. Many results can be obtained and used to study the behavior of the design as well as to do the ‘what if’ analysis to optimize the design.

Many methods can simplify the simulation analysis by reducing the computation time. Some of these techniques are based on the TLM method in which the power plan is a mesh of transmission lines. A SPICE-like simulator solves the system equation accordingly (see Figure 12):

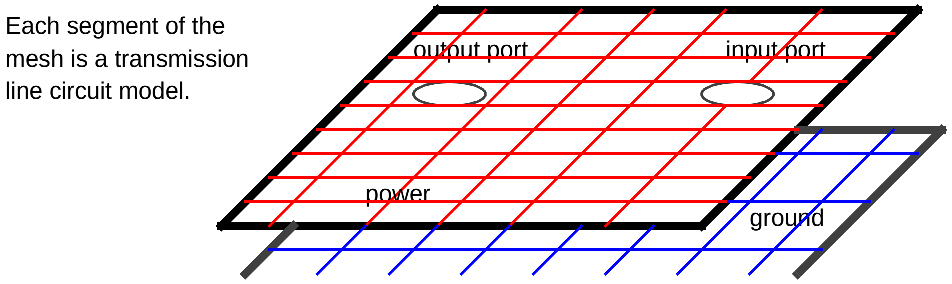


Figure 12.

3.4 PDN Model

When a circuit model is extracted from the layout, the design engineer can do the circuit analysis needed to proof that the layout comply with constraints. For example, the model of the board can generate a system equation like the following:

$$V = ZI \qquad \text{Eqn. 22}$$

Where V is the node voltages across the mesh. Thus, from the circuit designer's point of view, the power distribution system resembles Figure 13.

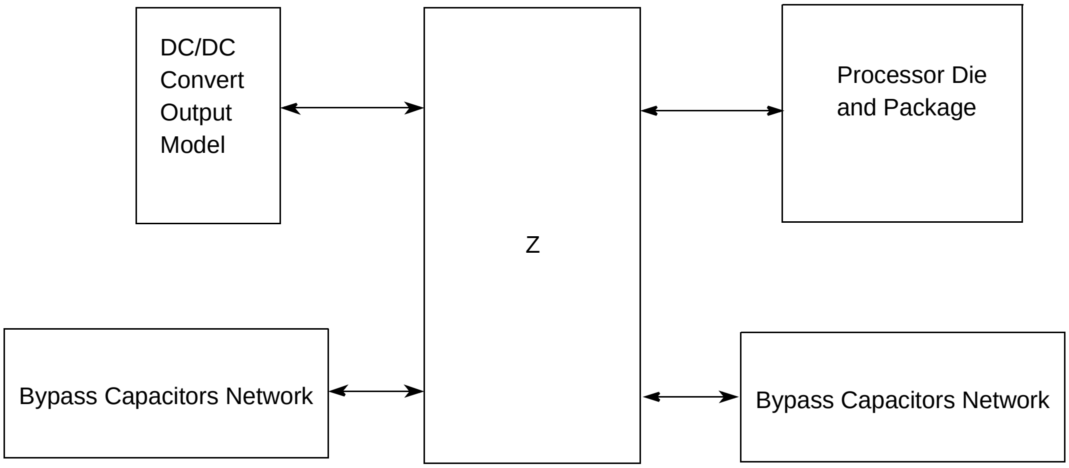


Figure 13.

Layout and circuit designers are interested in the overall circuit behavior, including the supply, DC/DC converter for instance, model, and bypass capacitors network that are close to the processor and the supply and in the PSD network. The circuit engineer may be interested in achieving the following constraint, for example, where Vi is any voltage node in the PDS for all times:

$$|Vi(t)| \leq \text{constant} \qquad \text{Eqn. 23}$$

. The design challenge is how to achieve this goal using the following:

- Selection of optimum number of bypass capacitors
- Selection of optimum location of the bypass capacitors
- Modification of layout geometry

3.5 Placement of the Decoupling Capacitor

The issue of placing the decoupling cap involves the following:

- Capacitor model
- Decoupling route model
- Via model

Placing a decoupling capacitor on the power distribution network changes its overall impedance profile. When we identify the main peaks of the PDN impedance, we try to add bypass capacitors that can suppress those peaks as much as possible. If the capacitor is placed in a board surface opposite to the processor board surface, a via must be in series with the bypass capacitor, which weakens the efficiency of the bypass because the via has an inductance that is approximated as the following (where *L* is the inductance of via in nH, *H* is the height of the inductance, and *d* is the diameter in inches):

$$L = 5.08 \times h \times \ln\left(\frac{4 \times h}{d} + 1\right) \qquad \text{Eqn. 24}$$

Also, vias have capacitance that depends on the via type. Bypass capacitors can be placed as closely as possible to the nodes Vi that exhibit higher |Vi(t)|, implying that we are trying to keep the absolute value of the node voltage below a certain constant and enabling us to budget for noise that is superimposed over the constant DC value.

Many techniques automate the bypass capacitors placement process. As in any optimization problem, we must have an energy function that we are to minimize. Then we have to descend across this energy surface via changing the bypass capacitor locations. Each time the bypass capacitor location is changed, a new Z matrix is generated for the PDN. The process continues until the goal of keeping all |Vi(t)| less than a constant is reached.

3.6 How the Via Causes EMI Problems

We must be aware of the effects of vias not from the bypass capacitor only but also from the power feed point of view. Vias are used to provide current paths to inner layers of the system board. The problem is that the current at the via must pass normally down the surface of the board. This direction change causes electromagnetic coupling with other vias, signals, or power, and radiation potential.

The electromagnetic coupling between vias is an important factor of cross-talk between signals that have vias close to each other. Vias have two types of inductances:

- Self-inductance, a function of the via geometry
- Mutual inductance with each neighboring via

To model the PCB more accurately, vias self- and mutual inductances must be taken into account. The radiation from Via accrues if the via is carrying a high frequency signal, and the via happens to be close to two parallel conductors. the emission is towards the PCB edges parallel to the PCB surface.

4 References

1. Howard W. Johnson, Martin Graham. *High Speed Digital Design A Handbook Of Black Magic*. Prentice Hall,1993, pp. 263–292.
2. T.C. Edwards, M.B. STEER. *Foundations of Interconnect and Microstrip Design*, Third edition. Wiley, 2000, pp. 315–344.
3. Balsha R.Stanisc, Rob A. Rutenbar, L. Richard Carley. *Synthesis of power distribution to manage signal integrity in mixed-signal ICs*. Kluwer Academic Publishers, 1996.
4. Stephen H. Hall, Garrett W. Hall, James A. McCall. *High Speed Digital System Design A Handbook of Interconnect theory an Design Practice*.Wiley 2000, pp. 102–154.
5. Hartmut Grabinski. *Interconnects in VLSI Design*. Kluwer Acadimic Publishers, 2000, pp. 61–147.
6. S. Boyd, L. Vandenberghe, A. El Gamal, S. Yun. “Design of Robust Power and Ground Networks.” *IEEE Trans Adv Pack*.2001.
7. Shiyou Zhao; Roy, K.; Cheng-Kok Koh. “Decoupling capacitance allocation and its application to power-supply noise-aware floor planning. Computer-Aided Design of Integrated Circuits and Systems,” *IEEE Transactions on*, Volume: 21 Issue: 1, Jan. 2002, pp. 81–92
8. Shiyou Zhao, Kaushik Roy, Cheng-Kok Koh. “Decoupling Capacitance Allocation for Power Supply Noise Suppression.” *IEEE Trans Adv. Pack*. 2001.
9. Nanju Na, Jinwoo Choi. “Modeling and Simulation of Core Switching Noise for ASICs. Advanced Packaging,” *IEEE Transactions on* [see also Components, Packaging and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on], Volume: 25 Issue: 1, Feb. 2002, pp. 4–11
10. Sachio Hayashi, Masaaki Yamada. “EMI Noise Analysis under ASIC Design Environment. Computer-Aided Design of Integrated Circuits and Systems,” *IEEE Transactions on*, Volume: 19 Issue: 11, Nov. 2000, pp. 1337–1346.
11. Russ Joseph, Margret Martonosi. “Run-Time Power Estimation in High Performance Microprocessors.” *Low Power Electronics and Design, International Symposium on, 2001*, 2001, pp. 135–140.
12. Sudhakar Bobba, Ibrahim N. Hajj. “Maximum Voltage Variation in the Power Distribution Network of VLSI Circuits with RLC models.” *Low Power Electronics and Design, International Symposium on, 2001*. 6–7 Aug. 2001, pp. 376–381.
13. Rajendran Panda, Savithri Sundareswaran, David Blaauw. “On the Interaction of Power Distribution Network with Substrate.” *Low Power Electronics and Design, International Symposium on, 2001*, 6–7 Aug. 2001, pp. 388–393

14. Zheng, L.-R.; Li, B.-X.; Tenlunen, H. “Efficient and accurate modeling of power supply noise on distributed on-chip power networks. Circuits and Systems, 2000.” *Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium*, Volume: 2, 28–31 May 2000, pp. 513–516.
15. Yi-Min Jiang; Kwang-Ting Cheng. “Vector generation for power supply noise estimation and verification of deep submicron designs.” *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, Volume: 9 Issue: 2, April 2001, pp. 329–340.

5 Revision History

Table 2 provides a revision history for this application note.

Table 2. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	1/2004	Initial release
1	1/2007	Non-substantive formatting.

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