



Migrating to PowerQUICC™ III TSEC from Previous Ethernet Controllers

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When migrating to a PowerQUICC™ III microprocessor, it is necessary to understand the differences among the MPC85xx three-speed Ethernet controller (MPC85xx TSEC), MPC8540 fast Ethernet controller (MPC8540 FEC), and previous Ethernet controllers. This application note summarizes these differences with the following objectives:

- To help customers develop Ethernet drivers for the MPC85xx TSEC and the MPC8540 FEC
- To illustrate how the TSEC programming flow and features differ from those of previous Ethernet controllers
- To provide recommendations for using the MPC85xx TSEC and the MPC8540 FEC

Contents

1 Ethernet Features	2
2 Programming Flows	3
3 Buffer Descriptors and General Differences	6
3.1 Receive Buffer Descriptors	6
3.2 Transmit Buffer Descriptors	11
3.3 General Ethernet Controller Differences	16
4 Requirements and Recommendations	16
5 Revision History	17

1 Ethernet Features

The following Ethernet controllers are in MPC8xx, MPC82xx, and MPC85xx communications processors:

- SCC Ethernet mode. In MPC8xx and MPC82xx devices, this controller uses the serial communications controller (SCC) of the CPM and supports 10 Mbps Ethernet only.
- MPC8xx fast Ethernet controller (MPC8xx FEC). In MPC8xx devices, this controller is a separate block from the CPM.
- MPC82xx fast Ethernet controller (MPC82xx FEC). This controller uses the fast communications controller (FCC), which is part of the CPM in MPC82xx devices.
- MPC8560 CPM Ethernet controller. Based on the MPC82xx FEC, this controller uses the FCC that is part of the CPM in MPC8560 devices.
- MPC85xx three-speed Ethernet controller (MPC85xx TSEC). In MPC85xx devices, this controller is a separate block from the CPM. It supports 10/100/1000 Mbps Ethernet.
- MPC8540 fast Ethernet controller (MPC8540 FEC). In MPC8540 devices, this controller is based on the MPC85xx TSEC and supports 10/100 Mbps Ethernet only.

Table 1 shows a side-by-side comparison of these Ethernet controllers.

Table 1. Comparison of Features in Ethernet Controllers

Features	MPC8xx and MPC82xx SCC Ethernet Mode	MPC8xx FEC	MPC82xx FEC and MPC8560 CPM Ethernet Controller	MPC8540 FEC	MPC85xx TSEC
10/100/1000 Mbps IEEE 802.3 GMII	No	No	No	No	Yes
10/100 Mbps IEEE 802.3 MII	No	Yes	Yes	Yes	Yes
10 Mbps IEEE 802.3	Yes (7-wire)	Yes (MII and 7-wire)	Yes (MII)	Yes (MII)	Yes (MII)
1000 Mbps IEEE 802.3z TBI	No	No	No	No	Yes
10/100 Mbps RGMII	No	No	No	No	Yes
1000 Mbps full-duplex RGMII	No	No	No	No	Yes
1000 Mbps RTBI	No	No	No	No	Yes
Full and half-duplex support	Yes	Yes	Yes	Yes	Yes (1000 Mbps supports only full-duplex)
IEEE 802.3 full-duplex flow control	No	No	Yes	Yes	Yes
Supports out-of-sequence transmit queue (for initiating flow-control)	No	No	Yes	Yes	Yes

Table 1. Comparison of Features in Ethernet Controllers (continued)

Features	MPC8xx and MPC82xx SCC Ethernet Mode	MPC8xx FEC	MPC82xx FEC and MPC8560 CPM Ethernet Controller	MPC8540 FEC	MPC85xx TSEC
Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE 802.1 virtual local area network (VLAN) tags and priority.	Yes (up to 1522 bytes)	Yes (up to 1522 bytes)	Yes (up to 1522 bytes)	Yes (up to 9.6k jumbo frames)	Yes (up to 9.6k jumbo frames)
Retransmission from transmit FIFO following a collision	Yes	Yes	Yes	Yes	Yes
Support CRC generation and verification of inbound/outbound packets	Yes	Yes	Yes	Yes	Yes
Address recognition	Yes	Yes	Yes	Yes	Yes
Broadcast address (accept/reject)	Yes	Yes	Yes	Yes	Yes
Exact match 48-bit individual (unicast) address	Yes	Yes	Yes	Yes	Yes
Hash check of individual (unicast) addresses	64-bit hash	64-bit hash	64-bit hash	256-bit hash	256-bit hash
Hash check of group (multicast) addresses	64-bit hash	64-bit hash	64-bit hash	256-bit hash	256-bit hash
Promiscuous mode	Yes	Yes	Yes	Yes	Yes
Extraction data and its associated buffer descriptors can be directed to processor's L2 cache to reduce access latency.	No	No	No	Yes	Yes
RMON statistics support	No	No	Yes	No	Yes

2 Programming Flows

Figure 1 through Figure 4 show typical programming flows for the various Ethernet controllers. Note that the programming flows for MPC85xx TSEC and MPC8540 FEC are the same. However, note also that for the MPC8540 FEC, the user must choose nibble mode for MII (MACCFG2[I/F_Mode] = 1). For details, see the “MAC Configuration Register 2” section in the *MPC8540 PowerQUICC III Integrated Host Processor Reference Manual*. Figure 1 shows the typical programming flow for the MPC8xx and MPC82xx SCC Ethernet mode.

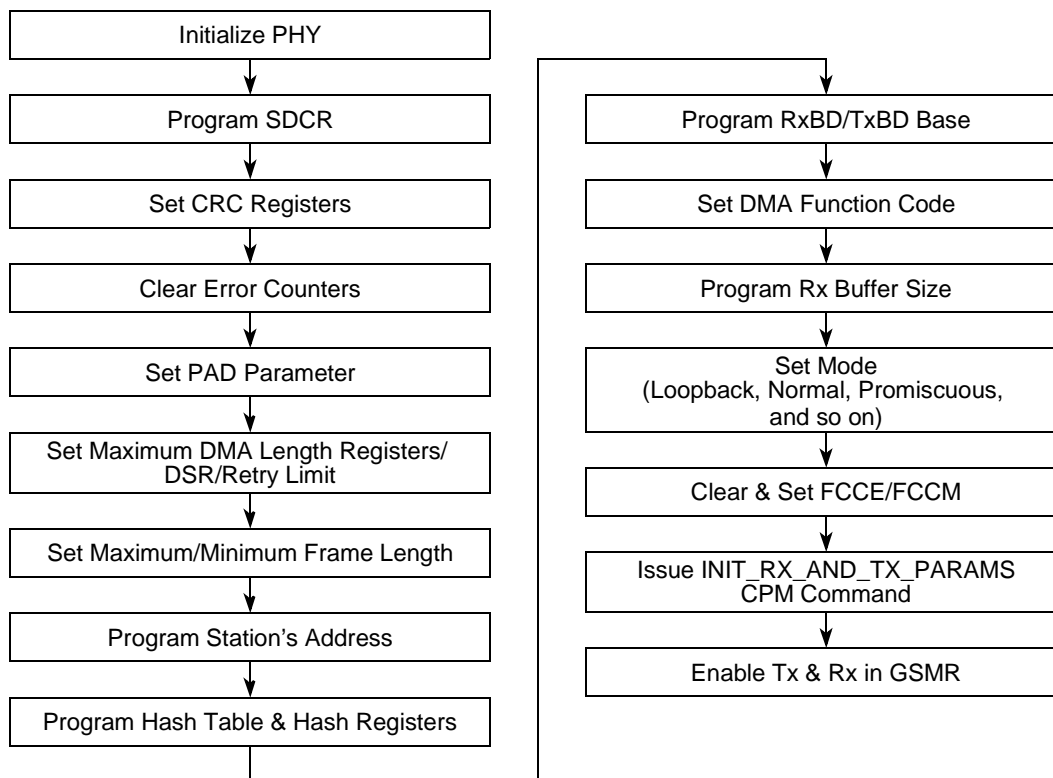


Figure 1. Typical MPC8xx and MPC82xx SCC Ethernet Mode Programming Flow

Figure 2 shows the typical programming flow for the MPC8xx FEC controller.

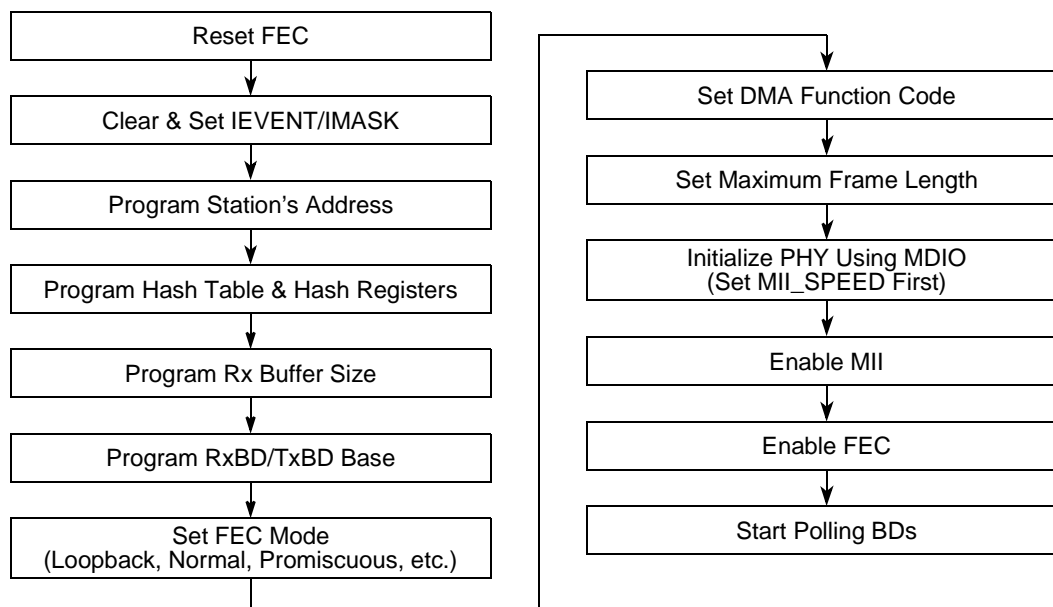


Figure 2. Typical MPC8xx FEC Programming Flow

Figure 3 shows the typical programming flow for the MPC82xx FEC and MPC8560 CPM Ethernet controller.

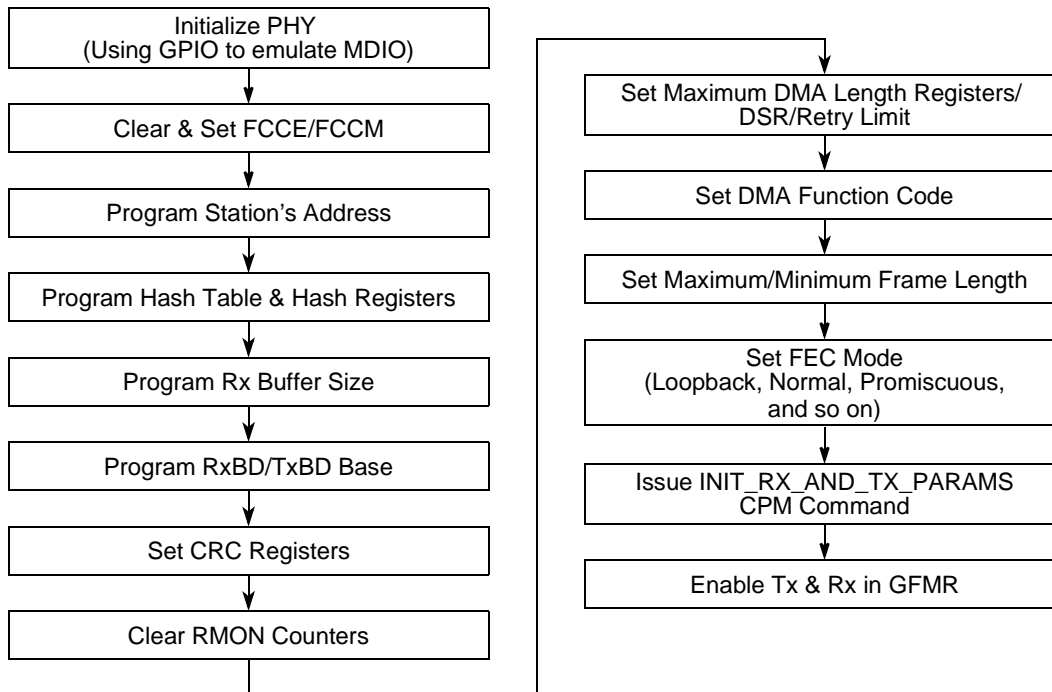


Figure 3. Typical MPC82xx FEC and MPC8560 CPM Ethernet Controller Programming Flow

Figure 4 shows the typical programming flow for the MPC85xx TSEC and MPC8540 FEC controllers.

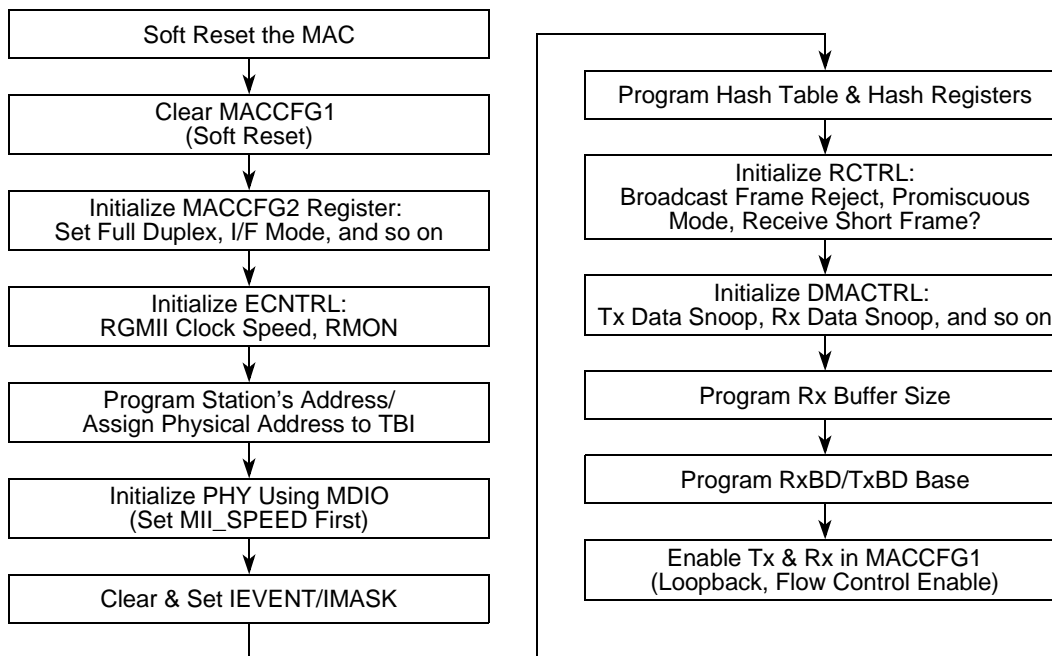


Figure 4. Typical MPC85xx TSEC and MPC8540 FEC Programming Flow

NOTE

If the Ethernet PHY supports auto-negotiation, set the TSEC full/half duplex modes *after* the auto-negotiation. The modes must match the mode that the PHY auto-negotiated.

3 Buffer Descriptors and General Differences

The buffer descriptor (BD) format of all Ethernet controllers is primarily the same. Only a few of the status and control fields (Offset + 0) change between each controller, allowing more flexibility when migrating software from one Ethernet controller to another. Figure 5 shows and describes (RxBD) and (TxBD) fields that are consistent for each device. Status and control fields that differ subject-to-device are highlighted and described in Figure 6 through Figure 9 (RxBD) and in Figure 14. Below each figure is a table that contains descriptions of the unique fields. For additional information, see the reference manual for the respective device.

3.1 Receive Buffer Descriptors

The following sections discuss receive buffer descriptors.

3.1.1 Common Fields of Receive Buffer Descriptors

Figure 5 shows the fields of a receive buffer descriptor, highlighting those common to all Ethernet controllers. Fields that contain an asterisk are unique to each Ethernet controller.

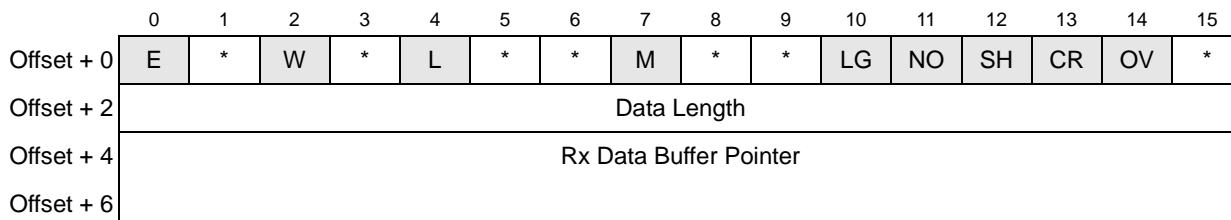


Figure 5. Common Receive Buffer Descriptor Format

Table 2 describes the RxBD fields that are common to all Ethernet controllers. See Figure 6 through Figure 9 for descriptions of fields that are unique to a specific Ethernet controller.

Table 2. Receive Buffer Status and Control Field Descriptions (Common Fields Only)

Bits	Name	Description
0	E	Empty. Written by controller (when cleared) and by user (when set). 0 The data buffer associated with this buffer descriptor is filled with received data, or an error condition causes abort of data reception. The status and length fields were updated as required. 1 The data buffer associated with this buffer descriptor is empty or reception is currently in progress.
2	W	Wrap. Written by user. 0 The next buffer descriptor is found in the consecutive location. 1 The next buffer descriptor is found at the location defined elsewhere (device-dependent).

Table 2. Receive Buffer Status and Control Field Descriptions (Common Fields Only) (continued)

Bits	Name	Description
4	L	Last in frame. Written by controller. 0 The buffer is not the last in a frame. 1 The buffer is the last in a frame.
6	—	Reserved, should be cleared.
7	M	Miss. Written by controller. (This bit is valid only if the L-bit is set and the controller is in promiscuous mode.) This bit is set by the controller for frames that were accepted in promiscuous mode but were flagged as a 'miss' by the internal address recognition. Thus, while in promiscuous mode, the user can use the M-bit to determine quickly whether the frame was destined to this station. 0 Frame received because of an address recognition hit. 1 Frame received because of promiscuous mode.
10	LG	Rx frame length violation. Written by controller. (This bit is valid only if the L-bit is set.) A frame length greater than maximum frame length was recognized.
11	NO	Rx non-octet aligned frame. Written by controller. (This bit is valid only if the L-bit is set.) A frame that contained a number of bits not divisible by eight was received.
12	SH	Short frame. Written by controller. (This bit is valid only if the L-bit is set.) A frame length that was less than the minimum length defined for this channel was recognized.
13	CR	Rx CRC error. Written by controller. (This bit is valid only if the L-bit is set.) This frame contains a CRC error and is an integral number of octets in length. This bit is also set if a receive code group error is detected.
14	OV	Overrun. Written by controller. (This bit is valid only if the L-bit is set.) A receive FIFO overrun occurred during frame reception. If this bit is set, the other status bits, M, LG, NO, SH, and CR lose their normal meaning and are 0.

3.1.2 MPC8xx and MPC82xx SCC Ethernet Mode Receive Buffer Descriptors

Figure 6 shows the fields of a receive buffer descriptor for the MPC8xx and MPC82xx SCC Ethernet mode.

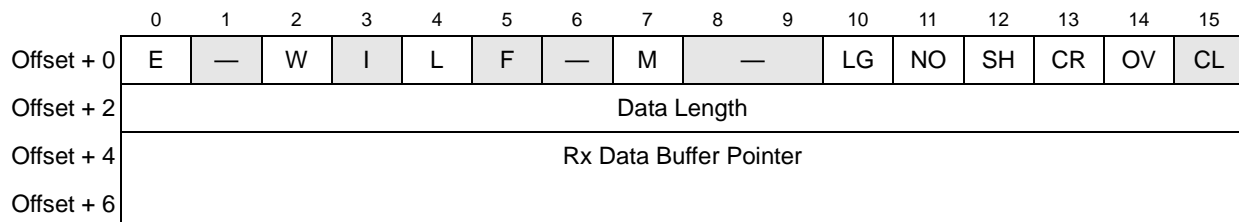

Figure 6. MPC8xx and MPC82xx SCC Ethernet Mode Receive Buffer Descriptor Format

Table 3 describes the RxB D fields unique to the MPC8xx and MPC82xx SCC Ethernet mode.

Table 3. MPC8xx and MPC82xx SCC Ethernet Mode RxB D Status and Control Field Descriptions (Unique Fields Only)

Bits	Name	Description
1	—	Reserved, should be cleared.
3	I	Interrupt. Note that this bit does not mask SCCE[RXF] interrupts. 0 No SCCE[RXB] interrupt is generated after this buffer is used. 1 SCCE[RXB] or SCCE[RXF] is set when the Ethernet controller uses this buffer. These two bits can cause interrupts if they are enabled.
5	F	First in frame. The Ethernet controller sets this bit when this buffer is the first one in a frame. 0 The buffer is not the first one in a frame. 1 The buffer is the first one in a frame.
6	—	Reserved, should be cleared.
8–9	—	Reserved, should be cleared.
15	CL	Collision. This frame is closed because a collision occurred during frame reception. CL is set only if a late collision occurs or if PSMR[RSH] is enabled. Late collisions are better defined in PSMR[LCW].

3.1.3 MPC8xx FEC Receive Buffer Descriptors

Figure 7 shows the fields of a receive buffer descriptor for the MPC8xx FEC.

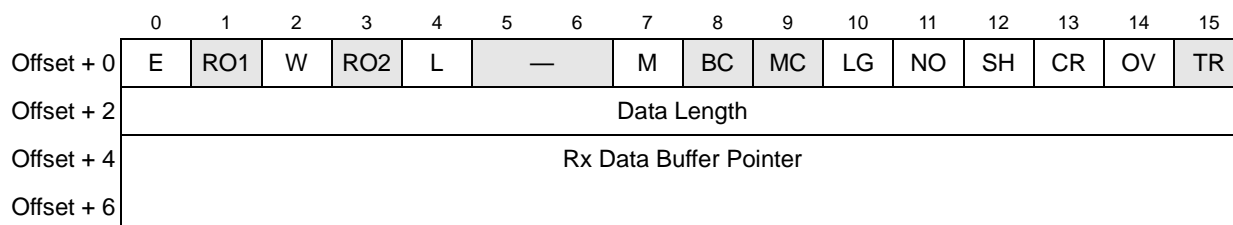


Figure 7. MPC8xx FEC Receive Buffer Descriptor Format

Table 4 describes the RxB D fields unique to the MPC8xx FEC.

Table 4. MPC8xx FEC RxB D Status and Control Field Descriptions (unique fields only)

Bits	Name	Description
1	RO1	Receive software ownership bit. Software use. This read/write bit is modified by hardware and does not affect hardware.
3	RO2	Receive software ownership bit. Software use. This read/write bit is not modified by hardware and does not affect hardware.
5–6	—	Reserved.
8	BC	Set if the DA is broadcast.
9	MC	Set if the DA is multicast and not broadcast.
15	TR	Truncate. Set if the receive frame is truncated (≥ 2 Kbytes).

3.1.4 MPC82xx FEC and MPC8560 CPM Ethernet Controller Receive Buffer Descriptors

Figure 8 shows the fields of a receive buffer descriptor for the MPC82xx FEC and MPC8560 CPM Ethernet controller.

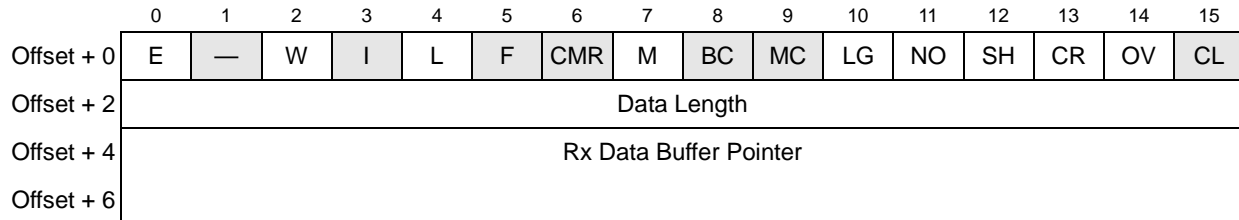


Figure 8. MPC82xx FEC and MPC8560 CPM Ethernet Controller Receive Buffer Descriptor Format

Table 5 describes the RxBDF fields unique to the MPC82xx FEC and MPC8560 CPM.

Table 5. MPC82xx FEC and MPC8560 CPM Ethernet Controller RxBDF Status and Control Field Descriptions (Unique Fields Only)

Bits	Name	Description
1	—	Reserved, should be cleared.
3	I	Interrupt 0 No interrupt is generated after this buffer is used. 1 FCCE[RXB] or FCCE[RXF] are set when the Ethernet controller uses this buffer. These two bits can cause interrupts if they are enabled.
5	F	First in frame. Set by the Ethernet controller when this buffer is the first in a frame. 0 Not the first buffer in a frame 1 First buffer in a frame
6	CMR	CAM match result for the frame. Set by the Ethernet controller when using a CAM for address matching and FPSMR[ECM] = 1. Valid only if the L bit is set. 0 A hit in the CAM 1 A miss in the CAM
8	BC	Broadcast address. Valid only for the last buffer in a frame (RxBDF[L] = 1). The received frame address is the broadcast address.
9	MC	Multicast address. Valid only for the last buffer in a frame (RxBDF[L] = 1). The received frame address is a multicast address other than a broadcast address.
15	CL	Collision. This frame is closed because a collision occurred during frame reception. Set only if a late collision occurs or if FPSMR[RSH] is set. The late collision definition is determined by the setting of FPSMR[LCW].

3.1.5 MPC85xx TSEC and MPC8540 FEC Receive Buffer Descriptors

Figure 9 shows the fields of a receive buffer descriptor for the MPC85xx TSEC and MPC8540 FEC.

Figure 9. MPC85xx TSEC and MPC8540 FEC Receive Buffer Descriptor Format.

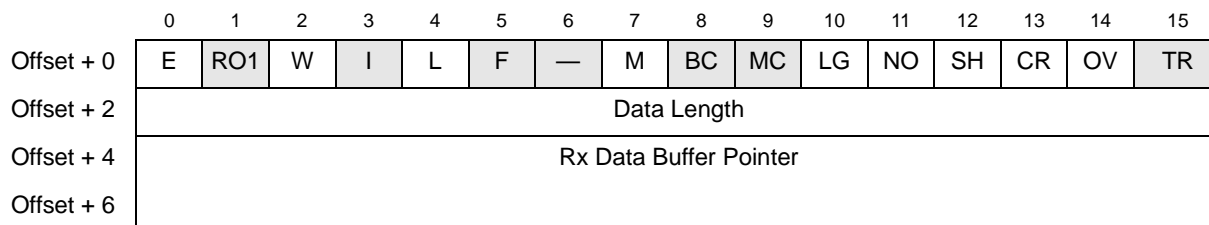


Table 6 describes the RxBD fields unique to the MPC85xx TSEC and MPC8540 FEC

Table 6. MPC85xx TSEC and MPC8540 FEC RxBD Status and Control Field Descriptions (Unique Fields Only)

Bits	Name	Description
1	RO1	Receive software ownership bit. Reserved for use by software. This read/write bit is not modified by hardware, nor does its value affect hardware.
3	I	Interrupt. Written by user. 0 No interrupt is generated after this buffer is serviced. 1 IEVENT[RXB0] or IEVENT[RXF0] are set after this buffer is serviced. This bit can cause an interrupt if enabled (IMASK[RXBEN0] or IMASK[RXFEN0]). If the user wants to be interrupted only if RXF0 occurs, the user must disable RXB0 (IMASK[RXBEN0] is cleared) and enable RXF0 (IMASK[RXFEN0] is set).
5	F	First in frame. Written by TSEC. 0 The buffer is not the first in a frame. 1 The buffer is the first in a frame.
6	—	Reserved, should be cleared.
8	BC	Broadcast. Written by TSEC. (Only valid if L is set.) Is set if the DA is broadcast (FF-FF-FF-FF-FF-FF).
9	MC	Multicast. Written by TSEC. (Only valid if L is set.) Set if the DA is multicast and not BC.
15	TR	Truncation. Written by TSEC. (Valid only if L is set.) Set if the receive frame is truncated. This situation can happen if a frame length greater than maximum frame length was received and the MACCFG2[Huge Frame Enable] is cleared. If this bit is set, the frame must be discarded and the other error bits must be ignored because they may be incorrect.

3.2 Transmit Buffer Descriptors

The following sections discuss transmit buffer descriptors.

3.2.1 Common Fields of Transmit Buffer Descriptors

Figure 10 shows the fields of a transmit buffer descriptor, highlighting those common to all Ethernet controllers. Fields that contain an asterisk are unique to each Ethernet controller.

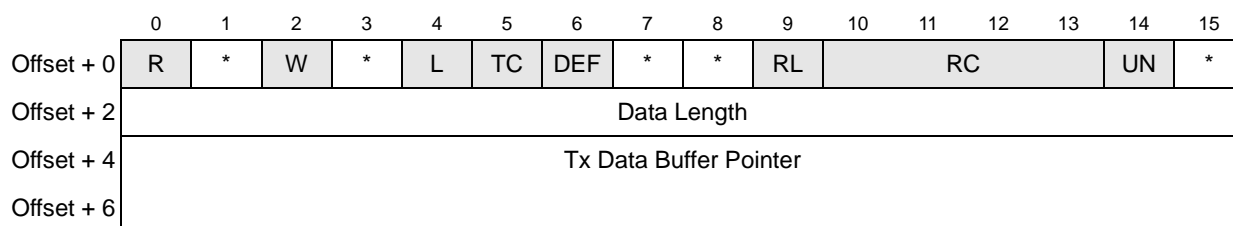


Figure 10. Common Transmit Buffer Descriptor Format

Table 7 describes the TxBD fields common to all Ethernet controllers. See Figure 11 through Figure 14 for descriptions of fields unique to a specific Ethernet controller.

Table 7. Transmit Buffer Status and Control Field Descriptions
(Common Fields Only)

Bits	Name	Description
0	E	Ready. Written by controller and user. 0 The data buffer associated with this buffer descriptor is not ready for transmission. The user may manipulate this buffer descriptor or its associated data buffer. The controller clears this bit after the buffer is transmitted or after an error condition is encountered. 1 The data buffer, which is prepared for transmission by the user, was not transmitted or is currently being transmitted. No fields of this buffer descriptor may be written by the user once this bit is set.
2	W	Wrap. Written by user. 0 The next buffer descriptor is found in the consecutive location. 1 The next buffer descriptor is found at the location defined elsewhere (device dependent).
4	L	Last in frame. Written by controller. 0 The buffer is not the last in a frame. 1 The buffer is the last in a frame.
5	TC	Tx CRC. Written by user. Valid only when L = 1. 0 End transmission immediately after the last data byte with no hardware-generated CRC appended. 1 Transmit the CRC sequence after the last data byte. Note for MPC85xx devices: (Valid only while it is set in first buffer descriptor and TxBD[PAD/CRC] is cleared and MACCFG2[PAD/CRC] is cleared and MACCFG2[CRC EN] is cleared.) If MACCFG2[PAD/CRC] is set or MACCFG2[CRC EN] is set, this bit is ignored.

Table 7. Transmit Buffer Status and Control Field Descriptions (Common Fields Only) (continued)

Bits	Name	Description
6	DEF	Defer indication. Hardware updates this bit if an excessive defer condition occurs. 0 This frame was not deferred. 1 This frame was deferred before being sent successfully. Note for MPC85xx devices: If HAFDUP[EXCESS_DEFER] = 1, this frame did not have a collision before it was sent but it was sent late because of deferring. If HAFDUP[EXCESS_DEFER] = 0, this frame was aborted and not sent.
9	RL	Retransmission limit. Written by controller. 0 Transmission before maximum retry limit is hit. 1 The transmitter failed (max. retry limit + 1) attempts to successfully send a message due to repeated collisions. The controller terminates the transmission and updates RL.
10–13	RC	Retry count. Written by controller. 0 The frame is sent correctly the first time or, if RL is set, the retry limit was reached. x One or more attempts were needed to send the transmit frame. If this field is 15, then 15 or more retries were needed. The Ethernet controller updates RC after sending the buffer.
14	UN	Underrun. Written by controller. 0 No underrun encountered. (Data was retrieved from external memory in time to send a complete frame). 1 The Ethernet controller encountered a transmitter underrun condition while sending the associated buffer. The controller terminates the transmission and updates UN.

3.2.2 MPC8xx and MPC82xx SCC Ethernet Mode Transmit Buffer Descriptors

Figure 11 shows the fields of a transmit buffer descriptor for the MPC8xx and MPC82xx SCC Ethernet mode.

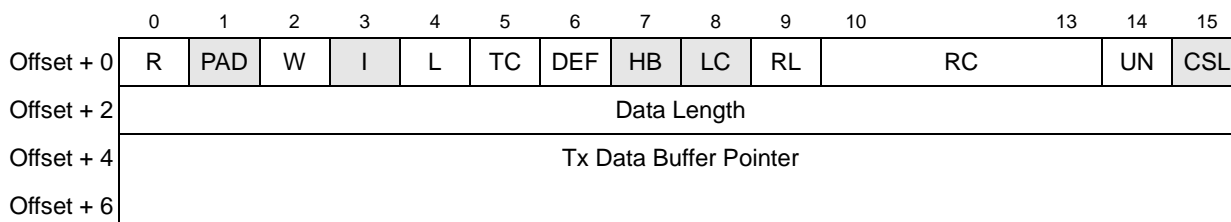


Figure 11. MPC8xx and MPC82xx SCC Ethernet Mode Transmit Buffer Descriptor Format

Table 8 describes the TxBD fields unique to the MPC8xx and MPC82xx SCC Ethernet mode.

Table 8. MPC8xx and MPC82xx SCC Ethernet Mode TxBD Status and Control Field Descriptions (Unique Fields Only)

Bits	Name	Description
1	PAD	Short frame padding. Valid only when L is set. Otherwise, it is ignored. 0 Do not add PADs to short frames. 1 Add PADs to short frames. Pad bytes are inserted until the length of the sent frame equals the MINFLR and they are stored in PADs in the parameter RAM.
3	I	Interrupt 0 No interrupt is generated after this buffer is serviced. 1 SCCE[TXB] or SCCE[TXE] is set after this buffer is serviced. These bits can cause interrupts if they are enabled.
7	HB	Heartbeat. Set when the collision input was not asserted within 20 transmit clocks after transmission. HB cannot be set unless PSMR[HBC] = 1. The SCC writes HB after it finishes sending the buffer.
8	LC	Late collision. Set when a collision occurred after the number of bytes defined for PSMR[LCW] are sent. The Ethernet controller stops sending and writes this bit after it finishes sending the buffer.
15	CSL	Carrier sense lost. Set when carrier sense is lost during frame transmission. The Ethernet controller writes CSL after it finishes sending the buffer.

3.2.3 MPC8xx FEC Transmit Buffer Descriptors

Figure 12 shows the fields of a transmit buffer descriptor for the MPC8xx FEC.

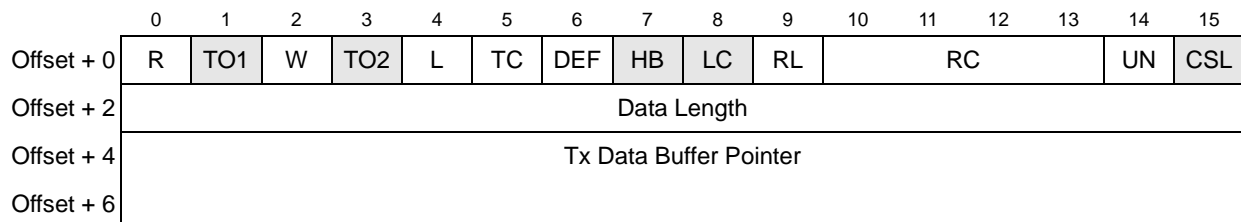


Figure 12. MPC8xx FEC Transmit Buffer Descriptor Format.

Table 9 describes the TxBD fields unique to the MPC8xx FEC.

Table 9. MPC8xx FEC TxBD Status and Control Field Descriptions (Unique Fields Only)

Bits	Name	Description
1	TO1	Transmit software ownership bit 1. This field is available for use by software. This read/write bit is not modified by hardware and its value does not affect hardware.
3	TO2	Transmit software ownership bit 2. This field is available for use by software. This read/write bit is not modified by hardware and its value does not affect hardware.
7	HB	Heartbeat error. Written by FEC (valid if L = 1). Set to indicate that the collision input was not asserted within the heartbeat window after transmission completed. HB can be set only if X_CNTRL[HBC] = 1.

Table 9. MPC8xx FEC TxBD Status and Control Field Descriptions (Unique Fields Only) (continued)

Bits	Name	Description
8	LC	Late collision. Written by FEC (valid if L = 1). Set to indicate that a collision occurred after 56 data bytes were transmitted. The FEC terminates the transmission.
15	CSL	Carrier sense lost. Written by FEC (valid if L = 1). Carrier sense dropped out or never asserted during transmission of a frame without collision.

3.2.4 MPC82xx FEC and MPC8560 CPM Ethernet Controller Transmit Buffer Descriptors

Figure 13 shows the fields of a transmit buffer descriptor for the MPC82xx FEC and MPC8560 CPM Ethernet controller.

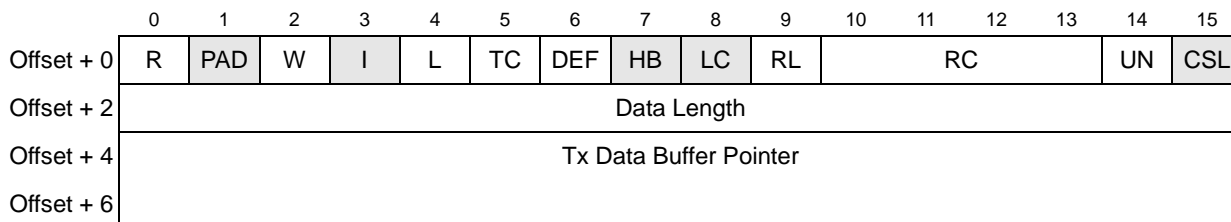


Figure 13. MPC82xx FEC and MPC8560 CPM Ethernet Controller Transmit Buffer Descriptor Format

Table 10 describes the TxBD fields unique to the MPC82xx FEC and MPC8560 CPM.

Table 10. MPC82xx FEC and MPC8560 CPM Ethernet Controller TxBD Status and Control Field Descriptions (Unique Fields Only)

Field	Name	Description
1	PAD	Short frame padding. Valid only when L = 1; otherwise, it is ignored. 0 Do not add PADs to short frames. 1 Add PADs to short frames. PAD bytes are inserted until the length of the transmitted frame equals the MINFLR. The PAD bytes are stored in a buffer pointed to by PAD_PTR in the parameter RAM.
3	I	Interrupt 0 No interrupt is generated after this buffer is serviced. 1 FCCE[TXB] or FCCE[TXE] is set after this buffer is serviced. These bits can cause interrupts if they are enabled.
7	HB	Heartbeat. The collision input is not asserted within 40 transmit serial clocks following completion of transmission. This bit cannot be set unless FPSMR[HBC] = 1. Written by the Ethernet controller after sending the associated buffer.
8	LC	Late collision. A collision occurred after the number of bytes defined in FPSMR[LCW] (56 or 64) are sent. The Ethernet controller terminates the transmission and updates LC after sending the buffer.
15	CSL	Carrier sense lost. Carrier sense is lost during frame transmission. The Ethernet controller updates CSL after sending the buffer.

3.2.5 MPC85xx TSEC and MPC8540 FEC Transmit Buffer Descriptors

Figure 14 shows the fields of a transmit buffer descriptor for the MPC85xx TSEC and MPC8540 FEC.

Figure 14. MPC85xx TSEC and MPC8540 FEC Transmit Buffer Descriptor Format.

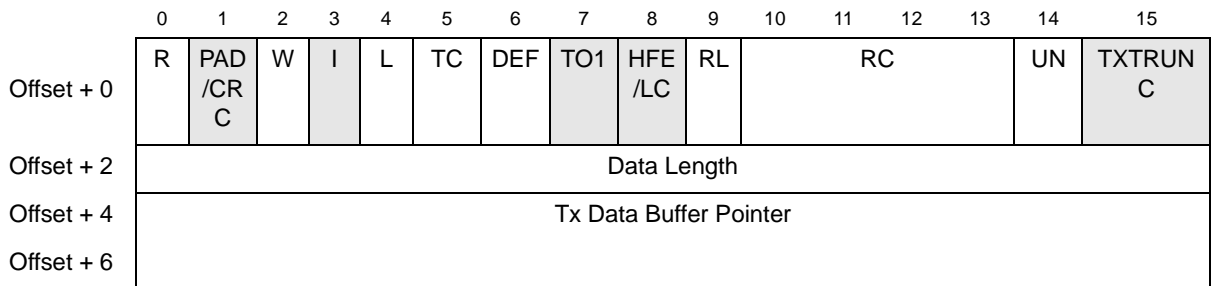


Table 11 describes the TxBD fields unique to the MPC85xx TSEC and MPC8540 FEC.

Table 11. MPC85xx TSEC and MPC8540 FEC TxBD Status and Control Field Descriptions (Unique Fields Only)

Field	Name	Description
1	PAD/ CRC	Padding and CRC attachment for frames. (Valid only while it is set in the first BD and MACCFG2[PAD/CRC enable] is cleared). If MACCFG2[PAD/CRC enable] is set, this bit is ignored. 0 Do not add padding to short frames. No CRC is appended unless TxBD[TC] is set. 1 Add PAD/CRCs to frames. PAD bytes are inserted until the length of the transmitted frame equals 64 bytes. Unlike the MPC8260 which PADs up to MINFLR value, TSEC always PADs up to the IEEE minimum frame length of 64 bytes. CRC is always appended to frames.
3	I	Interrupt. Written by user. 0 No interrupt is generated after this buffer is serviced. 1 IEVENT[TXB] or IEVENT[TXF] are set after this buffer is serviced. These bits can cause an interrupt if they are enabled (That is, IEVENT[TXBEN] or IEVENT[TXFEN] are set).
7	TO1	Transmit software ownership. This read/write bit may be utilized by software, as necessary. Its state does not affect the hardware nor is it affected by the hardware.
8	HFE/ LC	Huge frame enable (written by user)/late collision (written by TSEC) Huge frame enable. Written by user. Valid only while it is set in first BD and the MACCFG2[Huge Frame Enable] is cleared. If MACCFG2[Huge Frame Enable] is set, this bit is ignored. 0 Truncate transmit frame if its length is greater than the MAC's Maximum Frame Length register. 1 Do not truncate the transmit frame. Late collision. Written by TSEC. 0 No late collision. 1 A collision occurred after 64 bytes are sent. The TSEC terminates the transmission and updates LC.
15	TXTRU NC	The TSEC sets this bit to 1 when a BAPT condition truncates the frame. The BAPT condition occurs after the frame was transmitted exceeding the MAC's Maximum Frame Length.

3.3 General Ethernet Controller Differences

Note the following when comparing the MPC85xx TSEC and MPC8540 FEC to previous Ethernet controllers:

- The MPC85xx TSEC and MPC8540 FEC BDs were modeled based on the BD format of previous Ethernet controllers. Only a few status and control fields changed.
- In the MPC85xx TSEC and MPC8540 FEC, the CRC generation fields (TC and PAD/CRC) in the transmit BDs must be set in the first transmit BD of a frame. This requirement is different in MPC8xx FEC and MPC82xx FEC, in which the CRC generation field must be set on the last transmit BD.
- A 64-byte address alignment for receive data buffers is required in the MPC85xx TSEC and MPC8540 FEC. This requirement is different for previous Ethernet controllers, such as the MPC82xx FEC, which requires 32-byte address alignment.
- In the MPC85xx TSEC and MPC8540 FEC, the RC (retry count) and LC (late collision) bits are set in the current TxBD, unlike the CPM Ethernet controllers, in which these status bits are set in the last TxBD.
- Compared to other CPM-based Ethernet controllers, the MPC85xx TSEC and MPC8540 FEC have similar error handling procedures. Errors are reported in the channel BDs and in the IEVENT register. The IEVENT register is analogous to the Ethernet event register, FCCE, in MPC82xx FEC. To compare the definition of these registers, see the *MPC8260 PowerQUICC II Family Reference Manual* and the *MPC8560 PowerQUICC™ III Integrated Communications Processor Reference Manual*.
- When the MPC85xx TSEC or MPC8540 FEC report a ‘busy error’ condition (see the ‘Error Handling Procedure’ section of the *MPC8560 PowerQUICC™ III Integrated Communications Processor Reference Manual*), the controller sets the BSY field in the IEVENT register and stops until the RSTAT[RHLT] field is cleared. This behavior is different in MPC82xx FEC, in which the controller does not stop after reporting a ‘busy error’ condition.

4 Requirements and Recommendations

When using the MPC85xx TSEC or the MPC8540 FEC, adhere to the following guidelines:

- Do not use fewer than 2 buffer descriptors in a BD ring.
- Do not disable the transmitter (clearing MACCFG1[Tx_EN]) without stopping gracefully first (setting DMACTL[GTS] and confirming by polling IEVENT[GTSC]). Also, always gracefully stop (setting DMACTL[GRS] and confirming by polling IEVENT[GRSC]) *after* disabling the receiver (clearing MACCFG1[Rx_EN]). Failure to stop gracefully may cause the TSEC to lock up.
- Do not enable the MAC Tx if TBASE is cleared.
- Do not enable the MAC Rx if RBASE is cleared.
- Do not use loopback in half-duplex mode.
- Do not set the FIFO_TX_THR to the size of the Tx FIFO. Note that the maximum value for FIFO_TX_THR is the Tx FIFO size (2 Kbytes) minus the Tx internal DMA buffer size (64 bytes).

Furthermore, we recommend observing the following practices to improve system performance:

- Setting the FIFO_TX_THR too low may cause transmit underrun errors when the system is busy.
- Keep Tx data buffer pointers aligned to 32-byte addresses. Otherwise, the memory access transaction is divided into multiple transactions, which decreases performance.
- Limit the number of BDs needed to transmit a frame or receive a frame. We recommend using one BD per frame to reduce BD processing time to enhance system performance.
- Receive data buffers should be greater than 128 bytes. If a receive data buffer size of less than 128 bytes is needed, 64 byte data buffers can be used but the RxBDs must be placed in either DDR or L2 cache/SRAM memory.
- For jumbo frames, use data buffers greater than 128 bytes but less than 9.6 Kbytes. Larger data buffers can help avoid underrun errors.

5 Revision History

Table 12 provides a revision history for this application note.

Table 12. Document Revision History

Rev. No.	Substantive Change(s)
0	Initial release
1	Changed the second bullet in Section 4, "Requirements and Recommendations," to read as follows: <ul style="list-style-type: none"> • Do not disable the transmitter (clearing MACCFG1[Tx_EN]) without stopping gracefully first (setting DMACTL[GTS] and confirming by polling IEVENT[GTSC]). Also, always gracefully stop (setting DMACTL[GRS] and confirming by polling IEVENT[GRSC]) <i>after</i> disabling the receiver (clearing MACCFG1[Rx_EN]). Failure to stop gracefully may cause the TSEC to lock up.

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