Using the DSPI Module on the MPC5500 Family

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The MPC55xx family of microcontrollers provides several options for serial communication. The range of on-chip communication modules include the eSCI (Enhanced Serial Communication Interface), FlexCAN (Flexible Controller Area Network), and DSPI (Deserial/Serial Peripheral Interface).

This application note describes how the MPC55xx family implements SPI communication, as well as how to use the serialization/deserialization functions of the DSPI module.

The DSPI module supports serialization/deserialization of internal signals, such as the eTPU, eMIOS, and SIU interrupt signals. The purpose of serialization/deserialization is to allow functional pins to be used as GPIO.

Example code that configures the DSPI module for the modes mentioned above is included for reference.
1 Introduction

Figure 1 shows the block diagram of the MPC5554 device. The DSPI modules are located on Peripheral Bridge B.

All DSPI modules provide SPI (Serial Peripheral Interface), DSI (Deserial / Serial Interface), and CSI (Combined Serial Interface) functionality.

The SPI is a high speed (up to system frequency/4), full-duplex, four-wire synchronous interface. It is used to communicate to external devices such as sensors, voltage regulators, or A/D converters. To accommodate SPI transmit and receive queues, an efficient solution is to use the on-chip eDMA and SRAM modules. Alternatively, external RAM can be used.
Using the DSPI Module on the MPC5500 Family, Rev. 0
1.1 SPI

The SPI-bus is a 4-wire, full-duplex serial communications interface used by many microprocessor peripheral chips. The Serial Peripheral Interface (SPI) circuit is a synchronous serial data link that is standard across many microcontrollers and other peripheral chips. It provides support for a low/medium bandwidth network connection amongs MCUs and other devices supporting the SPI.

A synchronous clock shifts serial data into and out of a device in a configurable bit format. On the MPC55xx family, the frame size can be selected to be from 4–16 bits. However, when serial chaining of DSPI modules is selected, the number of bits to be transferred can be up to 64.

The SPI bus is a master/slave interface. Whenever two devices communicate, one is referred to as the "master," and the other as the "slave" device. The master drives the serial clock. When using SPI, data is simultaneously transmitted and received, making it a full-duplexed protocol.

The SPI signals on the MPC55xx family are as follows:
- SCK for serial clock, which is always driven by the master
- SOUT is the data out signal
- SIN is the serial data in signal
- PCS or peripheral chip select, used to enable the slave device

Figure 2 illustrates an 8-bit SPI transfer. Detailed in this figure are the different clock polarity options, i.e. the inactive state of the clock is LOW when DSPIx_CTAR[CPOL] = 0, or HIGH when DSPIx_CTAR[CPOL] = 1.

Also shown in Figure 2 is the sample point of the master and slave. The sample point is defined by the DSPIx_CTAR[CPHA] bit field. When this bit is 0, data is captured on the leading edge of SCK and changed on the following edge. When DSPIx_CTAR[CPHA] = 1, data is changed on the leading edge of SCK and captured on the following edge. The configurable delays are also illustrated in this figure.
From Figure 3, it can be seen that when in SPI mode, the DSPI Tx FIFO (4-entry transmit FIFO containing commands and data) transmits the data out onto the SOUT pin. When data is received on the SIN pin, it is transferred to the Rx FIFO via the shift register. Refer to Section 2 for SPI configuration and initialization information.
1.2 DSI

When Deserial Serial Interface (DSI) functionality is selected, the DSPI module is configured to serialize eTPU and eMIOS output channels and deserialize received data by routing it to the eTPU, eMIOS, or internal SIU interrupt inputs.

When DSI master mode is selected, the data to be transmitted can be taken from 16 internal parallel inputs from the eTPU or eMIOS. The data can also be taken from an alternate serialization data register (DSPIx_ASDR). Selection is dependent on the value of the DSPIx_DSICR[TXSS] bit. Refer to Figure 4.
When DSI slave mode is selected, the data received from the SPI bus is routed internally to the inputs of the eTPU, eMIOS, or SIU interrupts. The data to be routed internally is captured in the deserialization data register (DSPIx_DDR). Refer to Figure 5.

**1.3 CSI**

The Combined Serial Interface (CSI) mode allows the DSPI to operate in both SPI and DSI configuration, interleaving DSI frames with SPI frames. When there are SPI commands in the TX FIFO, the SPI data has priority over the DSI frames. When the TX FIFO is empty, the DSI transfer resumes.

Two peripheral chip select signals indicate whether DSI data or SPI data is transmitted. The user must configure the DSPI so that the two Clock and Transfer Attribute Registers (CTARs), associated with DSI data and SPI data, assert different peripheral chip select signals, denoted in Figure 5 as PCSx and PCSy. The DSI chip select is configured by writing the DSPIx_DSICR [DPCS, DSISTAS] bit fields accordingly. The SPI chip select is configured by writing the DSPIx_PUSHR[PCS, CTAS] bit fields accordingly.

**NOTE**

CSI mode is only supported in master mode.
2 DSPI Module Configuration

2.1 Data Transmission

There are two ways to transmit SPI data:

1. Application code writes command and data information to the DSPIx_PUSHR register. This pushes a 32-bit word (16-bit command and 16-bit data) into the TxFIFO. The TxFIFO is 4 entries deep.

2. The other method is to configure the eDMA, such that it fetches the commands and data from system RAM (RAM is an example, any system memory including flash memory could be used) and writes these values to the DSPIx_PUSHR register; i.e. create a transmit queue. Refer to Appendix A for source code that performs this task.

Figure 7 details the more efficient case 2.
The equivalent scenario applies for the reception of SPI messages. For reception, the DSPI TxFIFO can be flushed by writing 0b1 to DSPI FIFO. Entries can only be removed by shifting them out onto the SPI bus or by flushing the buffer. The interrupt (see Table 1). If a DMA transfer is selected, when TFFF = 1, the transfer is initiated. TFFF is only zeroed by the DSPI module when the TxFIFO buffer is full, i.e. when there are 4 entries in this buffer. TX FIFO entries can only be removed by shifting them out onto the SPI bus or by flushing the buffer. The TxFIFO can be flushed by writing 0b1 to DSPIx_MCR[CLR_TXF].

The equivalent scenario applies for the reception of SPI messages. For reception, the DSPIx SR[RFFDF] flag is used to trigger an eDMA transfer, moving the received data from a 4-entry RX FIFO to an area in system RAM. The draining of the RxFIFO is achieved by the associated eDMA channel reading the POP register (DSPIx_POPR). Refer to Appendix A for details of source code that implements the above functionality.

**Table 1. DSPI Interrupt/DMA Requests**

<table>
<thead>
<tr>
<th>Condition</th>
<th>Flag</th>
<th>Interrupt</th>
<th>DMA</th>
</tr>
</thead>
<tbody>
<tr>
<td>End of Queue reached (EOQ)</td>
<td>EOQF</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>TX FIFO is not Full</td>
<td>TFFF</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Transfer of Current Frame Complete</td>
<td>TCF</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Attempt to Transmit with an Empty Transmit FIFO¹</td>
<td>TFUF</td>
<td>X¹</td>
<td></td>
</tr>
<tr>
<td>RX FIFO is not Empty</td>
<td>RFDF</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Attempt to Transmit with an Empty Transmit FIFO¹</td>
<td>RFOF</td>
<td>X¹</td>
<td></td>
</tr>
<tr>
<td>FIFO Overrun¹</td>
<td>TFUF or RFOF</td>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 7. DSPI/eDMA Queue Creation**

In this figure, DSPIx_SR[TFFF] Transmit FIFO Fill Flag is used to trigger an eDMA transfer or cause an interrupt (see Table 1). If a DMA transfer is selected, when TFFF = 1, the transfer is initiated. TFFF is only zeroed by the DSPI module when the TxFIFO buffer is full, i.e. when there are 4 entries in this buffer. TX FIFO entries can only be removed by shifting them out onto the SPI bus or by flushing the buffer. The TxFIFO can be flushed by writing 0b1 to DSPIx_MCR[CLR_TXF].
Table 1 details all DSPI sources of interrupt requests and DMA transfers. It can be seen that there are 6 DSPI flags which can trigger an interrupt, and of those 6 flags, 2 can also cause a DMA request.

The 2 flags that can cause either an eDMA or interrupt request are DSPIx_SR[TFFF] and DSPIx_SR[RFDF]. This allows SPI communications to be handled with or without CPU intervention.

Selection of DMA over interrupt is controlled by the DSPIx_RSER [TFFF_RE,TFFF_DIRS,RFDF_RE and RFDF_DIRS] bit fields.

### 2.2 DSPIx_PUSHr

As mentioned previously, this register is used to transmit data out of the DSPI module. The following is an explanation of each of the bit fields:

<table>
<thead>
<tr>
<th>Bit Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CON</td>
<td>Continuous Peripheral Chip Select Enable. This bit field specifies if PCS signals remain asserted between transfers.</td>
</tr>
<tr>
<td>CTAS</td>
<td>Clock and Transfer Attributes Select. This is used to select one of CTAR 0:7 registers to be used for timings needed in communicating to external device. (Slave mode defaults to CTAR0)</td>
</tr>
<tr>
<td>EOQ</td>
<td>End of Queue</td>
</tr>
<tr>
<td>CTCNT</td>
<td>Clear SPI Transfer Counter. This provides a means to clear the SPI transfer counter (used for queue management).</td>
</tr>
<tr>
<td>PCS0:5</td>
<td>Peripheral Chip Select 0-5</td>
</tr>
<tr>
<td>TXData</td>
<td>Data to be transmitted</td>
</tr>
</tbody>
</table>

Notes:

1. The FIFO Overrun condition is created by OR-ing the TFUF and RFOF flags together.
NOTE

None of the control bits, including (EOQ and CTNT), are valid in slave mode.

### 2.3 DSPIx_CTAR[0:7]

<table>
<thead>
<tr>
<th>R</th>
<th>DBR</th>
<th>FMSZ</th>
<th>CPOL</th>
<th>CPHA</th>
<th>LSBFE</th>
<th>PCSSCK</th>
<th>PASC</th>
<th>PDT</th>
<th>PBR</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reset</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Reg Addr</td>
<td>Base + 0xC (DSPIx_CTAR0); 0x10 (DSPIx_CTAR1); 0x14 (DSPIx_CTAR2); 0x18 (DSPIx_CTAR3); 0x1C (DSPIx_CTAR4); 0x20 (DSPIx_CTAR5); 0x24 (DSPIx_CTAR6); 0x28 (DSPIx_CTAR7)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>R</th>
<th>CSSCK</th>
<th>ASC</th>
<th>DT</th>
<th>BR</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reset</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Reg Addr</td>
<td>Base + 0xC (DSPIx_CTAR0); 0x10 (DSPIx_CTAR1); 0x14 (DSPIx_CTAR2); 0x18 (DSPIx_CTAR3); 0x1C (DSPIx_CTAR4); 0x20 (DSPIx_CTAR5); 0x24 (DSPIx_CTAR6); 0x28 (DSPIx_CTAR7)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The DSPIx_CTAR[0:7] registers have the following bit fields for configuring the timing of the SPI frames:
- **FMSZ Frame Size**: 4 to 16 bits
- **CPOL Clock Polarity**: Inactive state of SCK is low (0) or high (1)
- **CPHA Clock Phase**:
  - 0: SCK Leading edge: data is captured; Following edge: data is changed
  - 1: SCK Leading edge: data is changed; Following edge: data is captured
- **LSBFE**: LSB First Enable – selects if LSB or MSB is transferred first.
- **PCSSCK, CSSCK**: PCS to SCK delay
- **PASC, ASC**: SCK to PCS delay
- **PDT, DT**: Delay after transfer (PCS negation to next PCS assertion)
- **PBR, BR**: Baud rate

These eight CTARs allow different frame types (baud rates, clock frequency, delays) to be entered into the TX FIFO queue.

### 2.4 Serialized / Deserialized Sources and Destinations

There are four sources for serialized data on the MPC5554. They are the following:
- eTPU_A, eTPU_B, and eMIOS output channels
DSPI Module Configuration

- Memory-mapped register DSPIx_ASDR

There are five destinations for deserialized data. They are the following:
- eTPU_A, eTPU_B, and eMIOS input channels
- SIU External Interrupt Request inputs
- Memory-mapped register in the DSPI

Refer to figures 8-11 for details of the individual connections.

### Figure 8. DSPI_A Connections

<table>
<thead>
<tr>
<th>eTPU_B</th>
<th>DSPI_A</th>
</tr>
</thead>
<tbody>
<tr>
<td>CH 15</td>
<td>IN 0</td>
</tr>
<tr>
<td>:</td>
<td>:</td>
</tr>
<tr>
<td>CH 0</td>
<td>IN 15</td>
</tr>
</tbody>
</table>

### Figure 9. DSPI_B Connections

<table>
<thead>
<tr>
<th>EMIOS</th>
<th>DSPI_B</th>
<th>SIU/IMUX</th>
</tr>
</thead>
<tbody>
<tr>
<td>CH 11</td>
<td>IN 0</td>
<td>IN1 IRQ[0]</td>
</tr>
<tr>
<td>CH 10</td>
<td>IN 1</td>
<td>IN1 IRQ[15]</td>
</tr>
<tr>
<td>CH 13</td>
<td>IN 14</td>
<td></td>
</tr>
<tr>
<td>CH 12</td>
<td>IN 15</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>eTPU_A</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CH 21</td>
<td>OUT 0</td>
<td></td>
</tr>
<tr>
<td>:</td>
<td>:</td>
<td></td>
</tr>
<tr>
<td>CH 16</td>
<td>OUT 13</td>
<td></td>
</tr>
<tr>
<td>CH 29</td>
<td>OUT 14</td>
<td></td>
</tr>
<tr>
<td>:</td>
<td>:</td>
<td></td>
</tr>
<tr>
<td>CH 24</td>
<td>OUT 15</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE**

In Figure 9, it may look as if there are 24 outputs; however, OUT[8:13] can be routed to eTPU_A or IRQ[8:13]. Likewise, OUT[14:15] can be routed to eMIOS[13:14].
A DSI transfer can be initiated in four different ways. They are the following:
- Continuous—data transmitted continuously
- Edge sensitive hardware trigger (when chaining DSPIs)
- Change in data (any change in the data to be transmitted causes a new SPI frame to be transmitted)
- Triggered or change in data

Table 2 details how each transfer initiation is selected. The method is dependent on the DSPI_DSICR[TRRE] and DSPI_DSICR[CID] bits.
2.5 Serial Chaining

As the eMIOS and eTPU channels are hardwired per DSPI module, if the user’s desired mix of channels to be serialized or deserialized is located on different DSPI modules, then serial chaining can be used to transfer the data in one frame. For example, if eTPU_A and eTPU_B channels are required to be serialized, then DSPI_A (for eTPU_B) and DSPI_B, _C, or _D (for eTPU_A) have to be used.

The MPC55xx supports parallel and serial chaining of DSPI modules. This can be achieved by using the hardware trigger mode. Refer to Appendix B source code that configures DSPI_A, _B, and _C for serial chaining.

Figure 10 shows a block diagram for chaining DSPI_A, _B, and _C serially to provide up to 48 (3 x 16) bits of serial data.

In Figure 12, DSPI_A is the master DSI module; both slave modules should be configured for change in data or triggered mode. When a slave has a change in data, the #MTRIG(Master Trigger) signal is asserted, propagating to the #HT (Hardware Trigger) input of the next slave or the master. Upon receiving this signal, the master then transmits a new SPI frame.
The SIU[DISR] register controls the internal shorting of the SCK, PCS, SOUT and SIN signals between modules. Refer to Revision 1.1 or later of the *MPC5554 Reference Manual* for more detail.

3 DSI Examples

3.1 Serialized Mode

Up to 16 eTPU (or a combination of eTPU and eMIOS ) channels can be serialized onto 3 wires (half-duplex master transmit) or 4 wires for master/slave operation. Data is taken from the eTPU, eMIOS, or ASDR and transmitted serially, as shown below in Figure 13. In the case of a half-duplex transfer, up to 13 pins can be saved as 16 outputs and can be transmitted on 3 pins. This means the 13 pins used previously for eTPU or eMIOS can be used as GPIO pins.
DSI Examples

A practical system application for serialization would be electronic transmission control, where the eMIOS PWM outputs are fed to solenoids that control the hydraulic fluid used for gear selection. Another example would be motor control in the industrial environment.

The following serialization example configures eMIOS channels 10–13 as general purpose outputs. These outputs are fed into inputs 6–9 of DSPI_D, as detailed in Table 3. Inputs 6–9 correspond to bits 6–9 of the SPI data frame. DSPI_D is configured as a DSI master, with DSPI_C configured as an SPI slave. DSPI_D is configured to transfer when there is a change in data.

The EMIOS_CCRn[EDPOL] bit is used to toggle the value of each of the four channels. When the channel value changes, this results in a new SPI frame being transmitted. The value transmitted can be viewed in the DSPI_C_POPR register.

For example, if channel 10 is changed from 0 to 1 and all remaining bit values are 0, then the value transmitted will be 0x0080.

Refer to Appendix C for the source code of this example.

Table 3. DSPI_D Connections

<table>
<thead>
<tr>
<th>DSPI_D Input</th>
<th>Connected to:</th>
<th>DSPI_D Output</th>
<th>Connected to:</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>eTPU_A Output Channel 21</td>
<td>0</td>
<td>Input 3 on IMUX for External IRQ[14]</td>
</tr>
<tr>
<td>1</td>
<td>eTPU_A Output Channel 20</td>
<td>1</td>
<td>Input 3 on IMUX for External IRQ[15]</td>
</tr>
<tr>
<td>2</td>
<td>eTPU_A Output Channel 19</td>
<td>2</td>
<td>N/C</td>
</tr>
<tr>
<td>3</td>
<td>eTPU_A Output Channel 18</td>
<td>3</td>
<td>N/C</td>
</tr>
<tr>
<td>4</td>
<td>eTPU_A Output Channel 17</td>
<td>4</td>
<td>Input 3 on IMUX for External IRQ[2]</td>
</tr>
<tr>
<td>5</td>
<td>eTPU_A Output Channel 16</td>
<td>5</td>
<td>Input 3 on IMUX for External IRQ[3]</td>
</tr>
<tr>
<td>6</td>
<td>EMIOS Output Channel 11</td>
<td>6</td>
<td>Input 3 on IMUX for External IRQ[4]</td>
</tr>
<tr>
<td>7</td>
<td>EMIOS Output Channel 10</td>
<td>7</td>
<td>Input 3 on IMUX for External IRQ[5]</td>
</tr>
<tr>
<td>8</td>
<td>EMIOS Output Channel 13</td>
<td>8</td>
<td>Input 3 on IMUX for External IRQ[6]</td>
</tr>
<tr>
<td>9</td>
<td>EMIOS Output Channel 12</td>
<td>9</td>
<td>Input 3 on IMUX for External IRQ[7]</td>
</tr>
<tr>
<td>10</td>
<td>eTPU_A Output Channel 29</td>
<td>10</td>
<td>Input 3 on IMUX for External IRQ[8]</td>
</tr>
<tr>
<td>11</td>
<td>eTPU_A Output Channel 28</td>
<td>11</td>
<td>Input 3 on IMUX for External IRQ[9]</td>
</tr>
<tr>
<td>12</td>
<td>eTPU_A Output Channel 27</td>
<td>12</td>
<td>Input 3 on IMUX for External IRQ[10]</td>
</tr>
<tr>
<td>13</td>
<td>eTPU_A Output Channel 26</td>
<td>13</td>
<td>Input 3 on IMUX for External IRQ[11]</td>
</tr>
<tr>
<td>14</td>
<td>eTPU_A Output Channel 25</td>
<td>14</td>
<td>EMIOS Input Channel 15, Input 3 on IMUX for External IRQ[12]</td>
</tr>
<tr>
<td>15</td>
<td>eTPU_A Output Channel 24</td>
<td>15</td>
<td>EMIOS Input Channel 14, Input 3 on IMUX for External IRQ[13]</td>
</tr>
</tbody>
</table>
NOTE
Input number refers to the bit number of the SPI frame that the signal to be serialized appears on. Output refers to the bit number of the SPI frame that is connected internally to the peripheral module.

3.2 Deserialized Mode

Data from a received SPI frame is routed through to the eTPU, eMIOS channels, or to the SIU interrupts, as illustrated in Figure 14.

The 16 SIU external interrupt inputs can be connected to either an external pin or to deserialized output signals from a DSPI module. This example is used to show how a deserialized message can cause an external interrupt on IRQ1. DSPI_A is used to transmit a SPI message to DSPI_B with bit 1 of the SPI frame controlling the interrupt. A practical example for this usage is when a SmartMOS™ device (such as the Freescale MC33394) in the system reports a fault to the MCU by asserting an interrupt.
The IRQn pins map to 16 independent interrupt request outputs from the SIU. An interrupt request is asserted when the corresponding IRQ Flag bit is set in in the (SIU_EISR) register, with the corresponding DMA/Interrupt Request Enable bit set in the DMA/Interrupt Request Enable Register (SIU_DIRER) and the corresponding DMA/Interrupt Select bit cleared in the DMA/Interrupt Request Select Register (SIU_DIRSR).

The IRQ Flag bit is set when an event as defined by IRQ Rising-Edge Event Enable Register (SIU_IREER) and IRQ Falling-Edge Event Enable Register (SIU_IFEER) occurs on the corresponding IRQn pin. This allows for rising, falling, or both edges to cause an interrupt. Figure 16 details graphically the process mentioned above.

From Table 4, it is evident that bit 1 of the SPI frame is routed through to input 1 on the SIU_IMUX, which connects to IRQ1. When the value 0x2 is received by DSPI_B, IRQ1 will be asserted. Refer to Appendix D for source code that implements a deserialized interrupt.

### Table 4. DSPI_D Connections

<table>
<thead>
<tr>
<th>DSPI_B Input</th>
<th>Connected to:</th>
<th>DSPI_B Output</th>
<th>Connected to:</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>EMIOS Output Channel 11</td>
<td>0</td>
<td>Input 1 on IMUX for External IRQ[0]</td>
</tr>
<tr>
<td>1</td>
<td>EMIOS Output Channel 10</td>
<td>1</td>
<td>Input 1 on IMUX for External IRQ[1]</td>
</tr>
<tr>
<td>2</td>
<td>eTPU_A Output Channel 21</td>
<td>2</td>
<td>Input 1 on IMUX for External IRQ[2]</td>
</tr>
<tr>
<td>3</td>
<td>eTPU_A Output Channel 20</td>
<td>3</td>
<td>Input 1 on IMUX for External IRQ[3]</td>
</tr>
<tr>
<td>4</td>
<td>eTPU_A Output Channel 19</td>
<td>4</td>
<td>Input 1 on IMUX for External IRQ[4]</td>
</tr>
<tr>
<td>5</td>
<td>eTPU_A Output Channel 18</td>
<td>5</td>
<td>Input 1 on IMUX for External IRQ[5]</td>
</tr>
<tr>
<td>6</td>
<td>eTPU_A Output Channel 17</td>
<td>6</td>
<td>Input 1 on IMUX for External IRQ[6]</td>
</tr>
<tr>
<td>7</td>
<td>eTPU_A Output Channel 16</td>
<td>7</td>
<td>Input 1 on IMUX for External IRQ[7]</td>
</tr>
<tr>
<td>8</td>
<td>eTPU_A Output Channel 29</td>
<td>8</td>
<td>Input 1 on IMUX for External IRQ[8]</td>
</tr>
<tr>
<td>9</td>
<td>eTPU_A Output Channel 28</td>
<td>9</td>
<td>Input 1 on IMUX for External IRQ[9]</td>
</tr>
<tr>
<td>10</td>
<td>eTPU_A Output Channel 27</td>
<td>10</td>
<td>Input 1 on IMUX for External IRQ[10]</td>
</tr>
<tr>
<td>11</td>
<td>eTPU_A Output Channel 26</td>
<td>11</td>
<td>Input 1 on IMUX for External IRQ[11]</td>
</tr>
<tr>
<td>12</td>
<td>eTPU_A Output Channel 25</td>
<td>12</td>
<td>Input 1 on IMUX for External IRQ[12]</td>
</tr>
<tr>
<td>13</td>
<td>eTPU_A Output Channel 24</td>
<td>13</td>
<td>Input 1 on IMUX for External IRQ[13]</td>
</tr>
<tr>
<td>14</td>
<td>EMIOS Output Channel 13</td>
<td>14</td>
<td>Input 1 on IMUX for External IRQ[14]</td>
</tr>
<tr>
<td>15</td>
<td>EMIOS Output Channel 12</td>
<td>15</td>
<td>Input 1 on IMUX for External IRQ[15]</td>
</tr>
</tbody>
</table>
The input source for each SIU external interrupt is individually specified in the external IRQ input select register (SIU_EIISR). An example of the multiplexing of an SIU external interrupt input is given in Figure 15. As shown in the figure, the IRQ0 input of the SIU can be sourced from either the IRQ0_GPIO203 pin, the DSPI_B0 serial input signal, the DSPI_C1 serialized input signal, or the DSPI_D2 serialized output signal.

All IRQ inputs are multiplexed in the same manner. The inputs to the IRQ from each DSPI module are offset by one, so that if more than one DSPI module is connected to the same external device type, a separate interrupt can be generated for each device. This also applies to DSPI modules connected to external devices of different type that have status bits in the same bit location of the deserialized information.

![Figure 15. Multiplexing an SIU External Interrupt Input](image-url)
NOTE

As every pin on the MPC55xx is configured individually, the function for the IRQ pins must be initialized to IRQ if required. However, in the example above, the pin is not monitored; it is the internal signal that causes the interrupt to be asserted. For further information on interrupts, the registers mentioned above, and those in previous sections, please refer to the MPC5554 Reference Manual, Revision 1.1, 05/2004 or later.

4 MPC5xx / MPC5554 SPI Comparison

Table 5 illustrates the direct comparison of the MPC5554 DSPOI module and the MPC5xx QSPI module with regardsto SPI communication.

<table>
<thead>
<tr>
<th>Source</th>
<th>Digital Filter</th>
<th>Rising Edge &amp; Falling Edge Enables</th>
<th>Status Flag</th>
<th>DMA or IRQ Enable</th>
<th>DMA or IRQ Select</th>
<th>IRQx (to INTC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRQ Pin</td>
<td>IDFR</td>
<td>IREER &amp; IFEER</td>
<td>EISR Clear</td>
<td>DIRER</td>
<td>DIRSR</td>
<td></td>
</tr>
</tbody>
</table>

Software writes “1” Service DMA Request OR

Another IRQ from same source

Overrun Request Enabled ORER

Overrun Status OR

Global Error IRQ

Figure 16. External Interrupt Configuration for the IRQ pins (logic gates are descriptive and not implemented in hardware)
<table>
<thead>
<tr>
<th>Feature/Comparison</th>
<th>MPC5xx / MPC5554 SPI Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>Visibility into TX and RX FIFOs for ease of debugging</td>
<td>FIFO bypass mode for low-latency updates to SPI queues</td>
</tr>
<tr>
<td>Wrap Around Operation allowing continuous transmit and receive</td>
<td>Using the SMOD and DMOD TCD fields circular buffers can be created to do the same.</td>
</tr>
<tr>
<td>Programmable transfer attributes on a per-frame basis:</td>
<td>Programmable serial frame size of 4 to 16 bits, expandable with software control</td>
</tr>
<tr>
<td>4 Programmable Peripheral Chip Select Pins, extended to 8 on the MPC561/3 however these are multiplexed with other pins.</td>
<td>Six peripheral chip selects, expandable to 64 with external demultiplexer</td>
</tr>
<tr>
<td>The QSPI allows byte, half-word, and word accesses.</td>
<td>DSPI allows byte, half-word and word accesses.</td>
</tr>
<tr>
<td>Data stored in the receive RAM is right-justified, (i.e., the least significant bit is always in the right-most bit position within the word regardless of the serial transfer length). Unused bits in a receive queue entry are set to zero by the QSPI upon completion of the individual queue entry.</td>
<td>Same</td>
</tr>
<tr>
<td>Data must be written to transmit RAM in a right-justified format. The QSPI cannot modify information in the transmit RAM.</td>
<td>Same. DSPI must be configured correctly</td>
</tr>
<tr>
<td>The CPU writes one byte of control information for each QSPI command to be executed. The QSPI cannot modify information in command RAM.</td>
<td>Command queue can be written at any time provided it is allocated to volatile memory. Both the DMA and CPU may write to a volatile command queue. Each command is 16 bits.</td>
</tr>
<tr>
<td>QSPI loop mode. LOOPQ controls feedback on the data serializer for testing.</td>
<td>Not supported</td>
</tr>
<tr>
<td>Halt QSPI. When HALT is set, the QSPI stops on a queue boundary. It remains in a defined state from which it can later be restarted.</td>
<td>Same</td>
</tr>
<tr>
<td>Master/slave mode select</td>
<td>Same</td>
</tr>
<tr>
<td>Wired-OR mode for QSPI pins. This bit controls the QSPI pins regardless of whether they are used as general-purpose outputs or as QSPI outputs, and regardless of whether the QSPI is enabled or disabled.</td>
<td>Not supported directly. However wired-or functionality can be achieved by setting the PCR[ODE,WPE] bit fields correctly.</td>
</tr>
<tr>
<td>Data transfers from 8 to 16 bits are supported.</td>
<td>Supported with different range of values.</td>
</tr>
<tr>
<td>Clock polarity. CPOL is used to determine the inactive state of the serial clock (SCK).</td>
<td>Same, but on a per frame basis instead of global.</td>
</tr>
<tr>
<td>Clock phase. CPHA determines which edge of SCK causes data to change and which edge causes data to be captured.</td>
<td>Same, but on a per frame basis instead of global.</td>
</tr>
<tr>
<td>Serial clock baud rate. The QSPI uses a modulus counter to derive the SCK baud rate from the MCU IMB3 clock. Baud rate is selected by writing a value from 2 to 255 into SPBR.</td>
<td>Supported with different range of values.</td>
</tr>
</tbody>
</table>
Conclusion

From the previous sections, it has been shown that the MPC55xx family provides flexibility for SPI communications with the DSPI module. It has also been shown that this module can facilitate the release of module pins to be used as GPIO. This in turn provides the user with flexibility to configure the pins on the MPC55xx device to suit their application.
Appendix A – Simple SPI example using the eDMA

NOTE
The example source code in these Appendices does not take care of device initialization after reset. This code is intended as main routines that can be pasted into the user’s initialization code.

```
#ifndef SPI_DMA_c
#define SPI_DMA_c

#include "mpc5554.h"
#include "typedefs.h"

extern vuint32_t DSPI_TXQUEUE[4];    // Set up a command queue for DSPI C transmit
extern vuint32_t DSPI_RXQUEUE[4];  // Set up a result queue for DSPI D

void initDSPI(void)
```

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{

****** SPI C to D using internal connections *********/

DSPI_C.MCR.R = 0x80010000; /* SPI mode DSPIC = Master PCS0=active lo*/

DSPI_C.CTAR[0].R = 0x78003255; /* FSIZE =4,CPOL=0,CPHA=0
LSBE=0 PCSSCK=0 CSSCK=3 PASC=0ASC=2PDT=0DT=5
PBR =0 BR=4 */

DSPI_D.MCR.R = 0x00010000; /* SPI mode DSPID = Slave SS0=active lo*/

DSPI_D.CTAR[0].R = 0x78003255;

SIU.DISR.R = 0x000000FC;/* DSPID inputs are taken from DSPIC o/ps
NO EXTERNAL CONNECTIONS
REQ'D*/

DSPI_C.RSER.R = 0x03000000; /* Setup TFFF to cause DMA transfer*/

DSPI_D.RSER.R = 0x00030000; /* Setup RFDF to cause DMA transfer */

}

void main (void)
{

DSPI_TXQUEUE[0] = 0x00010001; /* EOQ=0 PCS0=active Non continuos SCK Data = 1*/

DSPI_TXQUEUE[1] = 0x00010002; /* Data = 2*/

DSPI_TXQUEUE[2] = 0x00010003; /* Data = 3*/

DSPI_TXQUEUE[3] = 0x08010004; /* Data = 4, EOQ =1*/

initDMA(); /* Setup DMA */

initDSPI();

while(1)
{

}

}/**********************************************************************
*
*                           End of File
*
* *********************************************************************/

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#include "mpc5554.h"

#define DSPIA_PUSH 0xFFF90034
#define DSPIB_PUSH 0xFFF940034
#define DSPIC_PUSH 0xFFF98034
#define DSPID_PUSH 0xFFF9C034

#define DSPIA_POP 0xFFF90038
#define DSPIB_POP 0xFFF940038
#define DSPIC_POP 0xFFF980038
#define DSPID_POP 0xFFF9C0038

#define DSPIA_RXFR 0xFFF9007C
Conclusion

// ******************* Referenced Variables *******************

vuint32_t DSPI_TXQUEUE[4];    // Set up a command queue for DSPI C transmit

vuint32_t DSPI_RXQUEUE[4];  // Set up a result queue for DSPI D

// ********************** Function Prototypes **********************

void initDMA(void);

// *********************** Initialization Function ***********************

void initDMA(void)
{

// DMA Configuration Register (DMACR)
    EDMA.CR.R   = 0x0000E400;  // Group Arbitration scheme is : Fixed Priority
                        // Channel Arbitration scheme is : Fixed Priority
                        // Group 3 Priority (GRP3PRI) is : 4
                        // Group 2 Priority (GRP2PRI) is : 3
                        // Group 1 Priority (GRP1PRI) is : 2
                        // Group 0 Priority (GRP0PRI) is : 1
                        // Debug is : Disabled (0)
                        // Buffered Writes are : Enabled (1)

// DMA Enable Request Registers (DMAERQH,DMAERQL)
    EDMA.ERQRH.R   = 0x00000000;  // DMA Enable Request Register High (Channels 63-32) :
    EDMA.ERQRL.R   = 0x00000000;  // DMA Enable Request Register Low (Channels 31-0) :
                        // Clear these registers before initialising the channel TCD.
                        // Enable channels after TCDs have been initialised.
                        // Failure to do so could cause errors with a h/w triggered
                        // channel,
                        // i.e. the dma could be triggered after the ERQR bits are set
                        // and
                        // before the TCD is configured

// DMA Enable Error Interrupt Request Registers (DMAEEIH,DMAEEIL)
    EDMA.EEIRH.R   = 0x00000000;  // DMA Error Interrupt Enable Register High (Channels 32-63) :
    EDMA.EEIRL.R   = 0x00000000;  // DMA Error Interrupt Enable Register Low (Channels 0-31) :

// DMA Channel Priority Register Settings (DCHPRIn) Channels 0 - 63
    EDMA.CPR[0].R = 0x00;    // Channel 0 is Priority 1, Channel Preemption is Disabled
    EDMA.CPR[1].R = 0x01;    // Channel 1 is Priority 2, Channel Preemption is Disabled
    EDMA.CPR[2].R = 0x02;    // Channel 2 is Priority 3, Channel Preemption is Disabled
    EDMA.CPR[3].R = 0x03;    // Channel 3 is Priority 4, Channel Preemption is Disabled
    EDMA.CPR[4].R = 0x04;    // Channel 4 is Priority 5, Channel Preemption is Disabled
    EDMA.CPR[5].R = 0x05;    // Channel 5 is Priority 6, Channel Preemption is Disabled
    EDMA.CPR[6].R = 0x06;    // Channel 6 is Priority 7, Channel Preemption is Disabled

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EDMA.CPR[7].R = 0x07; // Channel 7 is Priority 8, Channel Preemption is Disabled
EDMA.CPR[8].R = 0x08; // Channel 8 is Priority 9, Channel Preemption is Disabled
EDMA.CPR[9].R = 0x09; // Channel 9 is Priority 10, Channel Preemption is Disabled
EDMA.CPR[10].R = 0x0A; // Channel 10 is Priority 11, Channel Preemption is Disabled
EDMA.CPR[11].R = 0x0B; // Channel 11 is Priority 12, Channel Preemption is Disabled
EDMA.CPR[12].R = 0x0C; // Channel 12 is Priority 13, Channel Preemption is Disabled
EDMA.CPR[13].R = 0x0D; // Channel 13 is Priority 14, Channel Preemption is Disabled
EDMA.CPR[14].R = 0x0E; // Channel 14 is Priority 15, Channel Preemption is Disabled
EDMA.CPR[15].R = 0x0F; // Channel 15 is Priority 16, Channel Preemption is Disabled
EDMA.CPR[16].R = 0x00; // Channel 16 is Priority 1, Channel Preemption is Disabled
EDMA.CPR[17].R = 0x01; // Channel 17 is Priority 2, Channel Preemption is Disabled
EDMA.CPR[18].R = 0x02; // Channel 18 is Priority 3, Channel Preemption is Disabled
EDMA.CPR[19].R = 0x03; // Channel 19 is Priority 4, Channel Preemption is Disabled
EDMA.CPR[20].R = 0x04; // Channel 20 is Priority 5, Channel Preemption is Disabled
EDMA.CPR[21].R = 0x05; // Channel 21 is Priority 6, Channel Preemption is Disabled
EDMA.CPR[22].R = 0x06; // Channel 22 is Priority 7, Channel Preemption is Disabled
EDMA.CPR[23].R = 0x07; // Channel 23 is Priority 8, Channel Preemption is Disabled
EDMA.CPR[24].R = 0x08; // Channel 24 is Priority 9, Channel Preemption is Disabled
EDMA.CPR[25].R = 0x09; // Channel 25 is Priority 10, Channel Preemption is Disabled
EDMA.CPR[26].R = 0x0A; // Channel 26 is Priority 11, Channel Preemption is Disabled
EDMA.CPR[27].R = 0x0B; // Channel 27 is Priority 12, Channel Preemption is Disabled
EDMA.CPR[28].R = 0x0C; // Channel 28 is Priority 13, Channel Preemption is Disabled
EDMA.CPR[29].R = 0x0D; // Channel 29 is Priority 13, Channel Preemption is Disabled
EDMA.CPR[30].R = 0x0E; // Channel 30 is Priority 15, Channel Preemption is Disabled
EDMA.CPR[31].R = 0x0F; // Channel 31 is Priority 16, Channel Preemption is Disabled
EDMA.CPR[32].R = 0x00; // Channel 32 is Priority 1, Channel Preemption is Disabled
EDMA.CPR[33].R = 0x01; // Channel 33 is Priority 2, Channel Preemption is Disabled
EDMA.CPR[34].R = 0x02; // Channel 34 is Priority 3, Channel Preemption is Disabled
EDMA.CPR[35].R = 0x03; // Channel 35 is Priority 4, Channel Preemption is Disabled
EDMA.CPR[36].R = 0x04; // Channel 36 is Priority 5, Channel Preemption is Disabled
EDMA.CPR[37].R = 0x05; // Channel 37 is Priority 6, Channel Preemption is Disabled
EDMA.CPR[38].R = 0x06; // Channel 38 is Priority 7, Channel Preemption is Disabled
EDMA.CPR[39].R = 0x07; // Channel 39 is Priority 8, Channel Preemption is Disabled
EDMA.CPR[40].R = 0x08; // Channel 40 is Priority 9, Channel Preemption is Disabled
EDMA.CPR[41].R = 0x09; // Channel 41 is Priority 10, Channel Preemption is Disabled
EDMA.CPR[42].R = 0x0A; // Channel 42 is Priority 11, Channel Preemption is Disabled
EDMA.CPR[43].R = 0x0B; // Channel 43 is Priority 12, Channel Preemption is Disabled
EDMA.CPR[44].R = 0x0C; // Channel 44 is Priority 13, Channel Preemption is Disabled
EDMA.CPR[45].R = 0x0D; // Channel 45 is Priority 14, Channel Preemption is Disabled
EDMA.CPR[46].R = 0x0E; // Channel 46 is Priority 15, Channel Preemption is Disabled
EDMA.CPR[47].R = 0x0F; // Channel 47 is Priority 16, Channel Preemption is Disabled
EDMA.CPR[48].R = 0x00; // Channel 48 is Priority 1, Channel Preemption is Disabled
EDMA.CPR[49].R = 0x01; // Channel 49 is Priority 2, Channel Preemption is Disabled
EDMA.CPR[50].R = 0x02; // Channel 50 is Priority 3, Channel Preemption is Disabled
EDMA.CPR[51].R = 0x03; // Channel 51 is Priority 4, Channel Preemption is Disabled
EDMA.CPR[52].R = 0x04; // Channel 52 is Priority 5, Channel Preemption is Disabled
EDMA.CPR[53].R = 0x05; // Channel 53 is Priority 6, Channel Preemption is Disabled
EDMA.CPR[54].R = 0x06; // Channel 54 is Priority 7, Channel Preemption is Disabled
EDMA.CPR[55].R = 0x07;  // Channel 55 is Priority 8, Channel Preemption is Disabled
EDMA.CPR[56].R = 0x08;  // Channel 56 is Priority 9, Channel Preemption is Disabled
EDMA.CPR[57].R = 0x09;  // Channel 57 is Priority 10, Channel Preemption is Disabled
EDMA.CPR[58].R = 0x0A;  // Channel 58 is Priority 11, Channel Preemption is Disabled
EDMA.CPR[59].R = 0x0B;  // Channel 59 is Priority 12, Channel Preemption is Disabled
EDMA.CPR[60].R = 0x0C;  // Channel 60 is Priority 13, Channel Preemption is Disabled
EDMA.CPR[61].R = 0x0D;  // Channel 61 is Priority 14, Channel Preemption is Disabled
EDMA.CPR[62].R = 0x0E;  // Channel 62 is Priority 15, Channel Preemption is Disabled
EDMA.CPR[63].R = 0x0F;  // Channel 63 is Priority 16, Channel Preemption is Disabled

// Transfer Control Descriptor for DSPI C TFFF
EDMA.TCD[14].SADDR = (vuint32_t) &DSPI_TXQUEUE[0];  // Start Address
EDMA.TCD[14].DADDR = DSPIC_PULLR;  // Destination address
EDMA.TCD[14].SMOD = 0x00;  // Source address modulo
EDMA.TCD[14].DMOD = 0x00;  // Destination address modulo
EDMA.TCD[14].DSIZE = 0x02;  // Destination transfer size : 32 Bits
EDMA.TCD[14].SSIZE = 0x02;  // Source transfer size : 32 Bits
EDMA.TCD[14].SOFF = 0x4;  // Signed source address offset
EDMA.TCD[14].NBYTES = 0x4;  // Inner "minor" byte count
EDMA.TCD[14].SLAST = 0;  // last Signed source address adjust
EDMA.TCD[14].DOFF = 0x0;  // Signed destination address offset
EDMA.TCD[14].DLAST_SGA = 0x0;  // Signed destination address adjust
EDMA.TCD[14].BITERE_LINK = 0x0;  // Channel-to-channel Linking on Minor Loop Complete
EDMA.TCD[14].BITER = 0x1;  // begining "major" iteration count
EDMA.TCD[14].CITERE_LINK = 0x0;  // Channel-to-channel Linking on Minor Loop Complete
EDMA.TCD[14].CITER = 0x1;  // Current "major" iteration count Disabled
EDMA.TCD[14].BWC = 0x00;  // Bandwidth control : No DMA Stalls
EDMA.TCD[14].MAJOR_LINKCH = 0x00;  // Major Channel number
EDMA.TCD[14].MAJOR_LINK = 0x0;  // Major Channel Link : Disabled
EDMA.TCD[14].DONE = 0x00;  // Channel Done
EDMA.TCD[14].ACTIVE = 0x00;  // Channel Active
EDMA.TCD[14].E_SG = 0x0;  // Enable Scatter/Gather : Disabled
EDMA.TCD[14].D_REQ = 0x0;  // Do NOT disable TCD When done
EDMA.TCD[14].INT_HALF = 0x0;  // Interrupt on minor loop count
EDMA.TCD[14].INT_MAJ = 0x0;  // Interrupt on major loop completion : Disabled
EDMA.TCD[14].START = 0x00;  // Explicit Channel Start bit

// Transfer Control Descriptor for DSPI D RFDF
EDMA.TCD[17].SADDR = DSPI_ID_POPR;  // Start Address
EDMA.TCD[17].DADDR = (vuint32_t) &DSPI_RXQUEUE[0];  // Destination address
EDMA.TCD[17].SMOD = 0x00;  // Source address modulo
EDMA.TCD[17].DMOD = 0x00;  // Destination address modulo
EDMA.TCD[17].DSIZE = 0x02;  // Destination transfer size : 32 Bits
EDMA.TCD[17].SSIZE = 0x02;  // Source transfer size : 32 Bits
EDMA.TCD[17].SOFF = 0;  // Signed source address offset
EDMA.TCD[17].NBYTES = 0x4; // Inner "minor" byte count
EDMA.TCD[17].SLAST = 0; // last Signed source address adjust
EDMA.TCD[17].DOFF = 4; // Signed destination address offset
EDMA.TCD[17].DLAST_SGA = 0; // Signed destination address adjust
EDMA.TCD[17].BITERE_LINK = 0x0; // Channel-to-channel Linking on Minor Loop Complete
EDMA.TCD[17].BITER = 0x1; // beginning "major" iteration count
EDMA.TCD[17].CITERE_LINK = 0x0; // Channel-to-channel Linking on Minor Loop Complete
EDMA.TCD[17].CITER=0x1; // Current "major" iteration count Disabled
EDMA.TCD[17].BWC = 0x00; // Bandwidth control : No DMA Stalls
EDMA.TCD[17].MAJORLINKCH = 0x00; // Major Channel number
EDMA.TCD[17].MAJORE_LINK = 0x0; // Major Channel Link : Disabled
EDMA.TCD[17].DONE = 0x00; // Channel Done
EDMA.TCD[17].ACTIVE = 0x00; // Channel Active
EDMA.TCD[17].E_SG = 0x0; // Enable Scatter/Gather : Disabled
EDMA.TCD[17].D_REQ = 0x0; // Do NOT disable TCD When done
EDMA.TCD[17].INT_HALF = 0x0; // Interrupt on minor loop count : Disabled
EDMA.TCD[17].INT_MAJ = 0x0; // Interrupt on major loop completion : Disabled
EDMA.TCD[17].START = 0x00; // Explicit Channel Start bit

// DMA Enable Request Registers (DMAERQH,DMAERQL)
// Enable Ch14=DSPIC TXFFF, Ch17=DSPID RFDF

EDMA.ERQRH.R = 0x00000000; // DMA Enable Request Register High (Channels 63-32) :
EDMA.ERQRL.R = 0x00024000; // DMA Enable Request Register Low (Channels 31-0):

/* ***********************************************************
 *                        End of File
 * *********************************************************** */
//************************************************************************************/
/*                                            COPYRIGHT (c) FREESCALE 2004         */
/* FILE NAME: dsitrigger                        */
/* PROJECT NAME :Copperhead(MPC5554) EVB silicon Evaluation */
/* INCLUDE FILES: MPC5554.h typedefs.h            */
/* VERSION: 0.1                                    */
/*                                            */
/*==========================================================================================*/
/*                                            */
/* DESCRIPTION: This test is used to check serial chaining of DSPIA,B,C*/
/* which requires the use of the hardware trigger. The data to be    */
/* transmitted for each module is stored in the DSPIx_ASDR register. */
/* DSPI B&C are configured to transmit 4 bits with DSPI A initialized for */
/* 8 bit. Using a debugger change the data in either DSPIB or C. This    */
/* should result on a 16 bit frame being transmitted on SOUTC. This 16 */
/* bit value is the result of concatenating 8 bits from DSPIA, 4 bits from */
/* DSPI B and 4 bits from DSPIC. The slave data for DSPIs B &C can be */
/* viewed in DSPI A Deserialisation Data Register. */
/*                                            */
/*==========================================================================================*/
/*                                            */
/* COMPILER: Diab Data VERSION: 5.1.2                                */
/*                                            */
/* AUTHOR: Steven McQuade CREATION DATE: 15/03/04 */
/* LOCATION: East Kilbride, Scotland.             */
/*                                            */
/* UPDATE HISTORY                              */
/* REV AUTHOR DATE DESCRIPTION OF CHANGE */
/* --- ----------- ------------------- */
/* 0.1 S.McQuade 14/04/04 Initial version of file */
/*                                            */
/*==========================================================================================*/

#include "mpc5554.h"
#include "typedefs.h"

void initDSPI(void)
{
    vuint32_t ADR =0;

    /***** DSI A master, B&C DSI slaves *******/
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void initPins(void) {
    
    /* Source of data is ADR*/
    DSPI_C.DSICR.B.TXSS = 1;
    /* Falling edge initiates a transfer*/
    DSPI_C.DSICR.B.TPOL = 0;
    /* Trigger enabled*/
    DSPI_C.DSICR.B.TRRE = 1;
    /* Change in Data disabled when 0*/
    DSPI_C.DSICR.B.DCONT = 0;
    /* Non continuous DSI chip select*/
    DSPI_C.DSICR.B.DSICTAS = 1;
    /* CTAR1 used for slaves*/
    DSPI_C.DSICR.B.DPCS0 = 1;
    /* USE DPCS0*/

    DSPI_A.ASDR.R = 0x12;
    /* Write alternate data*/
    DSPI_B.ASDR.R = 0x56;
    /* Write alternate data*/
    SIU.DISR.R = 0x81569400; /* short SOUT,SIN,SCK and PCS internally */
}

/***** SCKA ****/
SIU.PCR[93].B.PA = 0x3;
    /* Initialize pin assignment to primary, SCKA */
SIU.PCR[93].B.OBE = 1;
    /* Enable output buffer (SCK OBE =1 when Master and 0 when Slave) */
SIU.PCR[93].B.IBE = 1;
    /* Enable input buffer so pin can be monitored (can be set to 0 to reduce power consumption)*/
SIU.PCR[93].B.DSC = 0x3;
    /* 50pF drive strength*/

/**** SOUTC ****/
SIU.PCR[107].B.PA = 0x2;
    /* Initialize pin assignment to secondary, SOUTA */
SIU.PCR[107].B.OBE = 1;
    /* Enable output buffer as SOUTA is an output */
SIU.PCR[107].B.IBE = 1;
    /* Enable input buffer so pin can be monitored (can be set to 0 to reduce power consumption)*/
SIU.PCR[107].B.DSC = 0x3;
    /* 50pF drive strength*/

/**** PCSA0 ****/
SIU.PCR[96].B.PA = 0x3;
    /* Initialize pin assignment to primary, PCSA0 */
SIU.PCR[96].B.OBE = 1;
    /* Enable output buffer as PCSA0 is an output */
SIU.PCR[96].B.IBE = 1;
    /* Enable input buffer so pin can be monitored (can be set to 0 to reduce power consumption)*/
SIU.PCR[96].B.DSC = 0x3;
    /* 50pF drive strength*/
void main (void)
{
    initPins(); /* Initialize pins for non-GPIO assignments - DSPI */
    initDSPI();

    DSPI_C.ASDR.R = 0x0a; /* Write alternate data*/

    while(1)
    {
        /*End of code (trap)*/
    }
}

/******************************************************************************
*                                                                              *
*                              End of File                                       *
*                                                                              *
*******************************************************************************/
Appendix C – eMIOS Serialisation example

#include "mpc5554.h"
#include "typedefs.h"

#define HI 1
#define LO 0

vuint32_t CH10 =0; vuint32_t CH11 =0; vuint32_t CH12 =0; vuint32_t CH13 =0;
vuint32_t POPR =0;
void initeMIOS();
void delay();
void modifyMIOSdata();

void modifyMIOSdata(void)
{
    EMIOS.CH[10].CCR.B.EDPOL = CH10; /* EDPOL used to toggle pin value */
    EMIOS.CH[11].CCR.B.EDPOL = CH11; /* EDPOL used to toggle pin value */
    EMIOS.CH[12].CCR.B.EDPOL = CH12; /* EDPOL used to toggle pin value */
    EMIOS.CH[13].CCR.B.EDPOL = CH13; /* EDPOL used to toggle pin value */
}

void delay(void)
{
    vuint32_t a =0;
    for(a=0xFFFF;a!=0;a--)
    {
    }
}

void initeMIOS(void)
{
    EMIOS.MCR.R = 0;/* No Clocks enabled*/
    EMIOS.OUDR.R = 0;/* No update disabled*/
    EMIOS.CH[10].CADR.R = 0;/* CH10 Areg =0*/
    EMIOS.CH[10].CBDR.R = 0;/* CH10 Breg =0*/
    EMIOS.CH[11].CADR.R = 0;/* CH11 Areg =0*/
    EMIOS.CH[11].CBDR.R = 0;/* CH11 Breg =0*/
    EMIOS.CH[12].CADR.R = 0;/* CH12 Areg =0*/
    EMIOS.CH[12].CBDR.R = 0;/* CH12 Breg =0*/
    EMIOS.CH[13].CADR.R = 0;/* CH13 Areg =0*/
    EMIOS.CH[13].CBDR.R = 0;/* CH13 Breg =0*/
    EMIOS.CH[10].CCR.B.MODE = 0x1; /* Mode is General Purpose Output */
    EMIOS.CH[11].CCR.B.MODE = 0x1; /* Mode is General Purpose Output */
    EMIOS.CH[12].CCR.B.MODE = 0x1; /* Mode is General Purpose Output */
    EMIOS.CH[13].CCR.B.MODE = 0x1; /* Mode is General Purpose Output */
    EMIOS.CH[10].CCR.B.EDPOL = CH10; /* EDPOL used to toggle pin value */
EMIOS.CH[11].CCR.B.EDPOL = CH11; /* EDPOL used to toggle pin value */
EMIOS.CH[12].CCR.B.EDPOL = CH12; /* EDPOL used to toggle pin value */
EMIOS.CH[13].CCR.B.EDPOL = CH13; /* EDPOL used to toggle pin value */

void initDSPI(void)
{
    uint32_t SDR =0;

    /****** DSI D to C **********/
    DSPI_C.MCR.R = 0x00010000; /* SPI mode DSPIC = SLAVE SS0=active low*/
    DSPI_C.CTAR[0].R = 0x78003255 ;/*FSIZE=16,CPOL=0,CPHA=0
    LSBE=0 PCSSCK=0 CSSCK=3
    PASC=0ASC=2PDT=0DT=5 PBR =0 BR=4 */
    DSPI_D.MCR.R = 0x90010000;/* DSI mode DSPID = Master PCS0=active low*/
    DSPI_D.CTAR[0].R = 0x7800325 /*FSIZE=16,CPOL=0,CPHA=0
    LSBE=0 PCSSCK=0 CSSCK=3
    PASC=0ASC=2PDT=0DT=5 PBR =0 BR=4 */
    DSPI_D.DSICR.B.MTOE = 0; /* Enable multiple transfers*/
    DSPI_D.DSICR.B.MTOCNT = 0xF; /* No of SCK clocks to shift out frame. Same as no.of
    bits in frame to be shifted*/
    DSPI_D.DSICR.B.TXSS = 0; /* Source of data is SDR*/
    DSPI_D.DSICR.B.TPOL = 0; /* Falling edge initiates a transfer*/
    DSPI_D.DSICR.B.TRRE = 0; /* Trigger disabled*/
    DSPI_D.DSICR.B.CID = 1; /* Change in Data disabled when 0*/
    DSPI_D.DSICR.B.DCONT = 0; /* Non continuous DSI chip select*/
    DSPI_D.DSICR.B.DSICTAS = 0; /* CTAR0 used*/
    DSPI_D.DSICR.B.DPCS0 = 1; /* USE DPCS0*/

    SDR = DSPI_D.SDR.R; /* Read value of SDR should be valid on eMIOS CH10-13*/

    /******************************************************************************
    /* Use this line if SCK, SIN, SOUT and PCS pins have to be used.            */
    /******************************************************************************/

Using the DSPI Module on the MPC5500 Family, Rev. 0
void initPins(void) {

    /******************************************************************************/
    /******************************************************************************/
    /******************************************************************************/
    /******************************************************************************/

    SIU.DISR.R = 0x00000000; /* No serial or parallel chaining, data
                          is taken from the pins */
    //**********************************************************************************/
    // Use this line if SCK, SIN, SOUT and PCS signals are shorted internally. */
    //**********************************************************************************/

    //SIU.DISR.R = 0x0000FC00; /* DSPIC inputs are taken from DSPID o/ps*/

    }
Using the DSPI Module on the MPC5500 Family, Rev. 0

Conclusion

```c
/* Enable input buffer so pin can be monitored (can be set to 0 to reduce power consumption)*/
SIU.PCR[110].B.IBE = 1;

/* 50pF drive strength*/
SIU.PCR[110].B.DSC = 0x3;
```

/**** PCSC1 ****/

```c
/* Initialize pin assignment to secondary, PCSC1 */
SIU.PCR[102].B.PA = 0x2;

/* Enable output buffer as PCSC1 is an output */
SIU.PCR[102].B.OBE = 1;

/* Enable input buffer so pin can be monitored (can be set to 0 to reduce power consumption)*/
SIU.PCR[102].B.IBE = 1;

/* 50pF drive strength*/
SIU.PCR[102].B.DSC = 0x3;
```

/**** PCSC2 ****/

```c
/* Initialize pin assignment to secondary, PCSC2 */
SIU.PCR[103].B.PA = 0x2;

/* Enable output buffer as PCSC2 is an output */
SIU.PCR[103].B.OBE = 1;

/* Enable input buffer so pin can be monitored (can be set to 0 to reduce power consumption)*/
SIU.PCR[103].B.IBE = 1;

/* 50pF drive strength*/
SIU.PCR[103].B.DSC = 0x3;
```

/**** PCSC3 ****/

```c
/* Initialize pin assignment to secondary, PCSC3 */
SIU.PCR[85].B.PA = 0x2;

/* Enable output buffer as PCSC3 is an output */
SIU.PCR[85].B.OBE = 1;

/* Enable input buffer so pin can be monitored (can be set to 0 to reduce power consumption)*/
SIU.PCR[85].B.IBE = 1;

/* 50pF drive strength*/
SIU.PCR[85].B.DSC = 0x3;
```

/**** PCSC4 ****/

```c
/* Initialize pin assignment to secondary, PCSC4 */
SIU.PCR[86].B.PA = 0x2;

/* Enable output buffer as PCSC4 is an output */
SIU.PCR[86].B.OBE = 1;

/* Enable input buffer so pin can be monitored (can be set to 0 to reduce power consumption)*/
SIU.PCR[86].B.IBE = 1;

/* 50pF drive strength*/
SIU.PCR[86].B.DSC = 0x3;
```

/**** PCSC5 ****/

```c
/* Initialize pin assignment to secondary, PCSA5 */
SIU.PCR[104].B.PA = 0x2;

/* Enable output buffer as PCSA0 is an output */
SIU.PCR[104].B.OBE = 1;

/* Enable input buffer so pin can be monitored (can be set to 0 to reduce power consumption)*/
SIU.PCR[104].B.IBE = 1;

/* 50pF drive strength*/
SIU.PCR[104].B.DSC = 0x3;
```

*********************************************************************************/

/****************************        DSPID (SLAVE)                      *****************************/

/**** SCKD ****/
Using the DSPI Module on the MPC5500 Family, Rev. 0

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Conclusion

SIU.PCR[98].B.PA = 0x2; /* Initialize pin assignment to secondary, SCKD */
SIU.PCR[98].B.OBE = 1; /* disable output buffer (SCK OBE = 1 when Master and 0 when Slave) */
SIU.PCR[98].B.IBE = 1; /* Enable input buffer so pin can be monitored (can be set to 0 to reduce power consumption) */
SIU.PCR[98].B.DSC = 0x3; /* 50pF drive strength */

/**** SIND ****/

SIU.PCR[99].B.PA = 0x2; /* Initialize pin assignment to secondary, SIND */
SIU.PCR[99].B.OBE = 0; /* Disable output buffer as SINA is an input */
SIU.PCR[99].B.IBE = 1; /* Enable input buffer so pin can be monitored (can be set to 0 to reduce power consumption) */
SIU.PCR[99].B.DSC = 0x3; /* 50pF drive strength */

/**** SOUTD ****/

SIU.PCR[100].B.PA = 0x2; /* Initialize pin assignment to secondary, SOUTD */
SIU.PCR[100].B.OBE = 1; /* Enable output buffer as SOUTD is an output */
SIU.PCR[100].B.IBE = 1; /* Enable input buffer so pin can be monitored (can be set to 0 to reduce power consumption) */
SIU.PCR[100].B.DSC = 0x3; /* 50pF drive strength */

/**** PCSD0 ****/

SIU.PCR[106].B.PA = 0x2; /* Initialize pin assignment to secondary, PCSD0 */
SIU.PCR[106].B.OBE = 1; /* Disable output buffer as PCSB0 is an input when SS */
SIU.PCR[106].B.IBE = 1; /* Enable input buffer so pin can be SS */
SIU.PCR[106].B.DSC = 0x3; /* 50pF drive strength */

/**** PCSD1 ****/

SIU.PCR[91].B.PA = 0x2; /* Initialize pin assignment to secondary, PCSD1 */
SIU.PCR[91].B.OBE = 1; /* Enable output buffer as PCSD1 is an output */
SIU.PCR[91].B.IBE = 1; /* Enable input buffer so pin can be monitored (can be set to 0 to reduce power consumption) */
SIU.PCR[91].B.DSC = 0x3; /* 50pF drive strength */

/**** PCSD2 ****/

SIU.PCR[96].B.PA = 0x2; /* Initialize pin assignment to secondary, PCSD2 */
SIU.PCR[96].B.OBE = 1; /* Enable output buffer as PCSD2 is an output */
SIU.PCR[96].B.IBE = 1; /* Enable input buffer so pin can be monitored (can be set to 0 to reduce power consumption) */
SIU.PCR[96].B.DSC = 0x3; /* 50pF drive strength */

/**** PCSD3 ****/
Conclusion

```c
#define __上级__

void main (void)
{

    initPins();  /* Initialize pins for non-GPIO assignments - DSPI */
    initMOS();   /* Setup DMA */
    initDSPI();  

    while(1)
    {
        modifyMOSdata();
        POPR = DSPI.C.POPR.R;
    }
}
/* **********************************************************************/
/*                           End of File                               */
/* ***********************************************************************/
```

Using the DSPI Module on the MPC5500 Family, Rev. 0

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Appendix D – SIU external interrupt deserialisation example

#include "mpc5554.h"
#include "typedefs.h"
extern void initDMA();
void init_ext_int(void);
void IRQISR(void);
extern void IVOR4Handler (void);

asm void initExcep(void) {
    lis r0, 0x4000 ; IVPR = address of start of L2SRAM

Using the DSPI Module on the MPC5500 Family, Rev. 0
mtIVPRr0
lis r0, IVOR4Handler@h ;IVOR4 = address of handler
ori r0, r0, IVOR4Handler@l
mtIVOR4r0
}

void initINTC(void) {
    INTC.MCR.B.HVEN = 0; /* Initialize INTC for software vector mode */
    INTC.MCR.B.VTES = 0; /* Use the default vector table entry offsets of 4 bytes */
    INTC.IACKR.R = 0x40000000; /* Set INTC Vector table base address to start of L2SRAM */
}

void initDSPI(void) {

    /**************************************************************************
    /****** SPIA to DSI B ***********/
    /**************************************************************************

    DSPI_A.MCR.R = 0x80010000;/* SPI mode DSPIA = Master, PCS0=active lo*/
    DSPI_A.CTAR[0].R = 0x78003255;/* FSIZE =16,CPOL=0,CPHA=0 LSBE=0
                             PCSSCK=0 CSSCK=3 PASC=0ASC=2PDT=0DT=5
                             PBR =0 BR=4 */

    DSPI_B.MCR.R = 0x10010000;/* DSI mode DSPIB = Slave, PCS0=active lo*/
    DSPI_B.CTAR[1].R = 0x78003255;/* FSIZE =16,CPOL=0,CPHA=0 LSBE=0
                             PCSSCK=0 CSSCK=3 PASC=0ASC=2PDT=0DT=5
                             PBR =0 BR=4 */

    /* When config'd as a DSI slave CTAR1 must be used.*/
    /* DSI slave means that the rx'd data is transfered to the DSPI
    i/p's e.g. eMIOS and eTPU channels*/

    DSPI_B.DSICR.B.MTOE = 0; /* Enable multiple transfers*/
    DSPI_B.DSICR.B.MTOCNT = 0xF; /* No of SCK clocks to shift out frame. Same as no.of bits in
    frame to be shifted*/
    DSPI_B.DSICR.B.TXSS = 0; /* Source of data is SDR*/
    DSPI_B.DSICR.B.TPOL = 0; /* Falling edge initiates a transfer*/
    DSPI_B.DSICR.B.TRRE = 0; /* Trigger disabled*/
    DSPI_B.DSICR.B.CID = 0; /* Change in Data disabled when 0*/
    DSPI_B.DSICR.B.DCONT = 0; /* Non continuous DSI chip select*/
    DSPI_B.DSICR.B.DSICTAS = 0; /* CTAR0 used*/
    DSPI_B.DSICR.B.DPCS0 = 1; /* USE DPCS0*/

    SIU.DISR.R = 0x00540000; /* DSPIB inputs taken from DSPIA internally */
    /* No need to connect these signals on the board*/

Using the DSPI Module on the MPC5500 Family, Rev. 0
void enableIrq(void) {
    INTC.CPR.B.PRI = 0; /* Ensure INTC's current priority is 0 */
    asm(" wrteei 1"); /* Enable external interrupts */
}

void init_ext_int(void)
{
    SIU.EISR.R = 0x00000004; /*configure mux for IRQ1 driven from DSPIB1*/
    INTC.PSR[47].R = 1; /* IRQ1 priority = 1 */
    SIU.DIRSR.R = 0x00000000; /*select interrupt request*/
    SIU.DIRER.R = 0x00000002; /*enable interrupt request*/
    SIU.IREER.R = 0x00000002; /*enable interrupt request on rising edge*/
    SIU.IFEER.R = 0x00000002; /*enable interrupt request on falling edge*/
}

void main (void) {
    int i = 0; /* Dummy idle counter */
    initExcep(); /* Initialize exceptions: load IVPR only for this example */
    initINTC(); /* Initialize INTC for hardware vector mode */
    initDSPI(); /* Initialize DSPI*/
    init_ext_int();
    enableIrq(); /* Ensure INTC current priority=0 & enable IRQ */
    DSPI_A.PUSHR.R = 2; /*Trigger the interrupt*/
    while (1) { i++; }
    /* Loop forever */
}

void IRQISR(void) {
    if(SIU.EISR.B.EIF1 == 1)
    {
        SIU.EISR.B.EIF1 = 0;
    }
}
NOTE

All of the above source code is for example use only. Freescale does not accept liability for use of this code in the user’s application.
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