32 kHz Oscillator Start-up Time and POR Pulse Width Considerations
For i.MX Applications Processors with ARM920T

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1 Abstract

The POR (power-on reset) pulse into the i.MX series of Applications Processors must be of sufficient duration to ensure proper initialization. For most applications, the cold start-up time is not critical and the data sheet recommendations can be used. However, for those applications where cold start-up time is a consideration, this document describes a method for determining the minimum allowable POR pulse width. Supply voltage and ambient temperature effects are shown. Part-to-part variation is explored.

At the time of publication, this document applied to the following devices:

- MC9328MX1
- MC9328MXL
- MC9328MXS

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2 Introduction

The POR minimum pulse width is dependent on the 32 kHz or 32.768 kHz oscillator start-up time. This start-up time is challenging to measure due to the loading impact of probes on the crystal oscillator. This loading can adversely affect start-up time.

Therefore, a non-invasive method is needed to determine start-up time without loading the crystal circuit. This paper uses an indirect measurement approach. That is, observation of signals which are dependent on the crystal oscillator without impacting the oscillator itself.

3 Reset Module Overview

The reset module controls and distributes all of the system reset signals used by the i.MX processor and external components. A simplified block diagram of the module is shown in Figure 1. For this paper, the signals of most interest are the POR input and HRESET, which is routed off-chip as RESET_OUT.

3.1 POR Input

The power-on reset (POR) input is a positive logic level input. That is, it is asserted with a logic high voltage. A suggested POR circuit is shown in Figure 2.

Assume capacitor C is initially discharged. On power up the output of Schmitt-trigger inverter U is a high voltage, which asserts POR. With power continually applied, the output of the inverter goes low after a time interval determined by the RC network.

Bleeder diode D improves the circuit performance by providing a quick discharge path for the capacitor upon power down. Thus, recovery time for the circuit is improved. Without the diode, the capacitor has a longer discharge time through the resistor and POR may not be activated when power is momentarily
interrupted. The diode may be either a standard silicon diode or Schottky diode, with the latter offering improved performance by discharging the circuit more quickly to a lower voltage.

![POR Circuit Diagram](image.png)

**Figure 2. External POR Circuit**

### 3.2 Crystal Oscillator

The oscillator is extremely low-power, consuming about 10 µA. The circuit's performance is impacted by stray resistance, capacitance, and inductance. Thus, measurement of the circuit by probing its nodes is not advisable. In some cases, placing a probe on the circuit prevents the oscillator from starting.

Either a 32 kHz or 32.768 kHz crystal may be used with the i.MX processors that use the ARM920T core.

### 3.3 Timer, Stretcher, and Outputs

From Figure 1, housekeeping is done by the 300 ms counter which times out the delay of the internal RESET_POR that feeds the stretcher circuits. The 14-cycle stretcher output feeds the synchronization logic. This logic generates HRESET, which is buffered and sent off-chip as RESET_OUT.

Equally important, however not of direct interest for this paper, are the other initialization signals shown in Figure 1.

### 3.4 Timing Relationship

Figure 3 shows the timing relationship between the two signals that are of primary concern for this application note: POR and RESET_OUT. When functioning properly, there is a propagation delay of 300 ms + 14 periods of the 32 kHz oscillator from the falling edge of POR to the rising edge of RESET_OUT. A calculation of the propagation delay is shown in the following formulas. The 300 ms counter divides by 9600.

- Utilizing a 32 kHz external crystal: \((9600 + 14) / 32000 = 300.4\) ms
- Utilizing a 32.768 kHz external crystal: \((9600 + 14) / 32768 = 293.4\) ms
4 Graphical Analysis Approach

The minimum allowable POR pulse width depends on the oscillator start-up time. However, the crystal oscillator start-up cannot be conveniently measured because placing a probe on the oscillator nodes affects performance. This particular oscillator is a very low-power circuit and stray impedances must be minimized. Adding capacitance, such as from an oscilloscope probe, affects oscillator performance.

Therefore, the minimum allowable POR pulse width is best determined using an indirect measurement. An analysis of a graph of the POR Pulse width versus the \( \text{RESET}_{\text{OUT}} \) delay is used to determine the critical POR pulse width.

4.1 Pass/Fail Criteria

A “pass” is considered when the POR pulse width results in a POR to \( \text{RESET}_{\text{OUT}} \) propagation delay of 300.4 ms with a 32 kHz crystal or 293.4 ms with a 32.768 kHz crystal. A “fail” occurs when the propagation delay is longer than these intervals.

The reason for the failure is as follows.

Immediately after power up, oscillator waveform CLK32 begins increasing in amplitude as depicted in Figure 3. This is known as an envelope. Until the envelope has sufficient amplitude to cause the 300 ms counter to increment, the counter is frozen. A certain period of time later, when the envelope has sufficient amplitude, the counter can increment if enabled by the negation of POR.
When asserted, the POR signal keeps the 300 ms counter initialized (inhibits it from incrementing). When POR is negated, the counter is enabled. If the POR pulse is too short, the counter is enabled too soon, and does not increment due to insufficient amplitude of the oscillator. However, the envelope eventually builds up sufficiently and causes the counter to increment. Thus, when the POR pulse width is too narrow, the delay from POR to \texttt{RESET\_OUT} is longer than it should be. Again, this is caused by the 300 ms counter beginning its time-out too late; i.e., not immediately following the POR falling edge.

If the 300 ms counter does not time out properly, the various reset signals generated by the Reset Module may not initialize the chip properly.

### 4.2 Analysis Platforms

Data was collected using a M9328MXLADS board, a M9328MX1ADS board, and an evaluation board (with a socket). All boards were populated with 32 kHz crystals sourced by Technical Crystal Ltd.\(^1\) (part number 32KFGB-26).

The POR pulse width was varied using a resistor substitution box for the resistor in the external POR circuit. Refer to Figure 2.

### 5 Measurement Results

Measurements were taken using an oscilloscope running at 500 samples per second. Therefore, measurements are accurate to ±2 ms.

#### 5.1 Pass/Fail Examples

Figure 4 on page 6 displays a passing condition with a POR pulse width of 240 ms. The POR falling edge to \texttt{RESET\_OUT} rising edge is 300 ms.

Figure 5 on page 6 displays a failing condition with a POR pulse width of 150 ms. The POR falling edge to \texttt{RESET\_OUT} rising edge is more than 300 ms.

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\(^1\) Freescale Semiconductor cannot recommend one supplier over another and in no way suggests that this is the only crystal supplier.
Measurement Results

Figure 4. Sufficient POR Pulse Width

Figure 5. Insufficient POR Pulse Width

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5.2 Supply Voltage Effect

Figure 6 shows data collected at 25°C on a board with no socket. The three curves illustrate performance with AVDD supply voltages of 1.7, 2.5, and 3.3 V.

Interpreting the graph is straightforward. Note the breakpoint at ~300 ms for the 1.7 V curve. This is the critical POR pulse width for the stated condition.

Fastest start-up, with a commensurate shorter allowable POR pulse width, is achieved at highest supply voltage.

![Figure 6. Variation with Supply Voltage at 25°C](image)

5.3 Temperature Effect

Figure 7 and Figure 8 on page 8 show data collected at a fixed supply of approximately 3.2 V on two boards with no socket. The three curves illustrate performance at ambient temperatures of −30°C, 25°C, and 85°C. Fastest start-up, with a resulting shorter POR pulse width, is achieved at lowest temperature.
Measurement Results

**Figure 7.** POR Pulse Width Effect over Temperature, Part A (Without Socket)

**Figure 8.** POR Pulse Width Effect over Temperature, Part B (Without Socket)

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5.4 Part-to-Part Variation

Figure 9 shows data collected at 25°C with a supply of approximately 3.2 V on a board with a socket. The 12 curves illustrate performance of 12 parts. These i.MX1 and i.MXL parts were random samples from seven date codes spanning over one year of production.

Note that the socket added stray impedance that slowed down the oscillator start-up time, resulting in longer required minimum POR pulse width. However, the data was taken to show the relative variation from part-to-part, not an absolute number as in the previous figures.

![Figure 9. Part-to-Part Variation at 25°C (With Socket)]

5.5 Improvement with Kick-Start

Figure 10 on page 10 shows an improvement using an oscillator kick-start circuit. This data was collected on a board without a socket.
The kick-start circuit is connected to the processor as illustrated in Figure 11. The oscillator circuit itself is not altered. The kick-start circuit drives the processor’s oscillator power supply connection (AVDD1).

Detail of the circuit used for evaluation purposes is shown in Figure 12. Improvements to make this circuit more robust and reduce board area are described later in this section. The kick-start circuit consists of a ring oscillator formed by NAND gates A, B, and C. This oscillator starts up much quicker than the 32 kHz oscillator of the processor and runs in the MHz range. Because of the quick start-up, the kick-start is able
to aid starting the slower 32 kHz oscillator. The ring oscillator output drives the 74HC4020 counter’s clock input. The counter’s Q11 output is sent to the AVDD1 processor supply connection via the 74AC04. Q14 enables the ring oscillator for a few milliseconds at power up as determined by reset circuit R1-C1. As seen in Figure 13, with R1 = 3.6 kΩ the test circuit toggled the AVDD1 power connection several times within the first 2 ms following power up. Toggling was halted by Q14 negating Enable. D1 is a bleeder diode that improves recovery time of the circuit if power is momentarily interrupted. D1 may be either a standard silicon diode or Schottky diode, with the latter offering improved performance by discharging the circuit more quickly to a lower voltage.

**Figure 12. Kick-Start Circuit Used for Evaluation**
Design Considerations

The oscillator of the i.MX processors only consumes ~10 µA. Therefore, the 74AC04 inverter can supply sufficient current with minimal voltage drop.

To facilitate production and provide design margin, a 74HC240 should be considered to replace the 74HC00 quad NAND gate as shown in Figure 14. Seven of the inverters of this device are wired as a ring oscillator. The seven inverters oscillate at a lower frequency than the three NAND gates of Figure 12. This gives margin to the maximum rated frequency of the 74HC4020 counter.

![Figure 14. Kick-Start Circuit with Improved Design Margin](image)

One of the negative-logic enable inputs of the 74HC240 inverting buffers is directly connected to Q14. The four 10 kΩ resistors are included to prevent the associated outputs from floating when OE1 is negated by Q14.

To save board space and reduce voltage drop to AVDD1, the 74AC04 inverter in Figure 12 could be replaced with a single-gate device, such as a Fairchild NC7SZ04 in Figure 14. Per the ‘7SZ04 data sheet, the worst-case output voltage drop is 0.1 V from the upper supply rail at 100 µA. This indicates a worst-case on-resistance of 0.1 V / 100 µA or 1 kΩ. Therefore, at 10 µA, the drop should be < 10 mV.

6 Design Considerations

6.1 Evaluating a Board Design

For systems with critical cold start-up times, the circuit board with its crystal should be evaluated. Data should be collected, graphed, and analyzed as illustrated in this paper.

The system designer must decide on the design margin for the POR pulse width. Margin should allow for the i.MX processor part-to-part variation, crystal variation, temperature effects, and supply voltage variation.

This paper is meant as a procedural guide to aid analysis of a system.

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1. Freescale Semiconductor cannot recommend one supplier over another and in no way suggests that this is the only supplier of a single-gate device.
6.2 **Tips for Minimizing POR Pulse Width**

Mount the crystal and ancillary components close to the associated i.MX processor contacts.

Do not use a socket for the i.MX chip or the crystal.

Minimize the use of vias in the connection path from the i.MX chip to the crystal and ancillary components.

Use a supply voltage for AVDD on the upper end of the range, for example: 3.2 V ±0.1 V.

Be aware of the negative effects of higher ambient temperatures.

If using the kick-start circuit, adjust R1 such that the AVDD1 processor supply connection has several excursions past 1.7 V as shown in **Figure 13**.

7 **References**

7.1 **Freescale Semiconductor Documents**

The following documents provide a complete description of the i.MX processors and are necessary to design properly with the devices. The following documents are helpful when used in conjunction with this application note.

*MC9328MX1 Data Sheet* (order number MC9328MX1/D)
*MC9328MXL Data Sheet* (order number MC9328MXL/D)
*MC9328MXS Data Sheet* (order number MC9328MXS/D)
*MC9328MX1 Reference Manual* (order number MC9328MX1RM/D)
*MC9328MXL Reference Manual* (order number MC9328MXLRM/D)
*MC9328MXS Reference Manual* (order number MC9328MXSRM/D)
*M9328MX1_L_ADS_V2_0 ADS Schematics and Orcad File*
*Bill of Materials B11021_I*, Bill of material for the *MC9328MXL*

The Freescale manuals are available on the Freescale Semiconductors Web site at http://www.freescale.com/imx. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered.

7.2 **Documents from Other Suppliers**

*NC7SZ04 TinyLogic® UHS Inverter Data Sheet*, DS012163 (Fairchild Semiconductor™, August 2004)
*MC74HC00A Quad 2-input NAND gate Data Sheet*, (ON Semiconductor®, Dec. 2004)
*74AC04 • 74ACT04 Hex Inverter Data Sheet*, DS009913 (Fairchild Semiconductor, 1999)
*MC74HC240A Octal 3-State Inverting Buffer/Line Driver/Line Receiver Data Sheet*, (ON Semiconductor, May 2000)
*MC74HC4020A 14-Stage Binary Ripple Counter*, (ON Semiconductor, Sep. 2001)

The data sheets are available and may be downloaded directly from the manufacturer’s Web site.
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