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MMM6035 Integrated Power Controller Features

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1 Introduction

This application note describes the power controller features integrated in the MMM6035 power amplifier module.

In multiple access radio systems, the RF power controller is used to minimize the transmit power required by the handset but still maintain quality radio links. The RF power on and off switching must also be tightly controlled to avoid splattering the signal into adjacent channels.

The power controller combines excellent RF power control with tight RF power switching while maintaining sufficient margins on transmitted RF output power parameters.

Contents

2 MMM6035 Device Overview

The MMM6035 quad-band GPRS power amplifier module (PAM) is designed in a low profile (1mm), compact form factor (6mm x6 mm) for quad band cellular handsets. The PAM also supports Class 12 GPRS multi-slot operation.

The module consists of two separated line-ups for GSM850/900 and DCS1800 /PCS1900, impedance matching circuitry for 50 ohm input and output impedances and integrated power controller based on drain supply voltage approach. PA and controller dies are mounted on an HDI substrate. The assembly is encapsulated with plastic overmold. The MMM6035 contains band select circuitry to select GSM (logic 0) or DCS/PCS (logic 1) as determined from the band select signal (LB_HB). The analog power control (VRAMP) controls the levels of output power. The TX_EN input allows turn-on or turn off of the integrated power control IC.

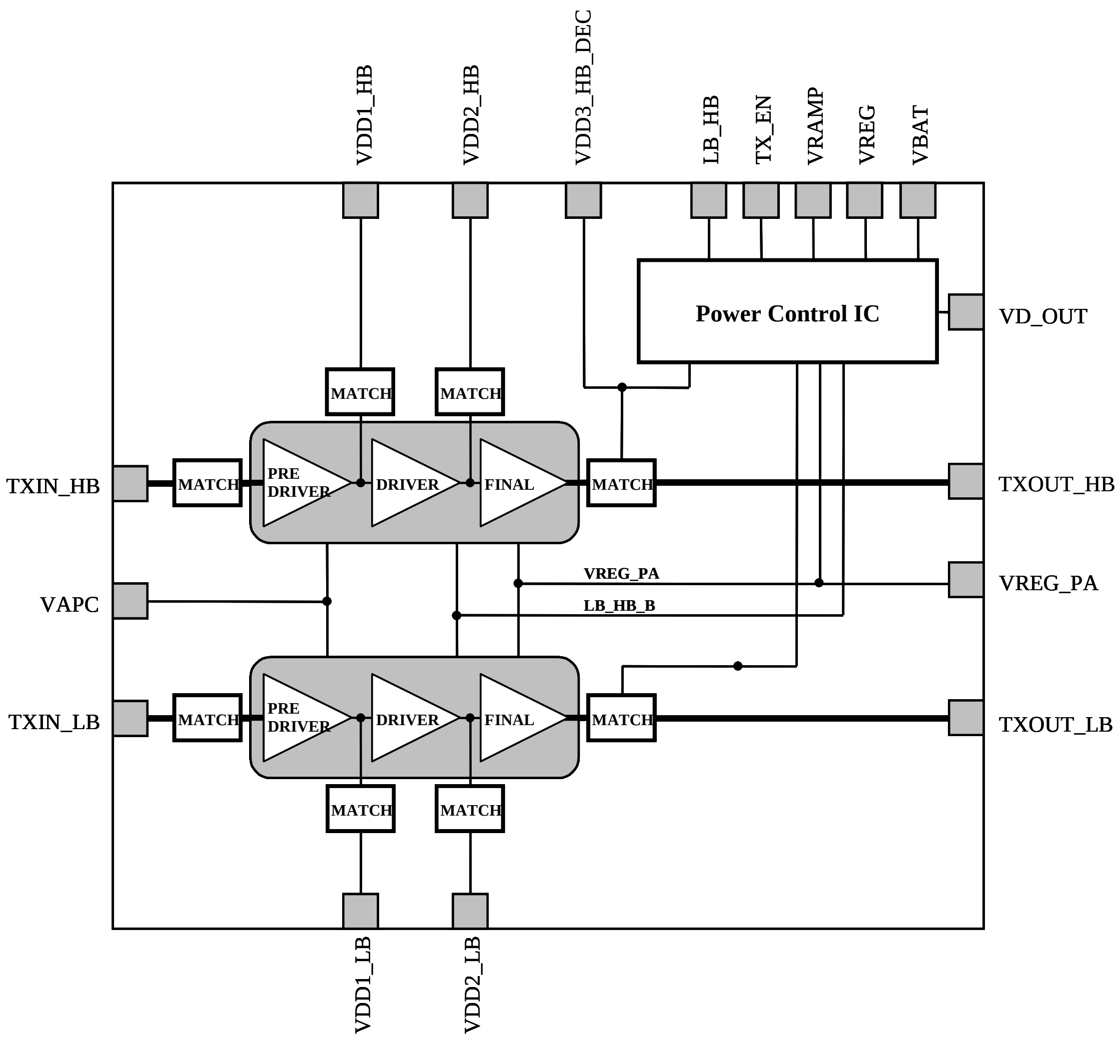

Figure 1. MMM6035 Functional Block Diagram

3 Power Control Overview

As shown in Figure 2, MMM6035 power control is accomplished using a drain supply voltage control technique that requires a P-channel MOSFET and an Operational Amplifier to control the supply voltage going to the PA (VD_OUT).

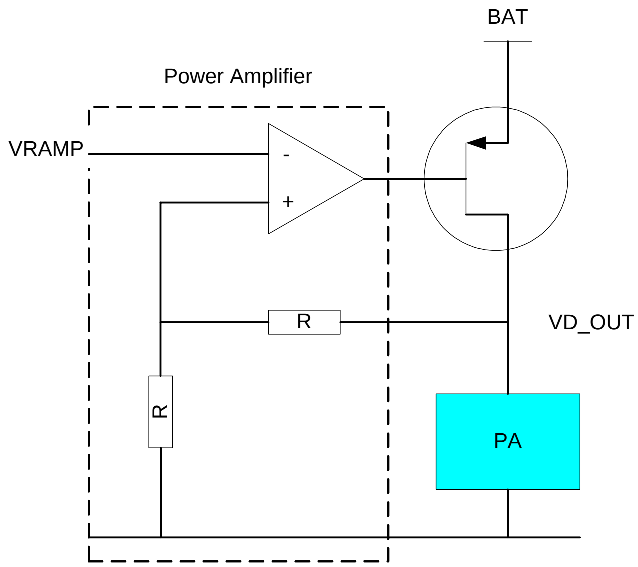

Figure 2. Drain Supply Voltage Control Technique

For square law devices such as the pHEMT FETs used in the MMM6035, the RF output power is proportional to the square of the supply voltage. Because the supply voltage is directly proportional to the control voltage (VRAMP), the transfer curve between the RF output power and the control voltage can be readily calculated. If users know the transfer curve, then handset power calibration is less complex.

4 Power Control Calibration Procedure

As already stated and shown in Figure 2, power control is accomplished using a drain supply voltage control technique. (Pout targeted vs. Pout measured) The power control calibration procedure is required to derive the numbers used in the drain supply voltage control technique. The power control calibration procedure is accomplished using two points. The procedure first requires the measurement of output power (Po) calibration points at two values, VRAMP(1) and VRAMP(2). Figure 3 shows these points after they were converted and then plotted on the RMS RF output voltage (V_{RF}) against the control voltage (VRAMP) characteristic. As a reminder:

$V_{RF} = 10^{(Po-13)/20}$

Where Po is expressed in dBm under 50 ohm load and V_{RF} is Vrms. Using these points, the estimated VRAMP voltage VRAMP(E) can be calculated for any desired output power level. In order to meet the transmitted power level versus time requirement of the GSM05.05 Specification at the lowest power level, it is also necessary to determine the VRAMP pedestal voltage (see Figure 3 and Figure 4) required to reach an acceptable power level when the controller section feedback loop has stabilized after wake-up.

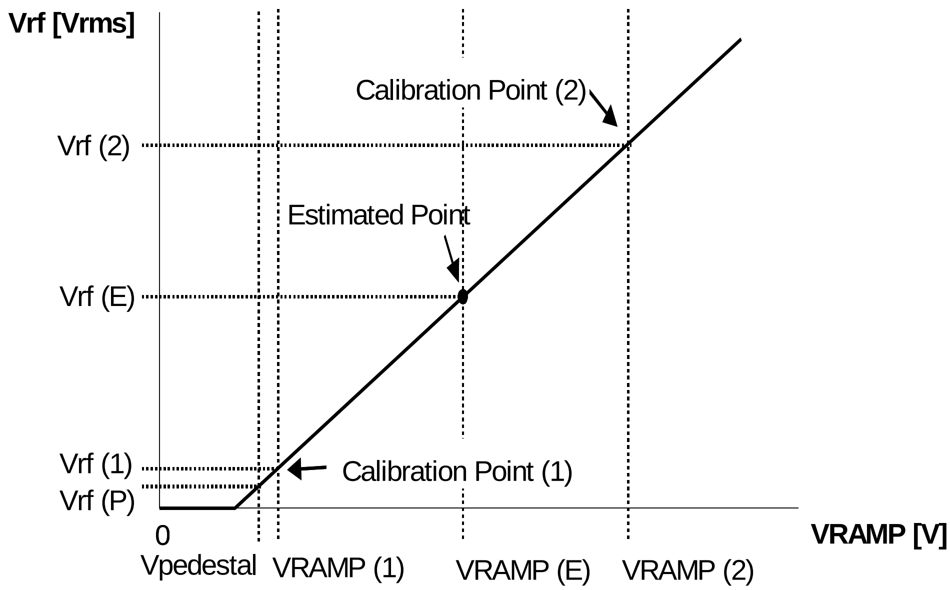

Figure 3. Vrf Versus VRAMP Characteristics

The calibration points $V_{RF}(1)$ and $V_{RF}(2)$ are each measured by forcing VRAMP levels of VRAMP(1) and VRAMP(2) respectively. The estimated VRAMP level for the required RF output voltage $V_{RF}(E)$ is then calculated from the following equation:

Eqn. 1

$$\mathrm{Vramp(E)} = \frac{\mathrm{Vramp(2)} \times [\mathrm{Vrf(E)} - \mathrm{Vrf(1)}] + \mathrm{Vramp(1)} \times [\mathrm{Vrf(2)} - \mathrm{Vrf(E)}]}{\mathrm{Vrf(2)} - \mathrm{Vrf(1)}}$$

In a similar way, Vpedestal is calculated using the following equation:

Eqn. 2

$$\mathrm{Vpedestal} = \frac{\mathrm{VRAMP(2)} \times [\mathrm{Vrf(P)} - \mathrm{Vrf(1)}] + \mathrm{VRAMP(1)} \times [\mathrm{Vrf(2)} - \mathrm{Vrf(P)}]}{\mathrm{Vrf(2)} - \mathrm{Vrf(1)}}$$

Vpedestal must be estimated in order to get Po = Pomin - 5dB.

The MMM6035 has been validated and demonstrates good output power predictability using this calibration procedure. Some of these results are shown Table 1.

Calibration Conditions:

Frequency=1810MHz

Input power at PA=3dBm, Battery voltage Vbat=3.5V

Calibration Points:

VRAMP1=0.3V, VRAMP2=1.5V

Insertion Losses Between PA and Antenna:

HB_IL=1.5dB

Calibration Results:

Voffset=0.181V

Vpedestal=0.209V

Table 1. Error on Predicted Power Results

Power Control Level [PCL]	pout_target at antenna [dBm]	pout_target at PA output [dBm]	VRAMP_computed [V]	pout_meas at PA output [dBm]	Error_Pout [dB]
15	+0	+1.5	0.231	+1.91	+0.41
14	+2	+3.5	0.244	+3.94	+0.44
13	+4	+5.5	0.260	+5.69	+0.19
12	+6	+7.5	0.281	+7.37	-0.13
11	+8	+9.5	0.307	+9.54	+0.04
10	+10	+11.5	0.340	+11.58	+0.08
9	+12	+13.5	0.381	+13.47	-0.03
8	+14	+15.5	0.433	+15.61	+0.11
7	+16	+17.5	0.498	+17.62	+0.12
6	+18	+19.5	0.580	+19.58	+0.08
5	+20	+21.5	0.683	+21.57	+0.07
4	+22	+23.5	0.813	+23.62	+0.12
3	+24	+25.5	0.977	+25.61	+0.11
2	+26	+27.5	1.183	+27.58	+0.08
1	+28	+29.5	1.443	+29.57	+0.07
0	+30	+31.5	1.769	+31.46	-0.04

5 Switching Spurious Minimization

As already stated, the rise and the fall time of the burst signal must be tightly controlled to meet spurious requirements into adjacent channels. Under specific conditions, for example, when a cell phone is far away from the base station, maximum RF output power would be required with minimum battery voltage available. In that case, the power MOSFET goes into its linear region and provides a distorted output signal. This distorted response of the loop turns into switching spurious noise in adjacent channels.

To avoid distorting the output, users should limit the input control signal and then the maximum output power available would not be transmitted.

The MMM6035 prevents degradation of switching transients, regardless of battery voltage, by use of an internal anti-saturation detection feature. The main objective of this block is to maintain the RF output power ramp within the power versus time mask while keeping acceptable spectral limits at specified offset frequencies.

The anti-saturation detection feature is implemented as a feedback loop inside the power control loop, which detects when the PMOS goes into the linear region and reduces VRAMP to maintain the pass device in its saturation region, even under low battery voltage conditions.

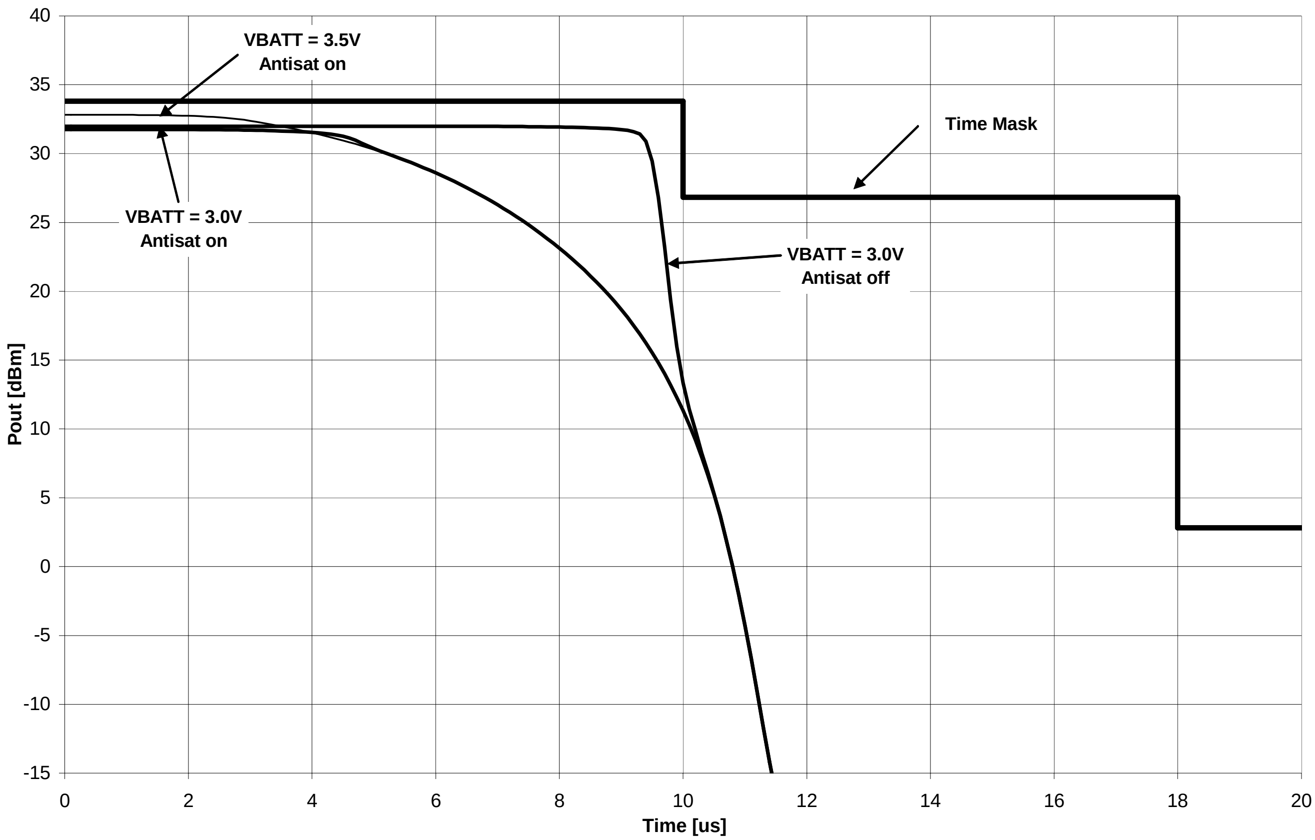

Figure 4. Anti-saturation Detection

6 MMM6035 Circuit Board

The MMM6035 and the antenna switchplexer module LMSP33QA-321 from Murata is selected as a Front End Module (FEM) power amplifier solution inside i250-22 platform. The fact that the power control is integrated inside the PA module as well as first step of the output matching reduces the external component counts and the overall size of the solution as shown in Figure 5.

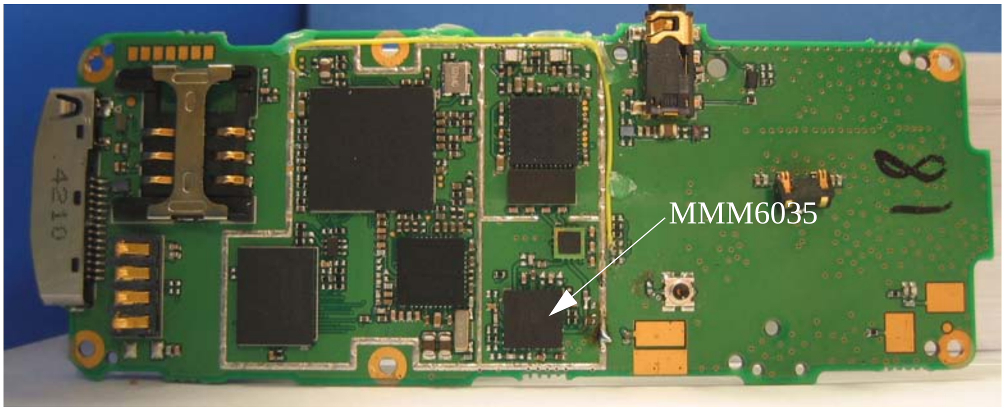

Figure 5. i250-22 Circuit Board

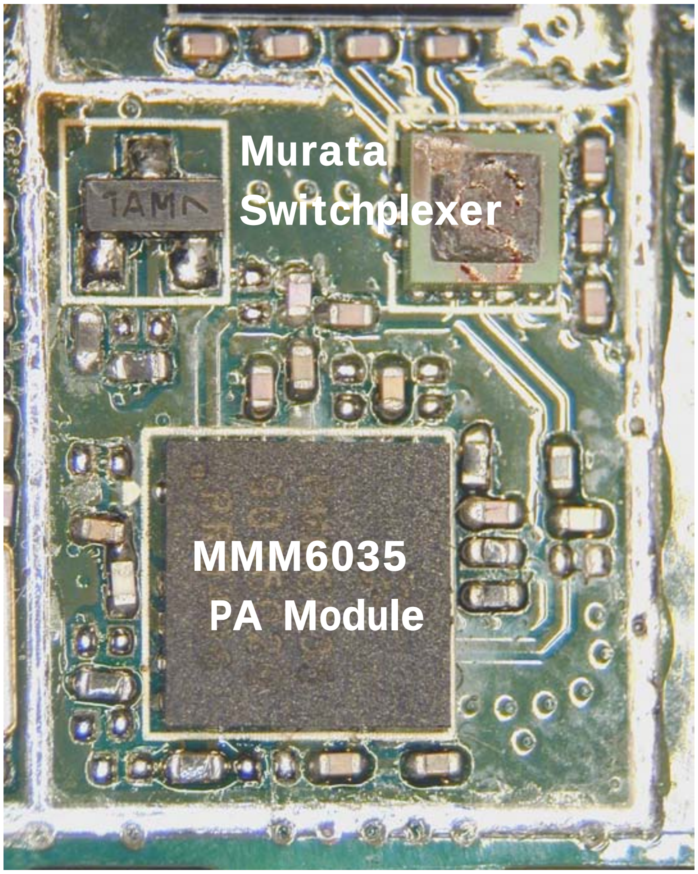

Figure 6. Zoomed in View of FEM PA

7 System Validation

To meet the GSM power versus time mask and switching transient requirements, the MMM6035 must be provided a specific ramp profile on the VRAMP input, as well as proper timing on digital control signals used by the control loop circuitry as shown on Figure 7.

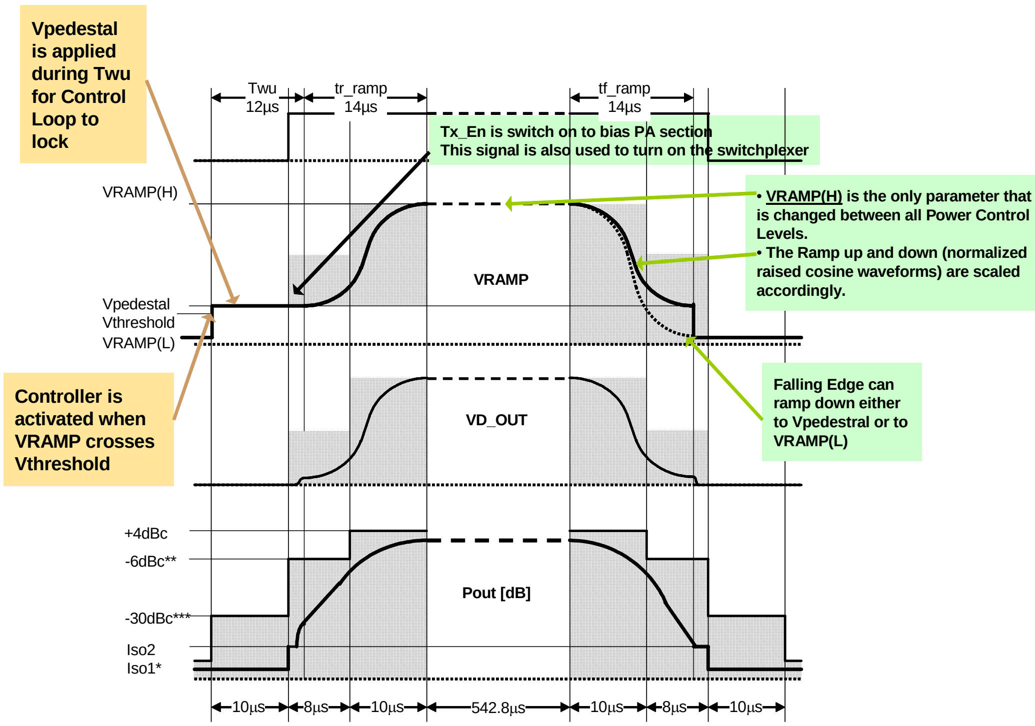

Figure 7. Timing Diagram

1 Iso1[dBm] = noise floor when VRAMP and TX_EN are set to 0V

2 Iso2[dBm] = noise floor when VRAMP is set to 0V and TX_EN is set to logic high

3 Twu = wake-up time (time needed to have the loop locked)

4 Tr_ramp = rising time

5 Tf_ramp = falling time

6 For definitions of these values, (*, **, ***) refer to Appendix B, page 72 in the 3GPP TS 05.05 V8.16.0 (2003-08) specification. This specification can be found at the European Telecommunications Standards Institute (ETSI) web site, www.etsi.org/.

The ramp profile consists of the following:

- A pedestal voltage
- 12 to 16 dBc steps on the rising edge of the burst
- A constant region
- 12 to 16 dBc steps on the falling edge of the burst.

Generally, the same profile, scaled in amplitude, is used for all frequencies and power control levels. The MMM6035 also includes an internal offset generator which functions to cancel any external offset associated with the DAC driving the VRAMP pin. Also, the MMM6035 has a 200kHz, two poles Sallen and Key filter included in the VRAMP path to remove quantization noise and to provide VRAMP signal smoothing.

8 Test and Measurement Setup

Figure 8 shows the MMM6035 test and measurement setup.

- The SMIQ generates GSM burst (without shaping) and provides system frame trigger.
- Pulse and arbitrary waveform generators realize burst shaping on the Device Under Test (DUT)
- The CMU200 is used in non-signalling mode and synchronized on burst midamble.

Complete validation of power versus time and switching transients can be done under Final Test Approval (FTA)-like conditions.

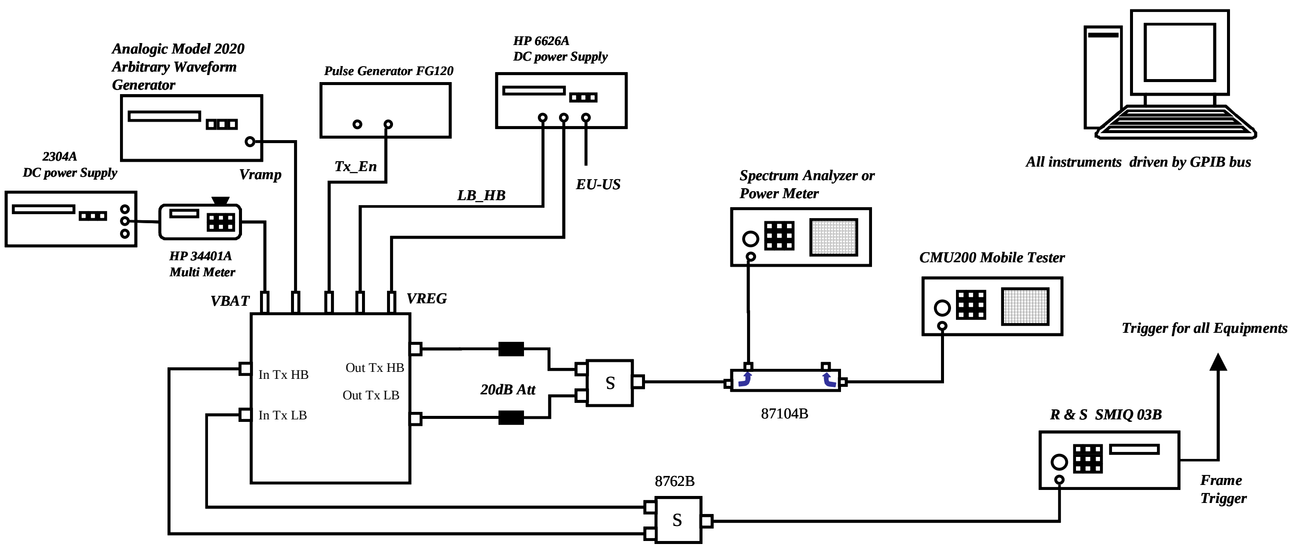

Figure 8. Test and Measurement Setup

8.1 System and RF Parameter Experimental Results

These signal settings lead to the following results.

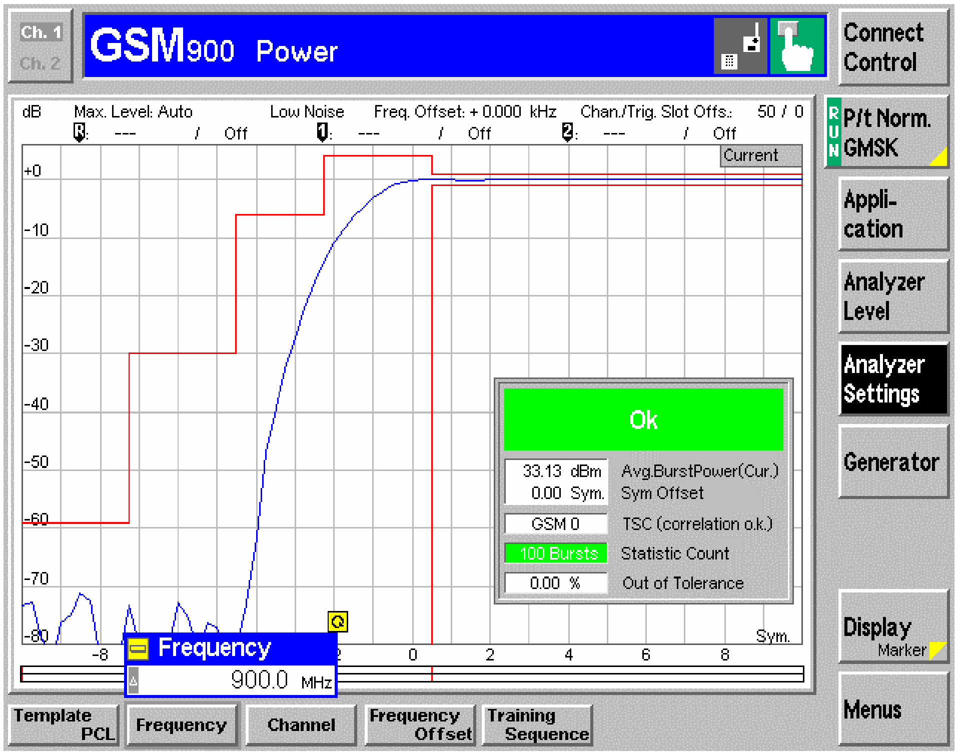

Figure 9. EGSM Rising Edge PCL5

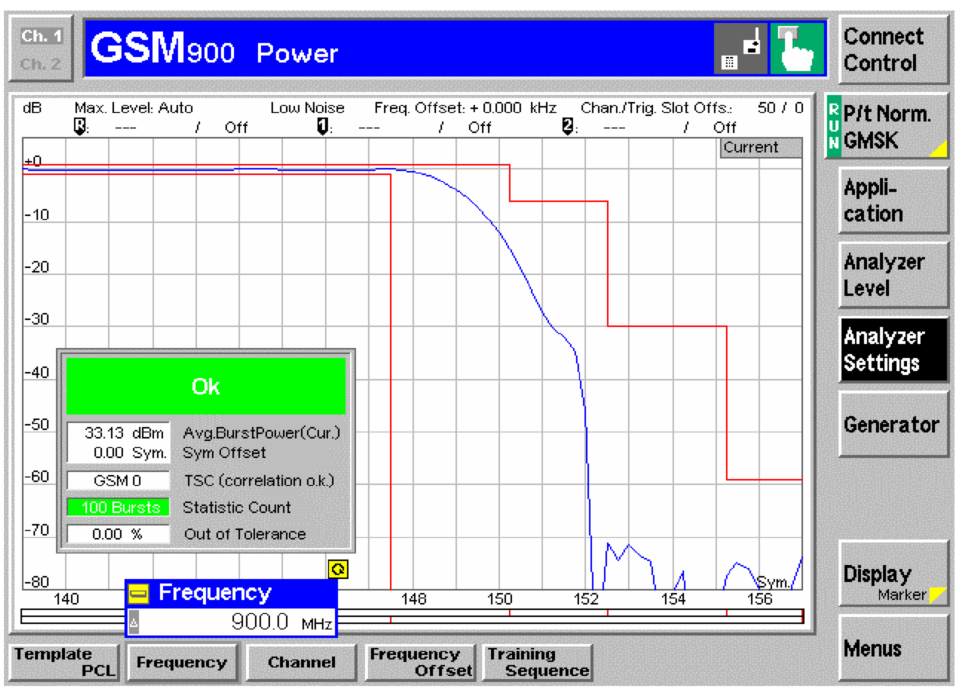

Figure 10. EGSM Falling Edge PCL5

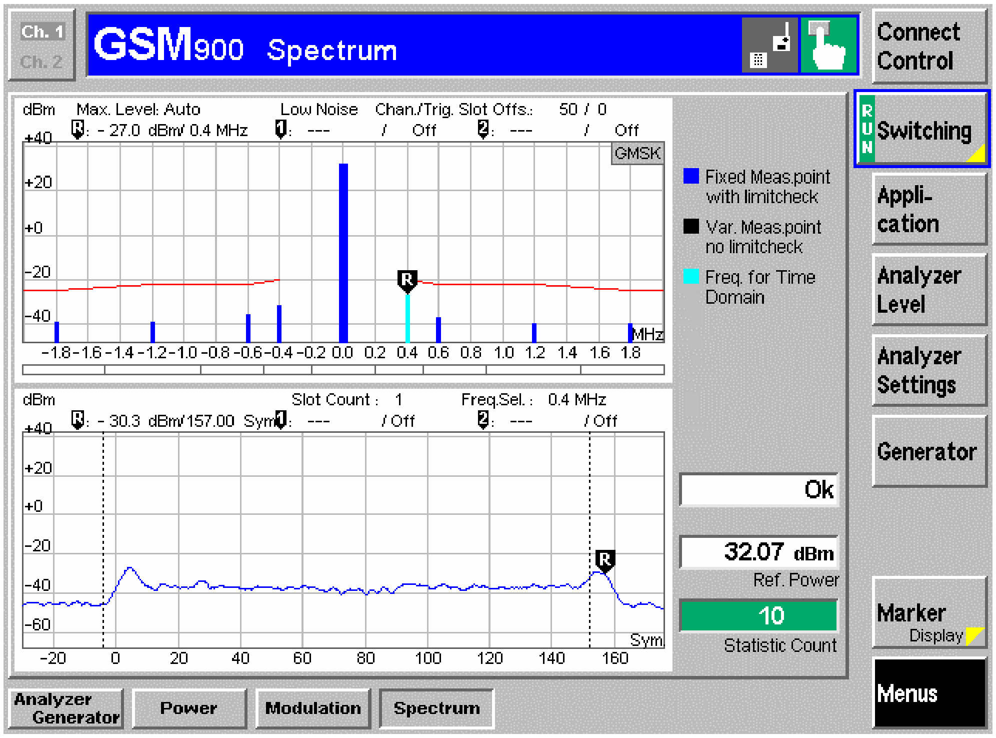

Figure 11. EGSM Switching Spectrum Low Vbatt

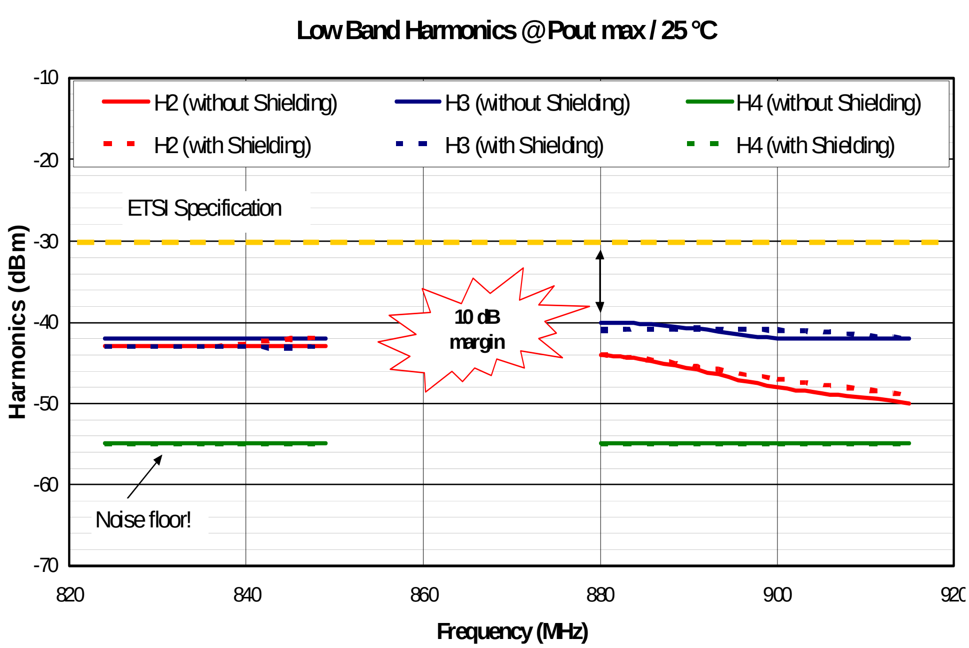

Figure 12. MMM6035 Low Band Harmonics At Antenna Port

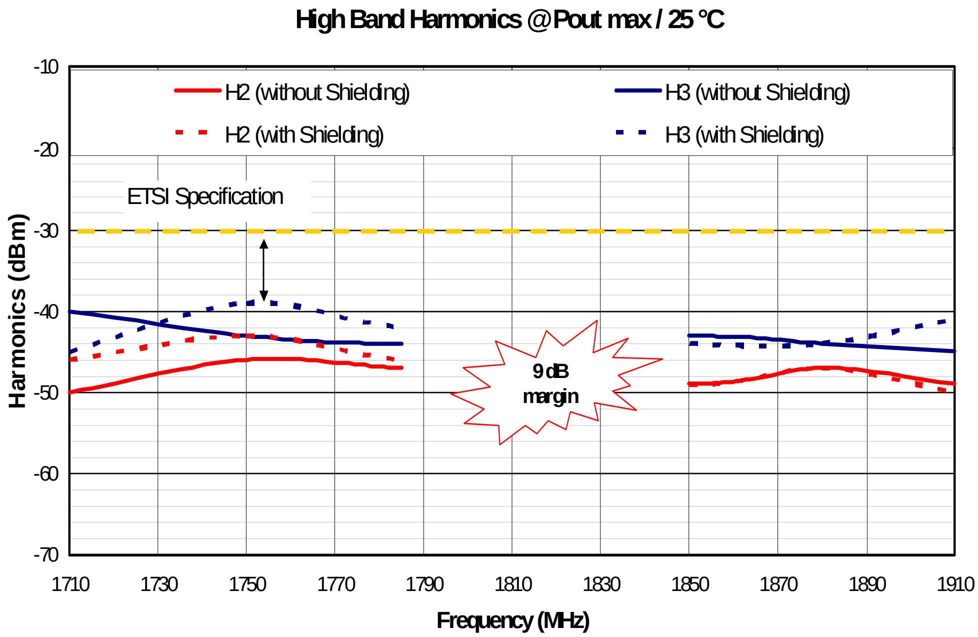

Figure 13. MMM6035 High Band Harmonics At Antenna Port

From the experimental results, the most critical RF parameters (harmonics, receiver band noise and time mask, as well as the switching and modulation ORFS) are FTA compliant.

9 Multi Slot Operation

The MMM6035 is suitable for GPRS applications, which among other things, can work with a 50 percent duty cycle burst. When a slot sequence is made of 1 to 4 slots of the same amplitude, VRAMP timing and shaping can be similar to the one described in the previous section. When slot sequences are of different amplitudes, appropriate inter-burst timing and shaping must be applied to fit the power versus time template.

The most constrained sequence is relative to Test 22.4 from the 05.05 ETSI specification. The first slot is transmitted at PCL5 and the second slot at PCL19 in Cellular/EGSM bands respectively and PCL15 and PCL0 for DCS1800/PCS1900 respectively.

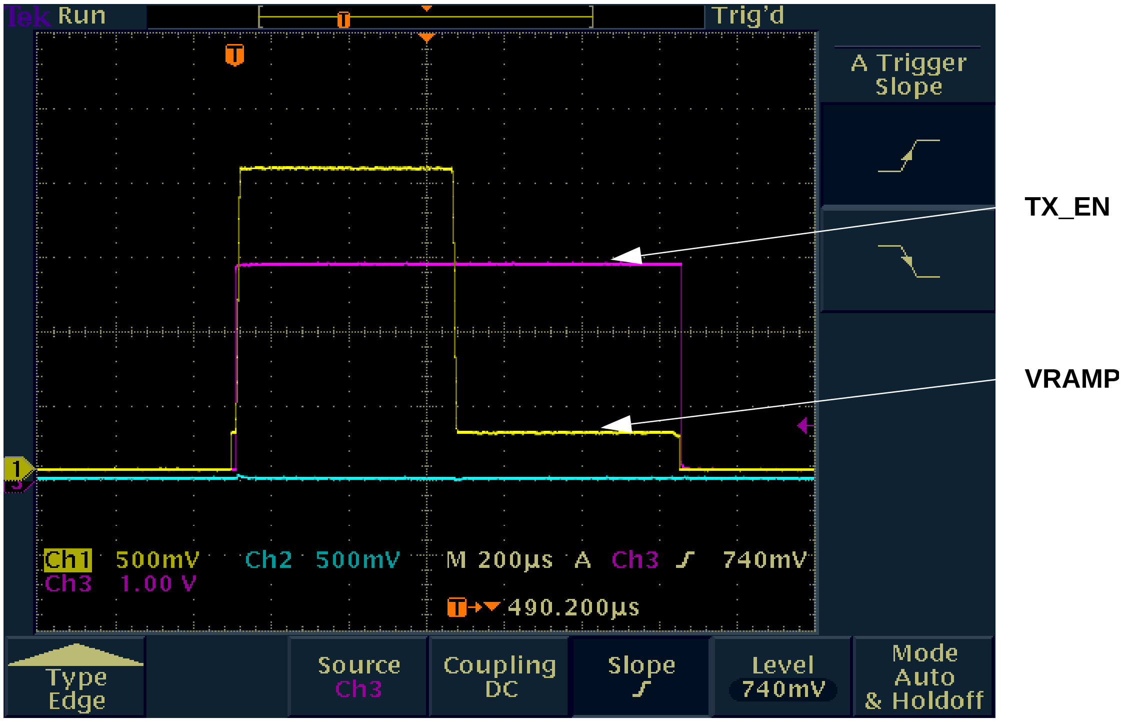

Figure 14. Control Signal For a 2 Slots Sequence

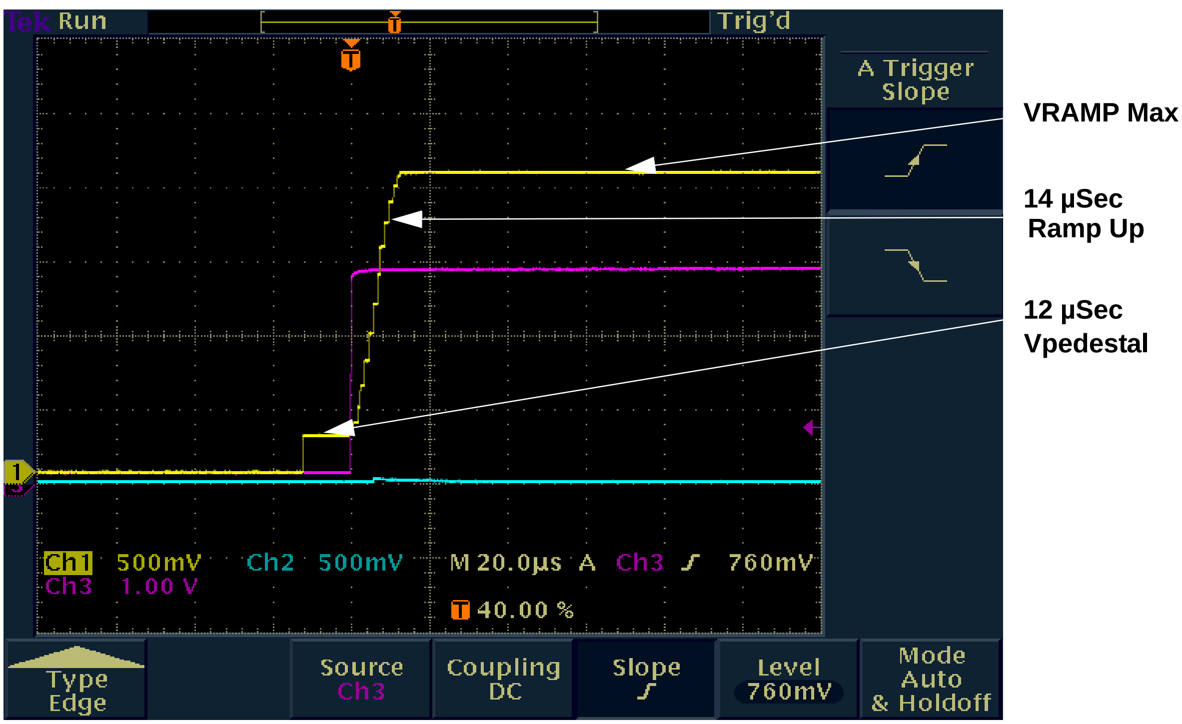

Figure 15. Zoom on 1st Slot Ramp-up

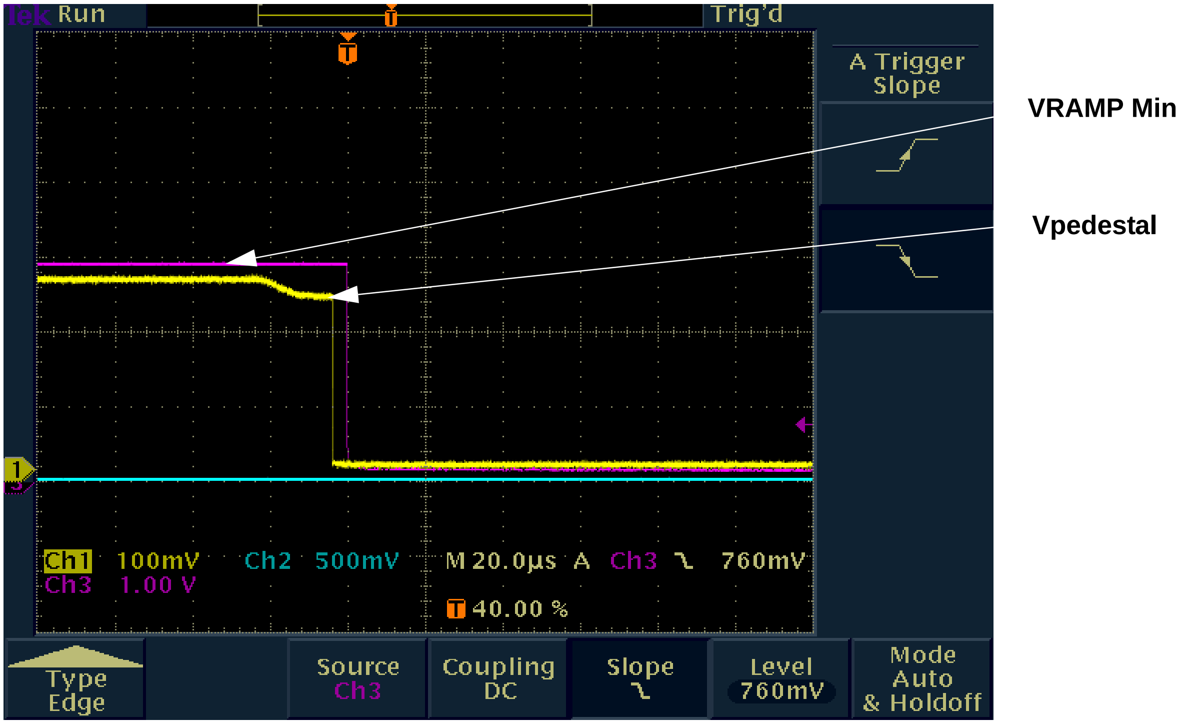

Figure 16. Zoom on 2nd slot ramp-down

To perform test 22.4 from the specification, the timing proposal for control signal can be the following.

As shown in Figure 15, Vpedestal is applied for a 12 µs period then Tx_En is activated. Once Tx_En has been activated, begin the ramp-up to generate 1st transmitted burst. The VRAMP maximum value has a duration of 543 µs then begin the 1st slot ramp-down until VRAMP minimum value. VRAMP is kept to VRAMP minimum during inter-slot and second slot duration. As indicated in Figure 16, ramp-down for 2nd slot goes from VRAMP minimum to Vpedestal for a14µs duration. VRAMP is then kept to Vpedestal for a couple of µs and then set to 0 V. Afterwards, Tx_En is set to low level to cut_off PA section.

Power versus time picture for the two slots sequence is shown in Figure 17.

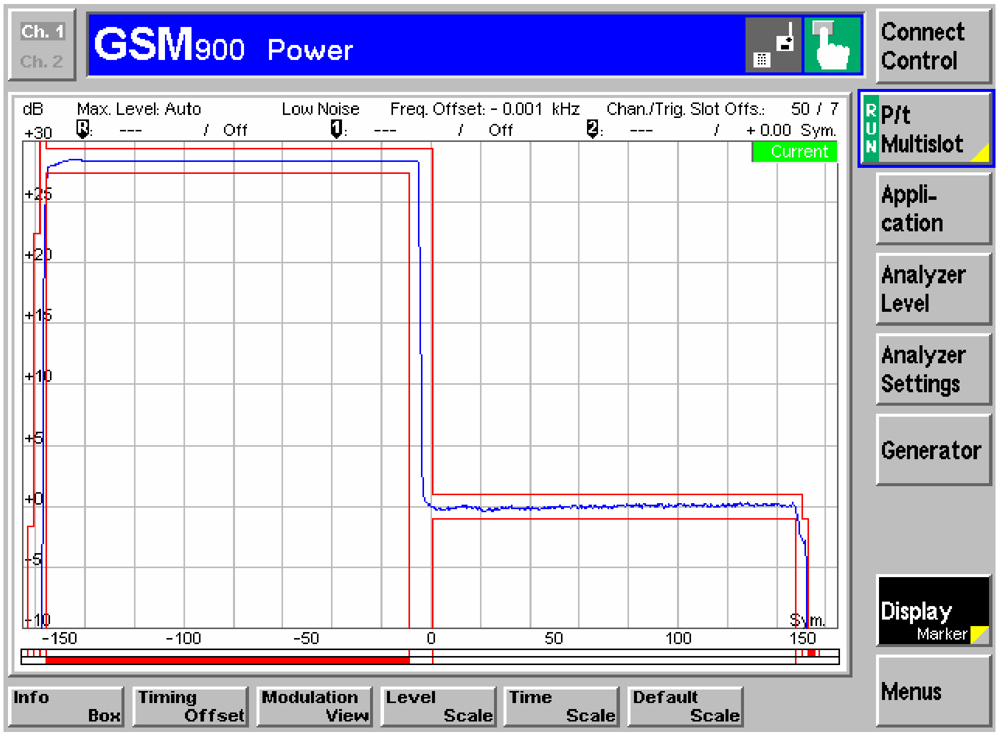

Figure 17. Power Versus Time For a 2 Slot Sequence

10 Current Limiter

The MMM6035 power controller exhibits lowered current drain in several scenarios. The power controller contains a current limiter block and one current reference was placed on the die. Current drawn by the PA under operation conditions is compared to this reference and clamped to a maximum value of 2.3A (related to the current reference) under extreme conditions. This limits damage to the power amplifier section. Figure 14 shows the impact of the current limiter feature under high output Voltage Standing Wave Ratio (VSWR).

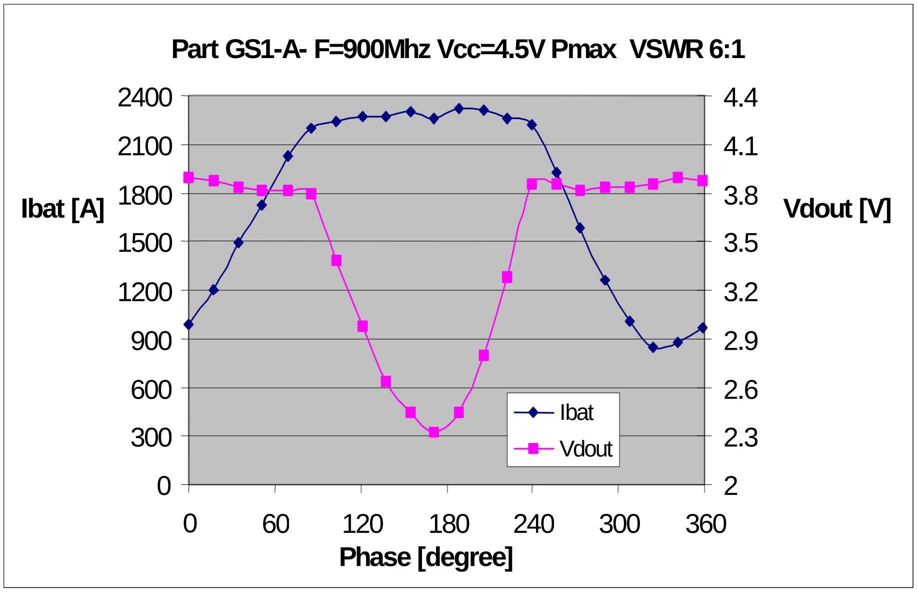

Figure 18. Current Limiter Effect

11 Conclusion

The MMM6035 is an effective product with multiple benefits.

- The drain supply voltage control technique leads to straightforward integration because no external passive components are required.
- It simplifies power calibration at the phone level.
- Its anti-saturation detection block allows switching transients to be passed under all conditions (Vbat, Temp. etc.) without any change on control signals.
- It exhibits robust loop behavior under output VSWR for power versus time and switching transients.

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