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MSC8103 Design Checklist

By Iantha Scheiwe

This application note provides a set of recommendations to assist you in a first-time design on the MSC8103 application development system (MSC8103ADS) board. This document can also be useful as a general guideline for debugging newly designed systems because it highlights the aspects of a design that merit special attention during initial system start-up.

CONTENTS

1 Getting Started

During the first phase of designing a system with the MSC8103 device, your main tasks are to estimate loads/performance for the communications peripheral module (CPM) and the buses, make the pin assignments, and configure the reset parameters. Before you get started, you should be familiar with the available documentation, silicon revisions, software, microcodes, models, and tools. Refer to **Section 11**, *Related Reading*, on page 16.

1.1 Estimating CPM and Bus Load

To estimate the CPM load factor for a specific combination of protocols, use the MPC8260 CPM Performance Evaluator tool. **Section 11** provides the Freescale web address where you can download this tool. In addition to CPM performance, this tool estimates the 60x system and local bus loads for the combination of protocols selected, bus frequencies, memory speeds, and placement of data structures. At start-up, the tool initializes all parameters with default values that are not recommended. Be sure to change these values according to those appropriate for your application.

1.2 Making Pin Assignments

The MSC8103 communications peripherals use four 32-bit parallel ports to exchange data with the physical interfaces. Each pin of the parallel ports multiplexes several signals. You can configure any pins not required for a particular communication protocol as general-purpose I/O (GPIO) signals. To verify the availability of the I/O functions chosen through pin multiplexing, use the MSC8103 Parallel Ports Configuration tool (Pin_mux8101), which is available on the MSC8103 web page (see **Section 11**).[1] After you select the signals required by the application, this utility defines the pin configuration of each parallel port. A report can then be generated that includes all your selections and C initialization code for the registers associated with the parallel ports.

1.3 Configuring Reset Parameters

Review the Hard Reset Configuration Word (HRCW) as you determine the initial power-on reset parameters, such as single MSC8103 bus mode versus 60x–compatible bus mode, boot port size, and so on, and then set the bits for your application (see **Table 1**).

Table 1. Hard Reset Configuration Word (HRCW)

Bits	Name	Description	Comments
0	EARB	System bus arbitration	0 Internal. 1 External.
1	EXMC	Memory controller	0 Internal. 1 External.
2	IRQ7INT	$\overline{\text{IRQ7}}$ or $\overline{\text{INT\_OUT}}$ selection	0 $\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$ pin is $\overline{\text{IRQ7}}$. 1 $\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$ pin is $\overline{\text{INT\_OUT}}$.
3	EBM	External bus mode This bit cannot be changed after reset.	0 Single MSC8103 bus mode. 1 60x-compatible bus mode.
4–5	BPS	Boot port size	00 64-bit. 01 8-bit. 10 16-bit. 11 32-bit.
6	SCDIS	SC140 disabled This bit cannot be changed after reset.	0 SC140 core enabled. 1 SC140 core disabled.
7	ISPS	Internal space port size This bit cannot be changed after reset.	0 64-bit system data bus. 1 32-bit system data bus.
8–9	IRPC	Interrupt pin configuration Defines the initial value of the SIUMCR[IRPC].	01 $\overline{\text{IRQ2}}$, $\overline{\text{IRQ3}}$, $\overline{\text{IRQ5}}$ active. 10 BADDR29, BADDR30, BADDR31 active.
10–11	DPPC	Data parity pin configuration Defines the initial value of the SIUMCR[DPPC]. This value cannot be changed after reset.	00 $\overline{\text{IRQ1–7}}$ active. 01 DP(0–7) active. 10 $\overline{\text{IRQ1}}$, DREQ3, DREQ4, $\overline{\text{DACK3}}$, $\overline{\text{DACK4}}$ active. 11 Additional arbitration lines and $\overline{\text{IRQ6–7}}$ active.
12	NMI OUT	NMI out handling	0 NMI serviced by SC140 core 1 NMI routed to an external pin for service by external host

1. The Freescale application note, AN1854, describes how to use Pin_mux8101 to initialize the MSC8103 CPM I/O. Both this application note and the software that accompanies it are available on the MSC8103 web page.

Table 1. Hard Reset Configuration Word (HRCW) (Continued)

Bits	Name	Description	Comments
13–15	ISB	Defines the initial value of the IMMR(ISB[0–14]) internal memory space base and determines the base address of the DSPRAM on the local bus. ISB value 101 causes the system bus address space and the QBus address space to overlap. For details, see the *MSC8103 Reference Manual*.	ISB Internal Memory Space DSPRAM (Bank 10) 000 0xF000_0000 0x02000000 001 0xF0F0_0000 0x03000000 010 0xFF00_0000 0x04000000 011 0xFFF0_0000 0x05000000 100 RSRV RSRV 101 0x00F0_0000 0x07000000 110 0x0F00_0000 0x08000000 111 0x0FF0_0000 0x09000000
16	—	Reserved	—
17	BBD	Bus busy disable	0 Enabled. $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ active. 1 Disabled. $\overline{\text{IRQ2}}$ and $\overline{\text{IRQ3}}$ active.
18–19	MMR	Mask masters requests	00 No masking on bus request lines. 11 All external bus requests masked.
20–21	—	Reserved	—
22–23	TCPC	Transfer code pin configuration	00 TC(0-2). 10 BNKSEL(0-2).
24–25	BC1PC	BC1PC value	00 BCTL1 active. 01 BCTL1 active.
26	SWDIS	Software watchdog disable	0 Software watchdog timer enabled. 1 Software watchdog timer disabled.
27	DLLDIS	DLL disable	0 DLL enabled. 1 DLL bypassed.
28–30	MODCK_H	MODCK[4–6]	See “Clock Signal Configuration” in the *MSC8103 Technical Data* sheet
31	—	Reserved	—

2 Power

This section outlines the MSC8103 power considerations: power supply, power consumption, power sequencing, power planes, and decoupling. It also presents a recommended power supply design. For information on the MSC8103 AC and DC electrical specifications and thermal characteristics, refer to the data sheet.

- *Power supply*. The MSC8103 device has a core voltage, V_{DD}, that operates at a lower voltage than the I/O voltage, V_{DDH}. You should supply the MSC8103 core voltage V_{DD} via a variable switching supply or regulator to allow for future compatibility with possible core voltage changes on future silicon revisions. The core voltage is supplied across V_{DD} and V_{SS} (GND). The core supply voltages are 1.5V–1.7V, and the maximum frequency is 275 MHz.

  The I/O section of the MSC8103 device is supplied with 3.3V (± 5%) across V_{DDH} and V_{SS} (GND). Typically, this voltage is supplied by a simple linear regulator, which increases system complexity because multiple voltage supplies are required for the design. External signals on the MSC8103 device are not 5V tolerant. All input signals must meet the V_{IN} DC spec (–0.2 V to V_{DDH} + 0.2).

- *Power consumption*. The *MSC8103 Technical Data* sheet provides preliminary power dissipation estimates for various configurations.

- *Power sequencing.* For details, consult the “Design Considerations” section of the *MSC8103 Technical Data* sheet.
- *Suggested power supply design.* One of the most common ways to derive power is to use either a simple fixed or adjustable linear regulator. For the system I/O voltage supply, a simple fixed 3.3V supply can be used. However, a separate adjustable supply for the core voltage V_{DD} should be implemented. As **Figure 1** shows, an adjustable linear regulator supply can be used. To support future MSC8103 silicon revisions with lower core voltages for lower power, V_{OUT} can be adjusted by modifying the values of R_{2ADJ}. In the example shown in **Figure 1**, R_1 = 150 Ω, R_2 = 390Ω, R_{2ADJ} = 0–KΩ generates an output voltage of 1.36–1.7 V.

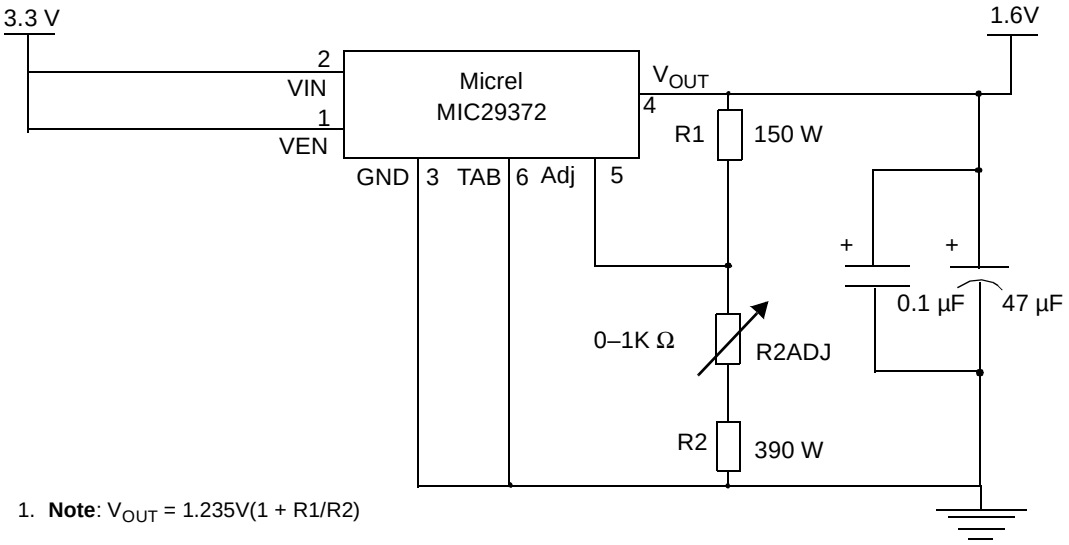

Figure 1. Core Power Supply Using Adjustable Linear Regulator

- *Power planes.* Each V_{CC} and V_{DD} pin should have a low-impedance path to the board power supply. Each GND pin should have a low-impedance path to ground. The power supply pins drive distinct groups of logic on the device. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as closely as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC}, V_{DD}, and GND should be kept to less than half an inch per capacitor lead. A minimum four-layer board that employs two inner layers as V_{CC} and GND planes is recommended. For details on MSC8103 layout, see the “Design Considerations” section of the *MSC8103 Technical Data* sheet.
- *Decoupling.* Both the I/O voltage (V_{DDH}) and core voltage (V_{DD}) should be decoupled for switching noise. Standard capacitor values of approximately 0.1 µF and 10 µF should be used. One high frequency decoupling cap for every two voltage pins is recommended. Following this guideline, approximately thirteen 0.1 µF and two 10 µF capacitors should be used on the I/O (V_{DDH}) supply and placed as closely to the MSC8103 device as possible. Approximately seven 0.1 µF and one 10 µF capacitors should be used on the Core (V_{DD}) supply and placed as closely to the MSC8103 device as possible. Other values and quantities can be substituted for these approximate numbers per designer discretion.
- *PLL power supply filtering.* The V_{CCSYN}/V_{CCSYN1} power signals on the MSC8103 device provide power to the clock generation phase-locked loops. To ensure stability of the internal clock, the power supplied to these pins should be filtered with capacitors that have low and high frequency filtering characteristics (0.01 µF and 10 µF). V_{CCSYN}/V_{CCSYN1} can be connected to V_{DD} through a 10Ω

resistor. GND_{SYN} and GND_{SYN1} can be tied directly to the V_{SS} (GND) plane. A circuit similar to the one shown in **Figure 2** is recommended.

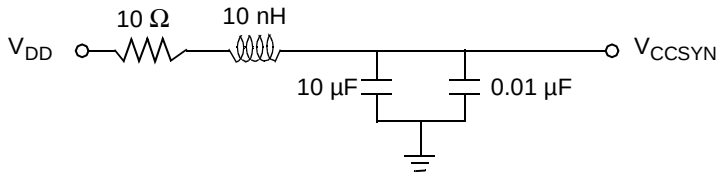

Figure 2. PLL Power Supply Filter Circuit

To minimize noise coupled from nearby circuits, the PLL loop filter should be placed as closely as possible to the V_{CCSYN} and V_{CCSYN1} pins.The 0.01 µF capacitor should be closest to V_{CCSYN} and V_{CCSYN1}, followed by the 10 µF capacitor, the 10-nH inductor, and finally the 10-Ω resistor to V_{DD}. These traces should be kept short. GND_{SYN} and GND_{SYN1} should be provided with an extremely low impedance path to ground and should be bypassed to V_{CCSYN} and V_{CCSYN1}, respectively, by a 0.01 µF capacitor located as closely as possible to the MSC8103 package. You should also bypass GND_{SYN} and GND_{SYN1} to V_{CCSYN} and V_{CCSYN1} with a 0.01 µF capacitor located as closely as possible to the MSC8103 package.

3 Clocks

All clock inputs and outputs except those associated with a serial clock are referenced to REFCLK. In DLL-enabled mode REFCLK is DLLIN. In DLL-disabled mode REFCLK is CLKOUT. The MODCK[1–3] pins are sampled 1024 clocks after the deassertion of $\overline{\text{PORESET}}$ (while $\overline{\text{HRESET}}$ is still asserted). Their value can be set using either pull-up/pull-down resistors. Therefore, open collector drivers are not needed. MODCK_H can be set in the HRCW, or you can take the default value. Collectively, the MODCK_H and MODCK fields define the multiplication of the input clock (CLKIN) to derive the SC140 core, system bus, and CPM clock ratios. Note that the PLL multiplication value is set only during an initial $\overline{\text{HRESET}}$ caused by a $\overline{\text{PORESET}}$, so the PLL does not change during subsequent assertions of $\overline{\text{HRESET}}$.[2]

4 Reset

This section presents recommendations for configuring the MSC8103 device for reset.

4.1 Power-On-Reset Circuit

There is no power-up detector on the MSC8103 device. Optionally, you can use a power-on-reset chip to monitor the power plane and drive $\overline{\text{PORESET}}$.

$\overline{\text{HRESET}}$ is a bidirectional signal and, if it is driven as an input, it should be driven with an open collector or open-drain device. When an open-drain output such as $\overline{\text{HRESET}}$ is used, take care when driving many buffers that implement input bus hold circuitry. The bus hold currents can cause enough voltage drop across the pull-up resistor to change the logic level to low. With either a smaller value of pull-up resistor or less current loading from the bus hold drivers, you can solve this problem. To avoid exceeding the MSC8103 output current, the pull-up value should not be too small.

2. For the most up-to-date clock configuration mode tables, consult the *MSC8103 Technical Data* sheet (MSC8103).

SRESET is a bidirectional signal and, if driven as an input, should be driven with an open collector or open-drain device. The MSC8103 device drives SRESET if the PORESET line or the HRESET line is asserted. SRESET can also be driven by a software watchdog time-out, bus monitor time-out, JTAG reset, or external soft reset.

4.2 Reset Configuration Pins

You can accept the default HRCW values (0x0000_0000) by connecting RSTCONF to a logic 1 during HRESET. In this case, no accesses are made to the PROM connected to CS0. The default for the device is single MSC8103 mode. Both BCTL0 and BCTL1 are active (functioning as W/R and OE) when the HRCW values are applied. Take care to avoid bus contention during this time if buffers on the board are under BCTL[0–1] control.

You can obtain initial values other than the default by connecting RSTCONF to logic 0 during HRESET. The HRCW is read from the PROM connected to CS0 at addresses 0x00, 0x08, 0x10, and 0x18, or received from a host. These four bytes are written to the fields of the HRCW. With RSTCONF tied to logic 0, the MSC8103 device acts as a configuration master to configure up to seven MSC810x configuration slaves. The RSTCONF lines of up to seven slaves must be individually connected to the most significant 7 address bits of the configuration master's address bus. The master continues to read bytes starting at 0x20, configures the next slave while driving the RSTCONF line of the slave, and writes a 32-bit configuration word to that slave while driving the HRESET asserted to the slave. This process repeats from addresses 0x40, 0x60, 0x80, 0xA0, 0xC0, and 0xE0 for the remaining six slaves.

The configuration master drives the full 32-bit configuration word on the 60x data bus after each of the four byte-reads from the PROM. Avoid any contention on the bus that would affect the configuration word. No pull-up resistors are required on the address bus as it is actively driven during this operation.

The slave can be configured to receive the HRCW through its HDI16 host interface. The host device should tie its address lines to the HA[0–3] address lines of the slave devices. The HPE pin of the slave devices must be pulled to V_{CC}. Also, the HRCW sent to the slave device must have the ISPS bit (bit 7) set. Note that the HRCW is still sent in four separate bytes.

A reduced reset option is available from serial EPROM via the I^2C protocol. Limited fields of the HRCW are configured via the appropriate data bus bits on the system bus. Only the NMI OUT (bit 12), ISB (bits 13–15), SWDIS (bit 26), and DLLDIS (bit 27) fields in the HRCW can be programmed using this method. MODCK_H cannot be programmed using this method, and the value is set by default to 000. Therefore, only clock modes 0–1 and 4–7 can be used with this boot mode. During the first 8 CLKIN cycles D[12–15] and D[26–27] are sampled to configure the NMI OUT, ISB, SWDIS, and DLLDIS fields in the HRCW. All other data bus bits are ignored. **Table 2** shows the reset pin configuration required for each reset and boot option.

5 Boot

The MSC8103 device can be booted from memory on the system bus by an internal memory controller, a host through the HDI16 interface, or the I^2C protocol with a serial EPROM. The state of the BTM[0–1] signals is sampled at the rising edge of PORESET (see **Table 2**). The MSC8103 device can be booted from memory that is 8-, 16-, 32-, or 64-bits wide.

Table 2. Boot Mode Settings

RSTCONF	HPE/EE1	BTM[0-1]/EE[4-5]	Boot Mode
1	1	01	Host reset configuration
0	0	00	Master hardware reset configuration

Table 2. Boot Mode Settings (Continued)

RSTCONF	HPE/EE1	BTM[0-1]/EE[4-5]	Boot Mode
1	0	00	Slave hardware reset configuration
0	0	10	Master reduced reset configuration
1	0	10	Slave reduced reset configuration

When an internal memory controller is the boot source, the memory should be attached to $\overline{\text{CS0}}$, which functions as the global boot select. The memory should also be of a type that can be controlled by a GPCM machine (EPROM or Flash memory). The HRCW[BPS] bit sets the width of the $\overline{\text{CS0}}$ space. After configuration, the SC140 core fetches the address of the boot routine from location 0xFE00_0110. When a host boots the MSC8103 device through the HDI16 interface, the host interacts with the HDI16 in polling mode and begins transmitting data. The third boot option, booting via serial interface (I^2C), is listed in **Table 2** as "reduced reset configuration."[3]

6 Bit and Byte Lane Ordering on the System Bus

On the system bus, the highest order address bit is A[0], and the lowest order address bit is A31. All 32 address pins are valid in a byte access. In a 64-bit double word access, only the A[0–28] address pins are valid, and A[29–31] are driven low. For the 60x data bus, the highest order data bit is D0 and the lowest order data bit is D63.[4] Following are bit and byte lane ordering considerations for various activities on the system bus:

- *Data byte lane ordering.* D[0–7] is the highest order byte lane on the data bus, and D0 is the highest order bit of that byte lane. D[0–7] corresponds to write enable 0 ($\overline{\text{PWE0}}$) and byte lane select 0 (for example, $\overline{\text{PSDDQM0}}$). **Table 3** shows the data byte lane ordering for both the system bus and the local bus.

Table 3. 60x Bus Data Byte Lane Ordering

Data Bus Signals	Byte Lane	External Pins (Byte Lane Select)
D[0–7]	0	$\overline{\text{PWE0}}$/$\overline{\text{PSDDQM0}}$/$\overline{\text{PBS0}}$
D[8–15]	1	$\overline{\text{PWE1}}$/$\overline{\text{PSDDQM1}}$/$\overline{\text{PBS1}}$
D[16–23]	2	$\overline{\text{PWE2}}$/$\overline{\text{PSDDQM2}}$/$\overline{\text{PBS2}}$
D[24–31]	3	$\overline{\text{PWE3}}$/$\overline{\text{PSDDQM3}}$/$\overline{\text{PBS3}}$
D[32–39]	4	$\overline{\text{PWE4}}$/$\overline{\text{PSDDQM4}}$/$\overline{\text{PBS4}}$
D[40–47]	5	$\overline{\text{PWE5}}$/$\overline{\text{PSDDQM5}}$/$\overline{\text{PBS5}}$
D[48–55]	6	$\overline{\text{PWE6}}$/$\overline{\text{PSDDQM6}}$/$\overline{\text{PBS6}}$
D[56–63]	7	$\overline{\text{PWE7}}$/$\overline{\text{PSDDQM7}}$/$\overline{\text{PBS7}}$

- *Memory controller byte lane ordering.* The memory controllers can access memories that are 8-, 16-, 32-, and 64-bits wide without creating any "holes" in the memory space on the system bus. In all cases, the memories should be placed into the most significant byte lanes, as shown in **Table 4**.

3. For details on booting the MSC8103 device, consult the "Boot" chapter in the *MSC8103 Reference Manual* (MSC8103RM).
4. It is recommended that schematics use documented terminology for this system bus as defined in the "External Signals" chapter of the *MSC8103 Reference Manual*.

Table 4. Byte Lanes for Memory Widths

Memory Width	Byte Lanes
Byte (8-bits)	0
Half Word (16-bits)	0, 1
Word (32-bits)	0, 1, 2, 3
Double Word (64-bits)	0, 1, 2, 3, 4, 5, 6, 7

- *Flash memory devices*. The data lines of most Flash memory devices connect to the MSC8103 device with byte lanes bit-reversed for programming algorithm purposes. **Figure 3** shows a 32-bit example.

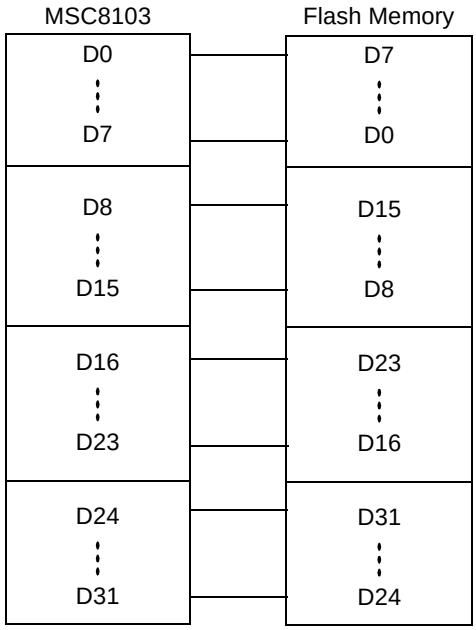

Figure 3. MSC8103 to Flash Memory Byte Lane Reversal

To bring up a board with blank Flash memory and no host processor, use a switch or other method to force $\overline{\text{RSTCONF}}$ to a logic “1.” This brings up the MSC8103 device in the default state. Otherwise, invalid PLL values may be loaded.

- *UTOPIA bit ordering*. The numbering of the MSC8103 UTOPIA interface is consistent with that of the UTOPIA standard. See **Table 5**.

Table 5. UTOPIA Bit Ordering

UTOPIA Mode	MSB	LSB
8-bit	TxDATA[7]/RxDATA[7]	TxDATA[0]/RxDATA[0]
8-bit	TxADD/RxADD[4]	TxADD/RxADD[0]

- *FCC Nibble mode bit ordering*. The numbering of the FCC interface is consistent with that of DS3 framers such as the TranSwitch TCX-03401. When data moves across the wire, TxD3/RxD3 is transmitted/received first relative to TxD0/RxD0.

7 External Signals

The MSC8103 is not 5V tolerant. All input signals must meet V_{IN} DC Spec (–0.2V to V_{DDH}+0.2). The bus can be pipelined up to two address cycles deep (for example, it can have a $\overline{\text{TS}}$, an $\overline{\text{AACK}}$, and another $\overline{\text{TS}}$ before the first $\overline{\text{TA}}$). Because the address is valid only during the address phase ending with $\overline{\text{AACK}}$, external latches and multiplexes are necessary for SDRAM and so on. Note that on accesses to internal slaves such as CPM dual-port RAM, as well as SDRAM page hits, $\overline{\text{TA}}$ can come before $\overline{\text{AACK}}$. In fact, $\overline{\text{AACK}}$ and $\overline{\text{TA}}$ are not guaranteed to be in order. In single MSC8103 bus mode, the bus operation is the same as the 60x bus mode, except that the address driven on A[0–31] is latched and possibly multiplexed inside the MSC8103 device. Therefore, the address is valid throughout the data phase of the cycle beginning with $\overline{\text{AACK}}$ and ending with the data phase of the next access. Single MSC8103 mode does not support mastering of the system bus by any other resource, including an additional MSC8103.

The local bus does not burst when accessed from an external master through the system bus bridge. Accesses to the local bus are not snooped by the SC140 core. Burst accesses by 60x masters to the DPRAM, registers, or local bus terminate with $\overline{\text{TEA}}$. The MSC8103 device uses $\overline{\text{AACK}}$ and $\overline{\text{TA}}$ for all accesses to CPM dual-port RAM and CPM registers. It also asserts $\overline{\text{AACK}}$ for all accesses to external memory that match a BR/OR range in the memory controller (and will also drive $\overline{\text{TA}}$ unless programmed otherwise).

8 Memory

Design considerations for MSC8103 memory are as follows:

- *System bus signals and memory transactions.* The memory controller drives $\overline{\text{PSDVAL}}$ during an access to an MSC8103-controlled resource—that is, internal space or chip-selects. Only external devices implementing the MSC8103 memory bank-based bus sizing protocol, such as an external MSC8103, use $\overline{\text{PSDVAL}}$. MSC8103 designs incorporating devices that do not implement the MSC8103 memory bank-based bus sizing protocol must either provide 64-bit ports on the system bus or ensure that only MSC8103-initiated transactions can access the 8-, 16-, or 32-bit memory-mapped slaves on the system bus. Use $\overline{\text{PWE[0–7]}}$ to control the R/$\overline{\text{W}}$ lines of memories for timing flexibility. For buffer direction control, use the $\overline{\text{BCTL[0–1]}}$ signals.
- *Addressing memories using the GPCM and UPM machines.* In 60x-bus-compatible mode, use the BADDR [27–31] pins—not the standard address A[27–31] pins—to address memories for the GPCM and UPM machines. The address lines are not to be used because 60x masters (including the internal SC140 core) do not dynamically adjust bus size, and they drive only the starting address on a burst, so the address lines do not increment. The GPCM memory controller accesses the memory in single accesses. Both the GPCM and the UPM increment the BADDRx lines to gather the bytes requested by the 60x master. In single MSC8103 mode, the memory controllers drive the address lines for small port sizes and increments for bursts. Therefore, the BADDRx pins are not needed in this mode.
- *Bank selects versus address lines.* In single MSC8103 mode, use the BNKSEL lines to interface to SDRAM in order to support different SDRAM densities without board wiring changes. Also, when you use the BNKSEL lines and set the BCR[EAV] bit, logic analyzers can view the non-multiplexed address of the access.
- *Page versus bank interleaving.* Page interleaving is the preferred method for connecting to SDRAM. Bank interleaving generally offers lower performance than page interleaving and is included for compatibility with designs that used this mode before page interleaving became available.

9 EOnCE/JTAG Interface

The MSC8103 device has an Enhanced On-Chip Emulation module (EOnCE), a feature that is common to all Freescale processors with the SC140 core. This feature gives internal access to scan chains for debug purposes and also provides a serial connection to the SC140 core for emulator support. Adding an EOnCE/JTAG connection adds little or no cost to the system but gains significant advantages during early system development. The EOnCE interface uses a standard 14 pin header, as shown in **Figure 4**.

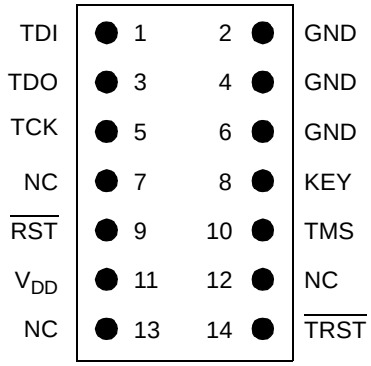

Figure 4. 14-Pin Header for JTAG/EOnCE Interface

The EOnCE interface connects through the JTAG port on the MSC8103 device with some additional status monitoring signals. **Table 6** shows the pin definitions and recommendations.

Table 6. JTAG/EOnCE Interface Pin Definitions

Pins	Connection	Description	Recommendations
1	TDI	Test Data In	If there are multiple devices on the JTAG chain, connect TDI to the TDO signal of the previous device in the chain.
2, 4, 6	GND	System Ground Plan	Connect to digital ground.
3	TDO	Test Data Out	If there are multiple devices on the JTAG chain, connect TDO to the TDI signal of the next device in the chain.
5	TCK	Test Clock	Add 10KΩ pull-up resistor to V_{CC}.
7,13,12	NC	No Connect	Leave unconnected.
8	KEY	Mechanical Keying	Pin should be removed.
9	$\overline{\text{RST}}$	Reset	May be tied to $\overline{\text{HRESET}}$.
10	TMS	Test Mode Select	None.
11	V_{DD}	I/O Power Supply	Connect to MSC8103 I/O voltage V_{DDH} through a 10k current limiting resistor.
14	$\overline{\text{TRST}}$	Test Reset	$\overline{\text{TRST}}$ has an internal pull-up resistor, so no external pull-up or pull-down resistor is required. However, you should add a 10k pull-down resistor to GND on this signal to keep the JTAG in reset mode while the device is operating regularly.

10 Signal Connectivity and Terminations

This section summarizes the connections and special conditions for the MSC8103 device, such as pull-up or pull-down resistors required. **Table 7** shows the states of all of the signals during $\overline{\text{HRESET}}$, along with their recommended terminations.

10.1 Connectivity Guidelines

Unused output signals can be left disconnected, and unused input signals should be connected to their non-active values, except for the following signals:[5]

- Clock signals:
  - MODCK[1–3] configure the MSC8103 device and are sampled on the deassertion of $\overline{\text{PORESET}}$, so they should be tied to V_{CC} or GND either directly or through pull-up or pull-down resistors until the deassertion of $\overline{\text{PORESET}}$. After $\overline{\text{PORESET}}$ is deasserted, these signals can be floating.
  - DLLIN synchronizes to an external device. If no external device is used for synchronization, then this signal should connect to CLKOUT.
- Reset, configuration, and EOnCE signals:
  - HPE/EE1 configures the MSC8103 device and is sampled on the deassertion of $\overline{\text{PORESET}}$, so it should be tied to V_{CC} or GND either directly or through pull-up or pull-down resistors until the deassertion of $\overline{\text{PORESET}}$. After $\overline{\text{PORESET}}$ is deasserted, this signal can be used as an EOnCE event signal and can be left floating if the EE_CTRL register is configured with this signal as an output.
  - BTM[0–1]/EE[4-5] configure the MSC8103 device and are sampled on the deassertion of $\overline{\text{PORESET}}$, so they should be tied to V_{CC} or GND either directly or through pull-up or pull-down resistors until the deassertion of $\overline{\text{PORESET}}$. After $\overline{\text{PORESET}}$ is deasserted, these signals can be used as EOnCE event signals, and they can be left floating if the EE_CTRL register is configured with these signals as outputs.
  - $\overline{\text{RSTCONF}}$ configures the MSC8103 device and is sampled on the deassertion of $\overline{\text{PORESET}}$, so it should be tied to V_{CC} or GND either directly or through pull-up or pull-down resistors until the deassertion of $\overline{\text{PORESET}}$. After $\overline{\text{PORESET}}$ is deasserted, this signal can be floating.
  - $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ should be pulled up.
- System bus, HDI16, and interrupt signals:
  - The following signals can be disconnected in single-master mode (BCR[EBM] is reset): $\overline{\text{BG}}$, $\overline{\text{DBG}}$, $\overline{\text{EXT\_BG[2-3]}}$, $\overline{\text{EXT\_DBG[2–3]}}$, $\overline{\text{GBL}}$, and $\overline{\text{TS}}$.
  - If BCR[EBM] is set, the following signals should be pulled up: $\overline{\text{BG}}$, $\overline{\text{DBG}}$, $\overline{\text{EXT\_BG[2–3]}}$, $\overline{\text{EXT\_DBG[2–3]}}$, $\overline{\text{GBL}}$, $\overline{\text{TS}}$, and $\overline{\text{AACK}}$.
  - The following signals must be pulled up: $\overline{\text{ARTRY}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, and $\overline{\text{PSDVAL}}$.
  - When they are used, the following signals should be pulled up: $\overline{\text{IRQx}}$.
- CPM port signals:
  - An unused GPIO pin can be disconnected. After boot, it should be defined as an output pin.

5. All of these signals are described in detail in the chapter on “External Signals” in the *MSC8103 Reference Manual* (MSC8103RM).

10.2 Signal Terminations

In **Table 7**, signal connections are classified as follows:

- xx–yyΩ V_{DDH}. A pull-up resistor to the V_{DDH} power supply, with a value between xx and yy Ω. You can select the value on the basis of system requirements, such as noise immunity.
- xx–yyΩ GND. A pull-down resistor to the ground power connection, with a value between xx and yy Ω. Again, you can specify the value.
- Open. The signal should/must be left unconnected. The Note column in **Table 7** specifies whether this is a recommendation or a requirement.
- "As needed." The connection is determined principally by the system. The signal generally connects to the system controller logic, whether from Freescale or one of several third parties who make such logic. If not designated, a pull-up resistor should be placed between 1K–10KΩ V_{DDH} and a pull-down between 100–1KΩ GND.

Unused inputs should be tied high or low, but not left floating. Unused inputs can be tied directly to GND, but a pull-up resistor is recommended if it is tied high. Generally, it is good practice to tie any unused input to GND or V_{DDH} through a resistor for board testing purposes.

The following signals are active during the reset configuration period of $\overline{\text{HRESET}}$: A[0–31], $\overline{\text{BCTL0}}$, $\overline{\text{BCTL1}}$, D[0–63], $\overline{\text{CS0}}$, $\overline{\text{POE}}$, and BADDRx. You can turn off all signals with the HIGHZ JTAG command. Input-only signals such as $\overline{\text{PORESET}}$ or signals configured in an input-only mode, such as $\overline{\text{IRQ}}$x and $\overline{\text{EXT_BR}}$x, do not require pull-up/pull-down resistors if they are actively driven. However, pull-up resistors are recommended in **Table 7**. You should exercise discretion.

The hard reset signal states provided here do not include the states during reset configuration. When $\overline{\text{PORESET}}$ is asserted, configurable signals have their default configuration and are therefore Hi-Z. During reset configuration, configurable signals still have their default configuration, and certain memory controller signals operate to perform the reset configuration function (A[0–31], $\overline{\text{BCTL0}}$, $\overline{\text{BCTL1}}$, D[0–63], $\overline{\text{CS0}}$, $\overline{\text{POE}}$, and BADDRx).

Table 7. Signal States and Recommended Termination

Signal	Function (1)	State at Hard Reset	Connection		Notes
			If Used	If Not Used	
$\overline{\text{BR}}$	B	Tri-stated, EARB=0 High, EARB=1	1K–10KΩ V_{DDH}		Pull up if EARB=0.
$\overline{\text{BG}}$	B	High, EARB=0 Tri-stated, EARB=1	1K–10KΩ V_{DDH}		Pull up if EARB=1.
$\overline{\text{ABB}}$/$\overline{\text{IRQ2}}$	B	Tri-stated	1K–10KΩ V_{DDH}		Pull up
$\overline{\text{TS}}$	B	Tri-stated	1K–10KΩ V_{DDH}		Pull up. If in single-master mode no Pull up required.
A[0–31]	B	Low	As needed	Open	No requirement
TT[0–4]	B	Tri-stated	1K–10KΩ V_{DDH}		Pull up in multi-master mode.
$\overline{\text{TBST}}$	B	Tri-stated	1K–10KΩ V_{DDH}		Pull up
TSIZ[0–3]	B	Tri-stated	As needed	Open	TSIZ bus can be pulled up or down. Pull down TSIZ0 (100Ω) if an external master exists, else no requirement. In single-master mode these can be left open.

Table 7. Signal States and Recommended Termination (Continued)

Signal	Function (1)	State at Hard Reset	Connection		Notes
			If Used	If Not Used	
AACK	B	Tri-stated	1K–10KΩ V_{DDH}		Pull up
ARTRY	B	Tri-stated	1K–10KΩ V_{DDH}		Pull up
DBG	B	High, EARB=0 Tri-stated, EARB=1	1K–10KΩ V_{DDH}		Pull up
DBB/IRQ3	B	Tri-stated	1K–10KΩ V_{DDH}		Pull up
D[0–31]	B	Tri-stated	As needed	Open	No requirement
D[32–47]/HD[0–15]	B	Tri-stated	As needed	Open	No requirement
D[48–51]/HA[0–3]	B	Tri-stated	As needed	Open	No requirement
D52/HCS1	B	Tri-stated	As needed	Open	No requirement
D53/HRW/HRD	B	Tri-stated	As needed	Open	No requirement
D54/HDS/HWR	B	Tri-stated	As needed	Open	No requirement
D55/HREQ/HTRQ	B	Tri-stated	As needed	As needed	Pull up if host port enabled.
D56/HACK/HRRQ	B	Tri-stated	As needed	As needed	Pull up if host port enabled.
D57/HDSP	B	Tri-stated	As needed	Open	No requirement
D58/HDDS	B	Tri-stated	As needed	Open	No requirement
D59/H8BIT	B	Tri-stated	As needed	Open	No requirement
D60/HCS2	B	Tri-stated	As needed	Open	No requirement
D[61–63]	B	Tri-stated	As needed	Open	No requirement
DP0/EXT_BR2	B	High, DPPC=10 Tri-stated, Otherwise	As needed	Open	Pull up if used as EXT_BR2.
IRQ1/DP1/ EXT_BG2	B	High, DPPC=11 Tri-stated, Otherwise	As needed	Open	Pull up if used as IRQ1. Pull up EXT_BG2 if in multi-master mode.
IRQ2/DP2/ EXT_DBG2	B	High, DPPC=11 Tri-stated, Otherwise	As needed	Open	Pull up if used as IRQ2. Pull up EXT_DBG2 if in multi-master mode.
IRQ3/DP3/ EXT_BR3	B	High, DPPC=10 Tri-stated, Otherwise	As needed	Open	Pull up if used as IRQ3 or EXT_BR3.
IRQ4/DP4/DREQ3/ EXT_BG3	B	High, DPPC=11 Tri-stated, Otherwise	As needed	Open	Pull up if used as IRQ4 or DREQ3. Pull up EXT_BG3 if in multi-master mode.
IRQ5/DP5/DREQ4/ EXT_DBG3	B	High, DPPC=11 Tri-stated, Otherwise	As needed	Open	Pull up if used as IRQ5 or DREQ4. Pull up EXT_DBG3 if in multi-master mode.
IRQ6/DP6/DACK3/ IRQ6	B	High, DPPC=10 Tri-stated, Otherwise	As needed	Open	Pull up if used as IRQ6 or DACK3.

Table 7. Signal States and Recommended Termination (Continued)

Signal	Function (1)	State at Hard Reset	Connection		Notes
			If Used	If Not Used	
IRQ7/DP7/DACK4/ IRQ7	B	High, DPPC=10 Tri-stated, Otherwise	As needed	Open	Pull up if used as IRQ7 or DACK4.
PSDVAL	B	Tri-stated	1K–10KΩ V_{DDH}		Pull up
TA	B	Tri-stated	1K–10KΩ V_{DDH}		Pull up
TEA	B	Tri-stated	1K–10KΩ V_{DDH}		Pull up
GBL/IRQ1	B	Tri-stated	1K–10KΩ V_{DDH}		Pull up
BADDR29/IRQ2	B	Low	As needed	Open	Pull up if used as IRQ2.
BADDR30/IRQ3	B	Low	As needed	Open	Pull up if used as IRQ3.
BADDR31/IRQ5	B	Low	As needed	Open	Pull up if used as IRQ5.
CS[0–7]	O	High	As needed	Open	No requirement
BCTL1	O	High	As needed	Open	No requirement (Pulled-up on ADS board)
BADDR[27–28]	O	Low	As needed	Open	No requirement
ALE	O	High	As needed	Open	No requirement
BCTL0	O	Low	As needed	Open	No requirement (Pulled up on ADS board)
PWE[0–7]/PSDDQM [0–7]/PBS[0–7]	O	High	As needed	Open	No requirement (Pulled up on ADS board)
PSDA10/PGPL0	O	High	As needed	Open	No requirement
PSDWE/PGPL1	O	High	As needed	Open	No requirement (Pulled up on ADS board)
POE/PSDRAS/PG PL2	O	High	As needed	Open	No requirement (Pulled up on ADS board)
PSDCAS/PGPL3	O	High	As needed	Open	No requirement (Pulled up on ADS board)
PGTA/PUPMWAIT /PPBS/PGPL4	B	Tri-stated	As needed	Open	Pull up if used as PUPMWAIT or PGTA.
PSDAMUX/PGPL 5	O	Low	As needed	Open	No requirement
NMI_OUT	O	Tri-stated	As needed	Open	No requirement (Pulled up on ADS board)
IRQ7/INT_OUT	O	High, IRQ7INT=0 Otherwise: Tri-stated.	As needed	Open	Pull up if used as IRQ7.
TRST	I	Internal pull-up	100–1KΩ GND		See **Table 6**.
TCK	I	Tri-stated	1K–10KΩ V_{DDH}		Pull up
TMS	I	Internal pull-up	1K–10KΩ V_{DDH}		No requirement
TDI	I	Internal pull-up	1K–10KΩ V_{DDH}		No requirement
TDO	O	Tri-stated	As needed	Open	No requirement
TEST	I		0Ω VSS		Pull down

Table 7. Signal States and Recommended Termination (Continued)

Signal	Function (1)	State at Hard Reset	Connection		Notes
			If Used	If Not Used	
$\overline{\text{PORESET}}$	I	Tri-stated	1K–10KΩ V_{DDH}		Pull up
$\overline{\text{HRESET}}$	OD	Low	1K–10KΩ V_{DDH}		Pull up
$\overline{\text{SRESET}}$	OD	Low	1K–10KΩ V_{DDH}		Pull up
$\overline{\text{RSTCONF}}$	I	Tri-stated	As required by reset configuration mode	—	$\overline{\text{RSTCONF}}$ can be tied to ground if the HRCW is to be read from a boot PROM, and it is a configuration master. If it is a configuration slave, the $\overline{\text{RSTCONF}}$ should be connected to one of the master's seven most significant address bits. Otherwise a 4.7KΩ pull-up resistor to V_{DDH} is recommended to accept the default HRCW.
EED	B	Tri-stated	1K–10KΩ V_{DDH}		Pull up
EE0/DBREQ	B	Active	As needed	As needed	Pull up if debug mode to be entered after reset. Pull down for SC140 to start normal processing after reset.
EE1/HPE	B	Active	As needed	As needed	Pull up if the host port is to be enabled at reset. Pull down if host port is disabled.
EE[2–3]	B	Tri-stated	1K–10KΩ V_{DDH}		Pull up
$\overline{\text{BTM[0–1]}}$/EE[4–5]	B	active	As needed	As needed	Pull down for MSC8103 to boot from external memory. Pull down EE4 and pull up EE5 for MSC8103 to boot from host port.
MODCK1/TC0/BNKSEL0	B	Tri-stated	As needed	—	Pull up or pull down per desired clock configuration. Refer to the data sheet for settings.
MODCK2/TC1/BNKSEL1	B	Tri-stated	As needed		Pull up or pull down per desired clock configuration. Refer to the data sheet for settings.
MODCK3/TC2/BNKSEL2	B	Tri-stated	As needed		Pull up or pull down per desired clock configuration. Refer to the data sheet for settings.
CLKIN	I	Tri-stated	As needed		Provide appropriate clock.
DLLIN	I	Tri-stated	none	None	Bypass DLL by setting bit 27 of hard reset configuration word.
PA[6–31]	B	Tri-stated	As needed	None	The parallel port (Port A, B, C, D) pins do not have internal pull-up or pull-down resistors. Unused parallel I/O pins can be configured as outputs after reset and left unconnected.
PB[18-31]	B	Tri-stated	As needed	None	"
PC[4–7, 12–15, 22–31]	B	Tri-stated	As needed	None	"
PD[7, 16–19, 29–31]	B	Tri-stated	As needed	None	"

Table 7. Signal States and Recommended Termination (Continued)

Signal	Function (1)	State at Hard Reset	Connection		Notes
			If Used	If Not Used	
V_{CCSYN}	Analog		Filtered V_{DD}		Refer to **Section 2**, *Power*. PLL power supply filtering. The V_{CCSYN}/V_{CCSYN1} power signals on the MSC8103 device provide power to the clock generation phase-locked loops. To ensure stability of the internal clock, the power supplied to these pins should be filtered with capacitors that have low and high frequency filtering characteristics (0.01µF and 10 µF). V_{CCSYN}/V_{CCSYN1} can be connected to V_{DD} through a 10W resistor. GND_{SYN} and GND_{SYN1} can be tied directly to the V_{SS} (GND) plane. Use a circuit similar to the one shown in **Figure 2**.
V_{CCSYN1}	Analog		Filtered V_{DD}		Refer to **Section 2**, *Power*. PLL power supply filtering. The V_{CCSYN}/V_{CCSYN1} power signals on the MSC8103 device provide power to the clock generation phase-locked loops. To ensure stability of the internal clock, the power supplied to these pins should be filtered with capacitors that have low and high frequency filtering characteristics (0.01µF and 10 µF). V_{CCSYN}/V_{CCSYN1} can be connected to V_{DD} through a 10W resistor. GND_{SYN} and GND_{SYN1} can be tied directly to the V_{SS} (GND) plane. Use a circuit similar to the one shown in **Figure 2**.
SPARE1		Tri-stated	Open	Open	This pin should be left disconnected.
SPARE5		Tri-stated	Open	Open	This pin should be left disconnected.
THERM[1–2]		Thermal	Open	Open	These pins should be left disconnected.

1. I = input, O = output, B = bidirectional three-state, OD = open-drain. Most multi-function pins are bidirectional three-state. This does not imply that they are all shared signals—only that they may be used as inputs or outputs.

11 Related Reading

The reference materials listed in **Table 8** are available at the web site listed on the back cover of this application note. Visit the relevant product summary page or search by title or document identification number (Document ID).

Table 8. MSC8103 Documents

Document Category	Document Title	Document ID
Data Sheet (Hardware Specifications)	*MSC8103 Technical Data* Sheet	MSC8103
Errata (device)	MSC8103 Silicon Errata	

Table 8. MSC8103 Documents (Continued)

Document Category	Document Title	Document ID
Manuals	*MSC8103 Reference Manual*	MSC8103RM
	MSC8103 Programmer User's Guide	MSC8103UG
	SC140 DSP Core Reference Manual	MNSC140CORE
Application Notes	*Functional Pin Difference Between the MSC8103 and MPC8260 Communications Processor Modules*	AN1851
	Initializing the MSC8103 Communications Processor Module (CPM) I/O	AN1854
	Using the SC140 Enhanced OnCE Stopwatch Timer	AN2090
	Clock Mode Selection for MSC8103 Mask Set 0K87M	AN2306
	Bootstrapping the MSC8103 Device Through the HDI16 Port	AN2311
Reference Design	*MSC8103 Application Development System*	MSC8103ADSUM

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Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

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Technical Information Center
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+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

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