

# Implementing PFC Average Current Mode Control using the MC9S12E128

## Addendum to Reference Design Manual DRM064

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This application note is intended as an addendum to the *Design Reference Manual DRM064* ([1]) and describes implementation of an average current mode control of Power Factor Correction (PFC) on MC9S12E128. The DRM064 deals with the design of a Single Phase On-Line UPS using an MC9S12E128. It includes control of a power factor correction (PFC), a DC/DC step up converter, a battery charger, and an output inverter.

The current UPS Reference Design (described in [1]) utilises so-called indirect PFC control. Indirect PFC means that the voltage (outer) control loop is performed digitally by the microcontroller. The output of the voltage control loop is converted by a D/A converter to an analogue signal, which acts as a current reference to the current (inner) control loop. The inner loop is executed by external hardware, which is implemented as an hysteretic controller working in continuous conduction mode (CCM).

The use of the indirect control approach reduces instruction loading of the MCU, since the current control loop requires high bandwidth. On the other hand, this approach needs additional hardware and does not take

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complete advantage of digital control, such as higher noise immunity, greater flexibility, fewer components, and so on.

This application note discusses a fully digital control technique; namely, an average current mode. The PFC running in average current mode utilises continuous conduction mode, so this control approach is suitable for medium and higher power applications.

# 1 Average Mode Control Theory

The control structure is similar to the indirect control, and is divided into two: an inner and outer control loop as shown in Figure 1. The outer voltage control loop is identical to the original. It keeps a constant voltage on the DC bus. The voltage control loop utilises a PI controller and the output defines amplitude required for the PFC current.

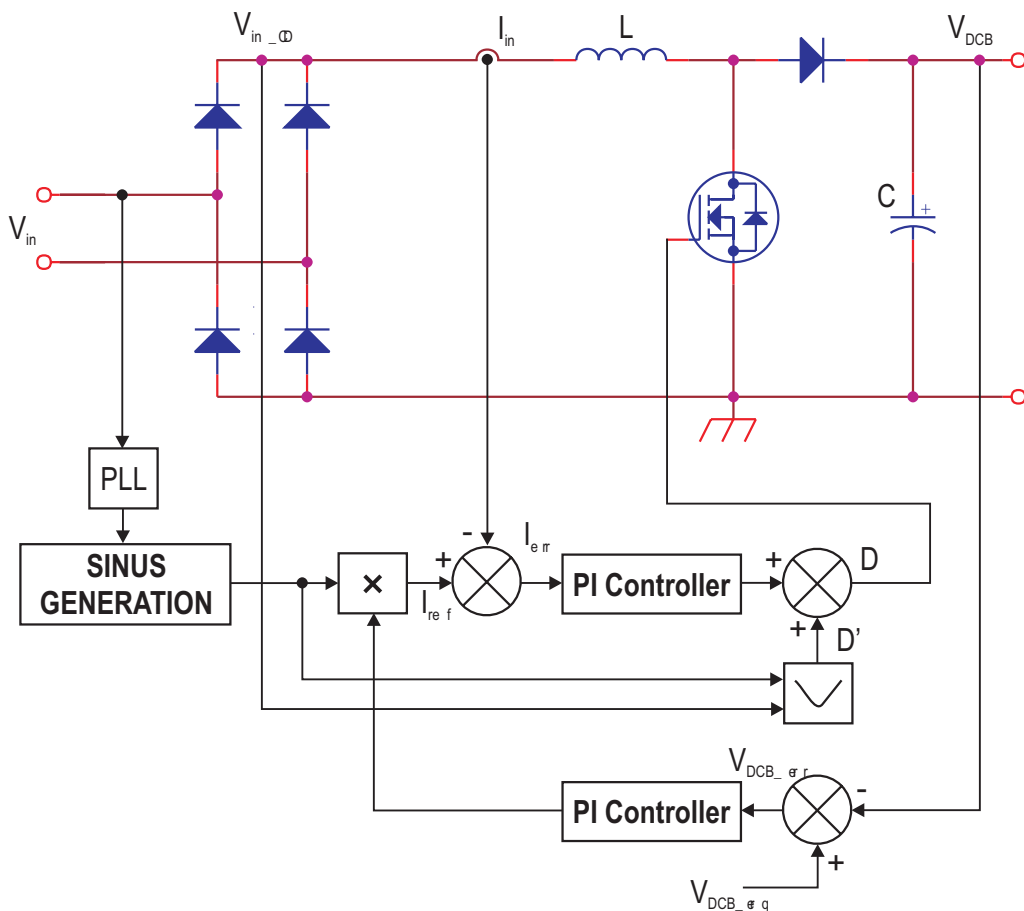


Figure 1. Average Mode Control Block Diagram

The inner current loop has a different structure to the original one used. First, the control loop is implemented via software in the microcontroller, which directly controls the PFC transistor. Second, the control loop employs the PI controller to maintain the sinusoidal input current. The inputs to the PI controller are  $I_{err}$ , as the difference between the current reference,  $I_{ref}$  and the actual current  $I_{in}$ . The sinusoidal waveform of  $I_{ref}$  can be derived from the shape of the input voltage  $V_{in\_DC}$ , or as shown in

Figure 1, generated digitally by a sinwave generator synchronised with the main input voltage  $V_{in}$ . The final current reference,  $I_{ref}$ , is acquired by multiplying a unitary sine waveform by the output of the voltage controller. The current PI controller's output is summed by the feedforward block, which compensates for variation in the input voltage. The feedforward block generates a signal,  $D'$ , corresponding to the duty cycle of a boost converter in an open loop, expressed as

$$D' = \frac{V_{DCB} - V_{IN\_DC}}{V_{DCB}} \quad \text{Eqn. 1}$$

where:

$V_{DCB}$	= DC bus voltage
$V_{IN\_DC}$	= rectified input voltage
$D'$	= duty cycle of PWM transistor

The resultant signal  $D$  defines the duty cycle of the PFC transistor. The bandwidth of the current PI controller has to be set above 8 kHz to get a sufficient response. Therefore the current PI controller algorithm has to be executed at least once every 60  $\mu$ s, which puts a lower-limit requirement on the performance of the microcontroller. The MCU performance requirement for the voltage control loop remains unchanged. And since the bandwidth of the voltage control loop is set below 20 Hz, the MCU performance is not a limiting factor in this part of the PFC algorithm.

## 2 Hardware Implementation

The PFC circuit uses the same components (inductor, capacitor, transistor, current sensor, etc.) as in the original design described in [1]. The design changes lie in the control and sensing signals only. The PFC transistor is directly connected to the PMF module, channel 0. The inductor current is sensed by the A/D converter, channel 6. The input voltage (AN11), top (AN7) and bottom (AN8) voltages are unchanged. The overview of all the control signals used in the average current mode PFC control is depicted in Figure 1.

## 3 Software Implementation

As with the hardware, small changes were made to implement the average current mode control in software. The voltage control loop remains unchanged, and is still running in the 1 ms interrupt. The current loop was integrated into the fastest (50  $\mu$ s) interrupt as shown in Figure 2. The current controller utilises a recursive algorithm for fast execution time.

Next, the conversion of analogue values were rearranged. The input current was routed to channel six since the A/D converter doesn't allow a change in the order of samples. Now the fast conversion converts the output current, output voltage and input current in one sequence. The overview of all sensed quantities can be seen in Table 1. The difference between the fast and slow conversion is explained in [1].

The output of the current controller is summed by the feedforward block. The feedforward block performs calculations according to Equation 1. Since the hardware design allows measuring the average value of the input voltage only, the waveform of  $V_{in\_DC}$  is generated using the sinewave generator. The result of the summation defines the duty cycle of the PFC transistor.

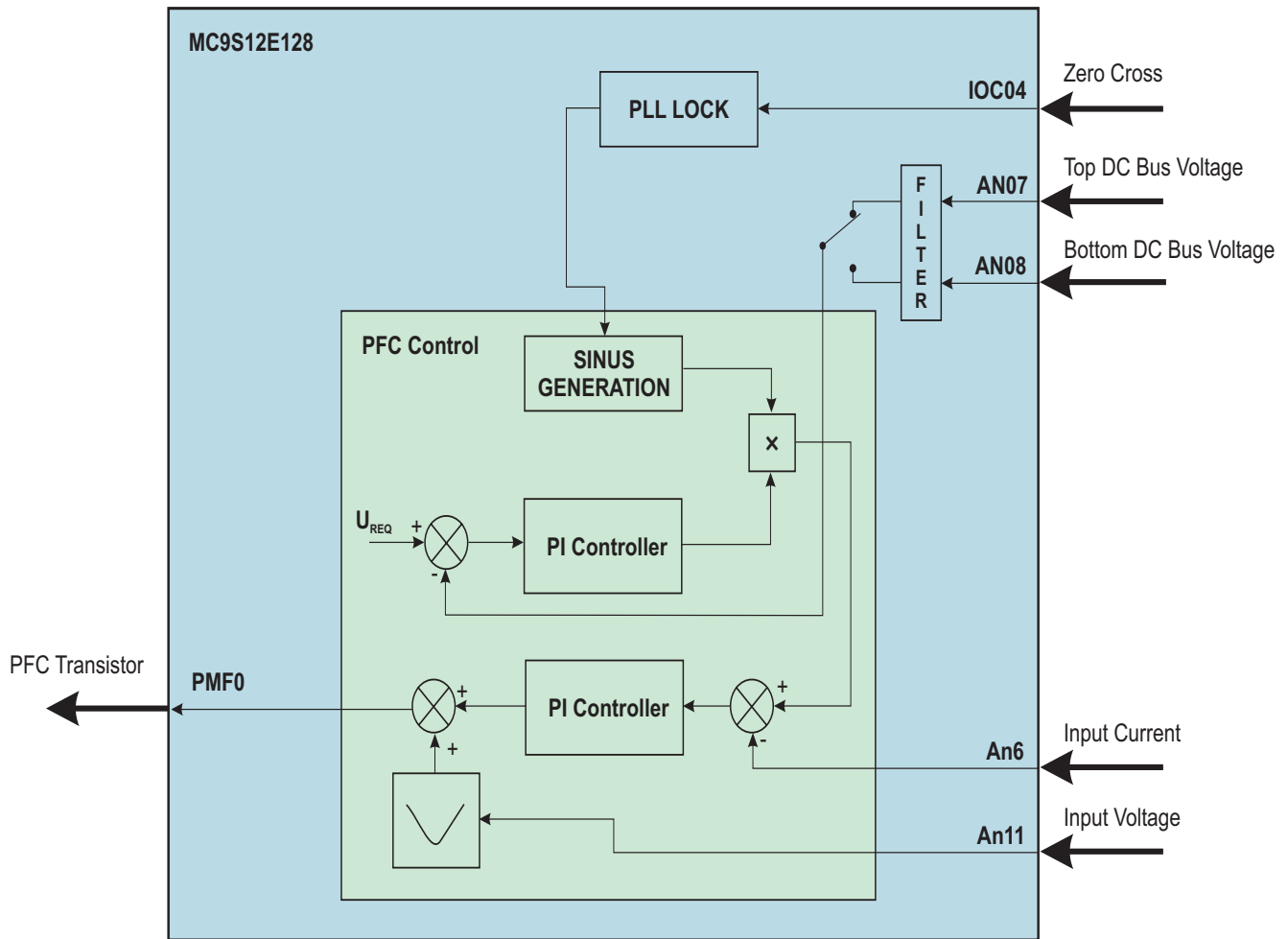


Figure 1. Average Current Mode PFC Algorithm Implemented with MC9S12E128

The switching frequency of the PFC transistor is set to 40 kHz in order to be a multiple of the current loop execution frequency (20 kHz). This constant switching frequency of the PFC transistor simplifies the design of the input filter.

Table 1. Overview of Sensed Quantities

Quantity	Type of Conversion	Conversion Period
$I_{OUT}$	fast	50 $\mu$ s
$V_{OUT}$	fast	50 $\mu$ s
$I_{IN}$	fast	50 $\mu$ s
$V_{IN}$	slow	300 $\mu$ s
$V_{DCB\_TOP}$	slow	100 $\mu$ s
$V_{DCB\_BOT}$	slow	100 $\mu$ s
$I_{BAT}$	slow	300 $\mu$ s
$V_{BAT}$	slow	300 $\mu$ s
Temp	slow	300 $\mu$ s

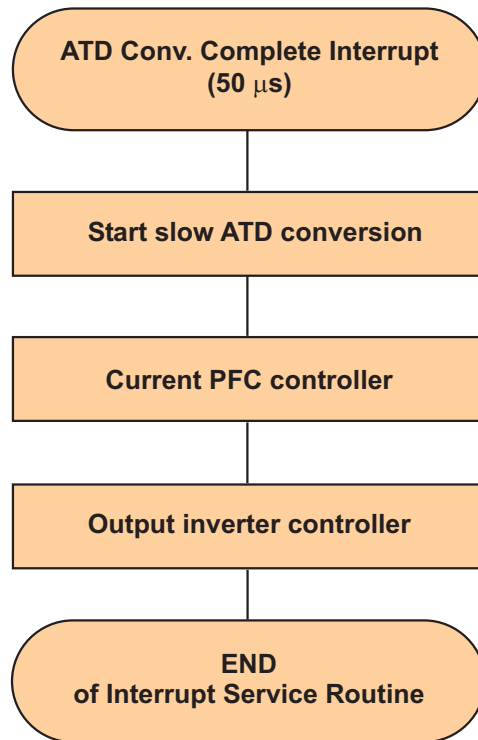


Figure 2. New Structure of ATD Conversion Complete Interrupt

### 3.1 MCU Loading and Interrupt Execution Time

The execution time of periodic interrupts were measured by oscilloscope. The results can be seen in [Figure 3](#). The blue colour represents a PMF reload interrupt, cyan is an ATD complete interrupt, violet shows a 1 ms interrupt and the green colour is a 50 ms interrupt. The total estimated MCU load is 77.5%. The execution time of each interrupt can be seen in [Table 2](#), and the code size in [Table 3](#). As shown in [Table 2](#), the implementation of average current mode control requires 12.3% more MCU execution time over the indirect approach.

Table 2. Execution Time Of Periodic Interrupts

Name	Execution Period	Execution Time
PMF Reload Interrupt	50 $\mu$ s	15.8 $\mu$ s
ATD Conversion Complete Interrupt	50 $\mu$ s	19.4 $\mu$ s
TIM0 CH4 Input Capture Interrupt	8.3 ms or 10 ms	7.8 $\mu$ s
TIM0 CH5 Output Compare Interrupt	1 ms	69 $\mu$ s
TIM0 CH6 Output Compare Interrupt	50 ms	43.4 $\mu$ s

Table 3. Size of UPS Application Code

Memory Type	Size in Bytes
FLASH	11380
RAM	2547
Stack	512

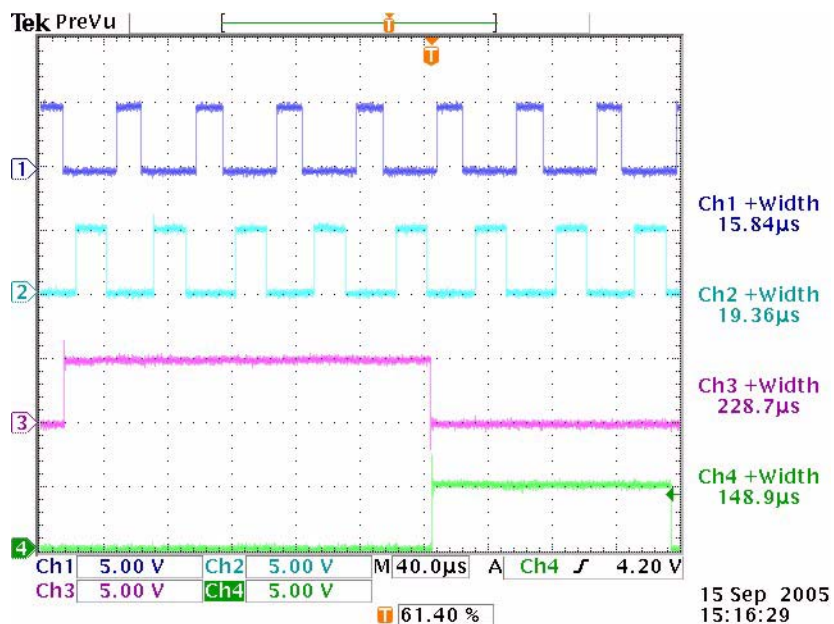


Figure 3. CPU Load of UPS Application

## 4 Conclusion

The average current mode control of the power factor correction has been tested in the UPS reference design described in [1]. The results can be seen in Figure 4 and Figure 5. Figure 4 shows the input current at the full UPS load. Figure 5 depicts the response of the PFC controller on a load step.

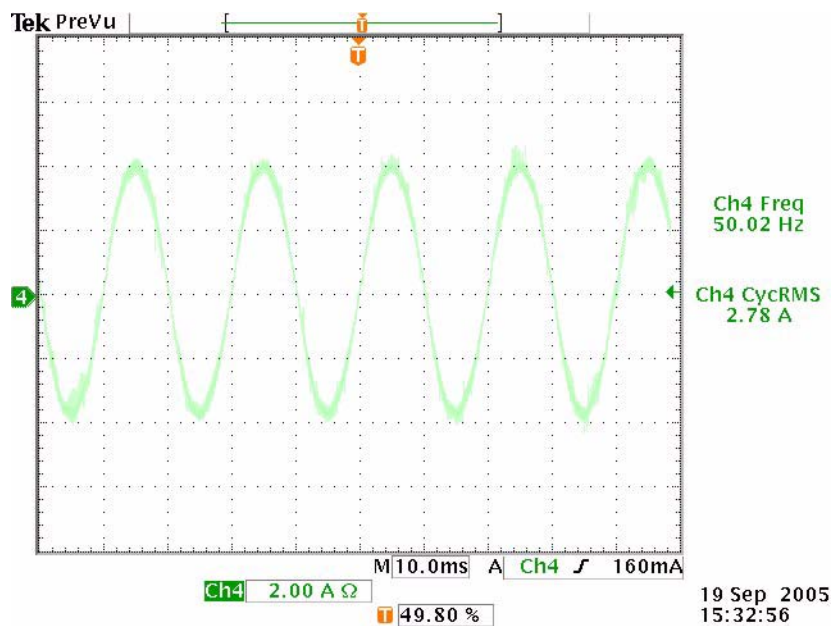


Figure 4. Input Current of the UPS

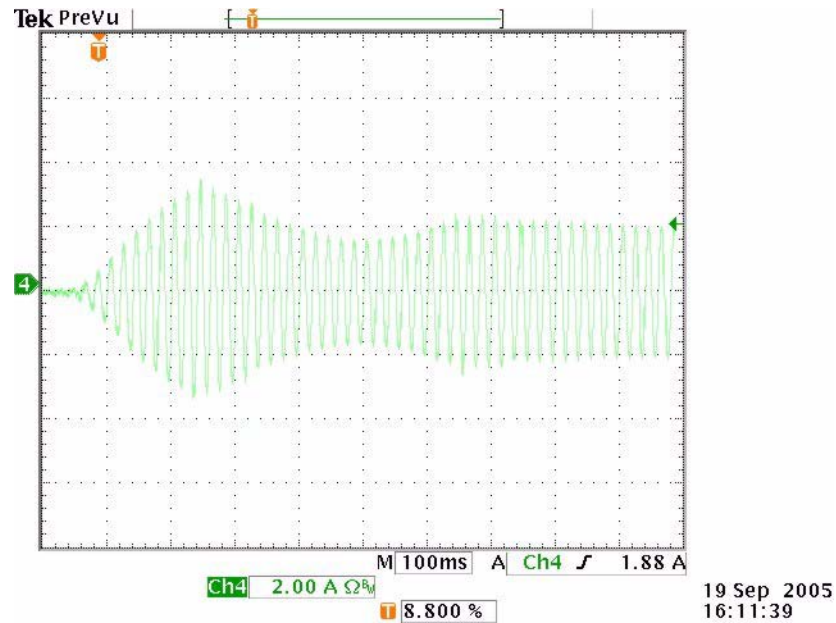


Figure 5. Response of the PFC Controller on Load Step

## 5 References

- [1] I. Feno, P. Grasblum, P. Stekl, "Single Phase On-line UPS using MC9S12E128," *Design Reference Manual DRM064*, Freescale 2004.
- [2] R. W. Erickson, D. Maksimovic, *Fundamentals of Power Electronics*, second edition, Springer Science + Business Media, Inc., 2001.
- [3] M. Xie, *Digital Control for Power Correction*, thesis, Virginia Polytechnic Institute and State University in Blacksburg, June 2003

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