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Application Note

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Design Rules for the HPC II Evaluation Platform

by *Michael Everman*
DSD Applications
Freescale Semiconductor, Inc.
Austin, TX

This document describes the design rules used for the High-Performance Computing Platform II (HPC II). Specifically it addresses issues for the design of the circuit board, such as layout, power supplies, and so forth. For details on the HPC II platform, consult *HPC II—A High-Performance, Low-Profile Server System (HPCIIUG),* which is available at the website on the back cover of this application note.

Contents

1 Features

The features of the HPC II board are as follows:

- Processor
  - — MPC7448 or MPC7447A
  - — 200 MHz front-side bus
- North bridge
  - — Integrated ethernet controllers: two 10/100/1000 BASE-T ports
  - — Two DDR2 DIMM sockets: up to 4 Gbyte at 400 MHz
  - — PCI/PCI-X bus

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  - Two user-defined slots supporting PCI 2.3 at 33-66 MHz and PCI-X at up to 133 MHz
  - SATA and USB
  - Isolation of unused portions of bus to maximize frequency
- Host Local Port
  - 16MB Flash (32-bits wide)
  - PromJet flash emulator support option
  - 8K non-volatile SRAM
  - Real-time Clock
- DUART
- Integrated clock generator
- I^2C

- SATA Disk Controller
  - Four channels
  - RAID-1 Support
- USB Interface
  - UHCI/EHCI USB 2.0 Interface
  - Two ports on stacked USB header
  - Two ports on PCB header (mates with standard PC chassis connectors)
- System Logic
  - Manages system reset sequencing
  - Manages system bus and PCI clock speeds
  - Controls system and user LED monitoring
  - Manages optional fan PWM control
  - Implements registers for system control and monitoring
- Clocks
  - Supports use of the internal clock generator on the TSI108

In addition, it is helpful to mention what is *not* supported on HPC II. HPC II is not a desktop machine, so it does not include:

- Video
- Audio
- Floppy
- Gameport
- Parallel Port

These features are not typically needed on a server and waste power and create additional heat. If needed, the slots on the PCI/PCI-X bus can be used.

2 System Architecture

Figure 1 shows the overall architecture of the HPC II system.

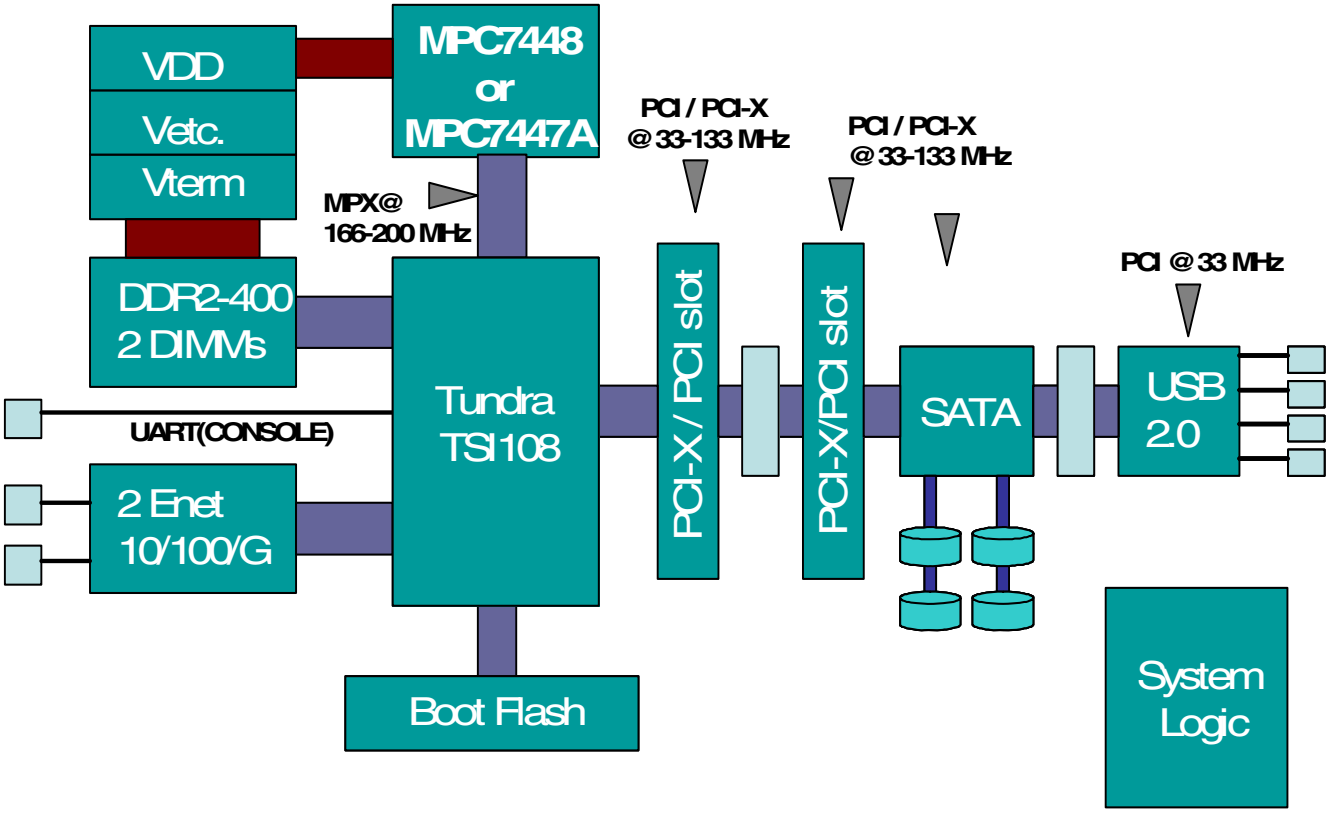

Figure 1. HPC II Block Diagram

3 Board Design

The PCB dimensions and mounting holes are based on the Micro-ATX standard V1.2. The HPC II uses 16 layers: 9 signal layers, 6 power/ground layers, and 1 split layer for the TSI108 3.3 V power rail and signals. The suggested stackup is shown on page 4 of the schematics. Reducing the layer count is likely to increase routing time significantly. For HPC II, considering the small volumes in which evaluation boards are produced, the savings benefit of a reduced layer count does not justify the increased routing effort.

3.1 Components

Components are as noted in the bill of material (BOM), except for these “non-components” or custom components:

mtg	A ATX chassis mounting hole, connected to ground.
tp_pth	A test point implemented as a plated-through hole. All other test points are “25 mil” pads, or circular 0.1”.
splice	A pair of “tp_pth” test points with a 1 inch trace between the pads.

3.2 Placement

3.2.1 General Rules

In general, none of the resistors, ceramic capacitors (no tantalums or electrolytics), or ferrites on the bottom of the board should exceed ~0.1 inch. An exception is the 74CBT16211 bus switches in order to place them as closely as possible to the end of each segment of the PCI bus.

3.2.2 Bypass Capacitor and AVDD Filter Placement

Bulk and high-frequency bypass capacitors are shown on the power supplies of each device on the schematic page; these capacitors must be located very close to the power pin. For the VCORE power rail, which supplies the core power for the MPC7448, there are several additional bypass capacitors which should be distributed along the VCORE plane between the power supply and the MPC7448.

The MPC7448 microprocessor, TSI108 bridgechip, 88E111 ethernet transceivers, 88SX5040 SATA controller, VT6214 USB controller, and APA150 FPGA all have analog circuits with separate power (AVDD) rails that require filter circuits to minimize noise on the analog supplies. These filter circuits are shown on the power supplies of each device on the schematic page. (See Section 3.3, “Specific Rules.”) They must be placed as closely as possible to the device, using short traces and minimal vias. In most cases, the pins for these supplies are located near the periphery of the device, making these requirements easy to meet.

3.2.3 Suggested Placement

The recommended placement of components is shown in Figure 2. The placement of the PCI slots is dictated by the Micro-ATX specification. The MPC7448 and TSI108 are oriented and placed to optimize the flow of the signals for each bus, as shown in Figure 3. Priority is given to the fastest interfaces. The MPX and DDR2 interfaces have top priority, and the relatively slow local (HLP) bus has low priority and therefore can follow a more circuitous path.

The DDR2 DIMMs are adjacent to the side of the TSI108 containing the pins for that interface which opens a channel of unimpeded airflow to facilitate heat transfer from the CPU. This is an advantage if the board is mounted in a 1U chassis and a low-profile passive heatsink is required.

A special case is the PCI/PCI-X bus, which is designed so that portions of the bus can be shut off to support higher frequencies. Routing to the first slot, which is the sole element in the first segment of the bus, should minimize and match trace lengths so this slot can operate at 133 MHz in PCI-X mode if the remaining segments are isolated from the bus. The bus then flows through the first set of bus isolators and on to the second slot, which is the first device on the second segment. The SATA controller is placed at the end of the second segment to speed up bus frequencies if the two slots are empty and the third segment is isolated. By default, a resistor option is populated that limits the bus to 66 MHz if the second segment is enabled. Routes on this segment should maintain length matching. The USB controller resides on the third segment. Because this device supports only the 33 MHz PCI bus, which constrains the entire bus when the third segment is enabled, routing in this segment has a lower priority than other segments of the bus and traces are allowed be longer. Routes on this length must also be matched so that the entire bus is length matched when all three segments are enabled.

The placement of the SATA controller and connectors results in traces longer than recommended by the chip manufacturer. However, it represents a compromise necessitated by the height restrictions around the PCI slots between two competing needs:

- To allow for use of a PCI riser card if the board is mounted in a 1U chassis which prevents vertical connectors from being used near the SATA controller.
- To allow enough clearance to plug cables into horizontal connectors if the board is mounted in a Micro-ATX desktop case, which precludes use of horizontal connectors on the left edge of the board.

The SATA interface is a high-speed serial bus designed to operate over relatively long cables. Therefore, the long traces on the board should have little negative impact except perhaps to require shorter cables to connect drives to the board. Shorter cables are not an issue because the bottom of the board is closest to the drive mounting bays in a typical case or chassis.

The placement of the remaining components is largely determined by height restrictions, accessibility, and routing convenience. Section 3.3, “Specific Rules,” contains specific guidance on the placement of individual components not mentioned above.

The diagram in Figure 2 includes a region allocated for a passive heatsink that is near the I/O area on the top, the DIMM slots on the right, the border of area A (as defined in the Micro-ATX specification) on the bottom, and PCI slot 1 on the left. Components higher than 2.7 mm should not be placed in this region because they may interfere with the mounting of the heatsink. Two sets of heatsink mounting holes are provided. The inner set are for either a small passive heatsink or the standard fansink used on Freescale evaluation boards for the MPC7450 family of microprocessors. The outer set are provided for a larger passive heatsink. Note that the keepout area and the mounting holes are strictly to facilitate heatsink design and are not as a specification for heatsink size or design. A heatsink need not use this entire area and can use the mounting holes appropriate for a particular design.

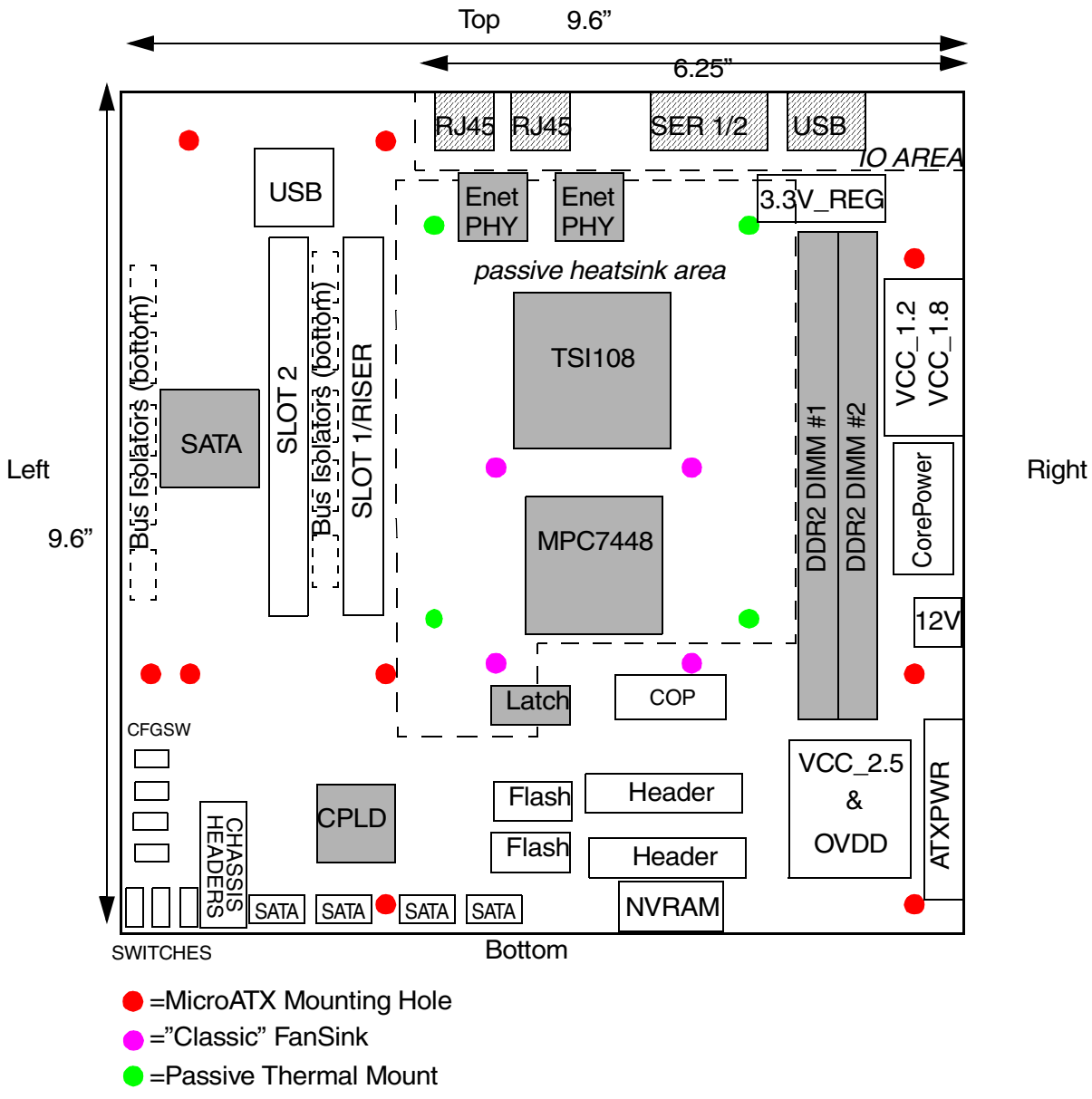

Figure 2. Placement Guide

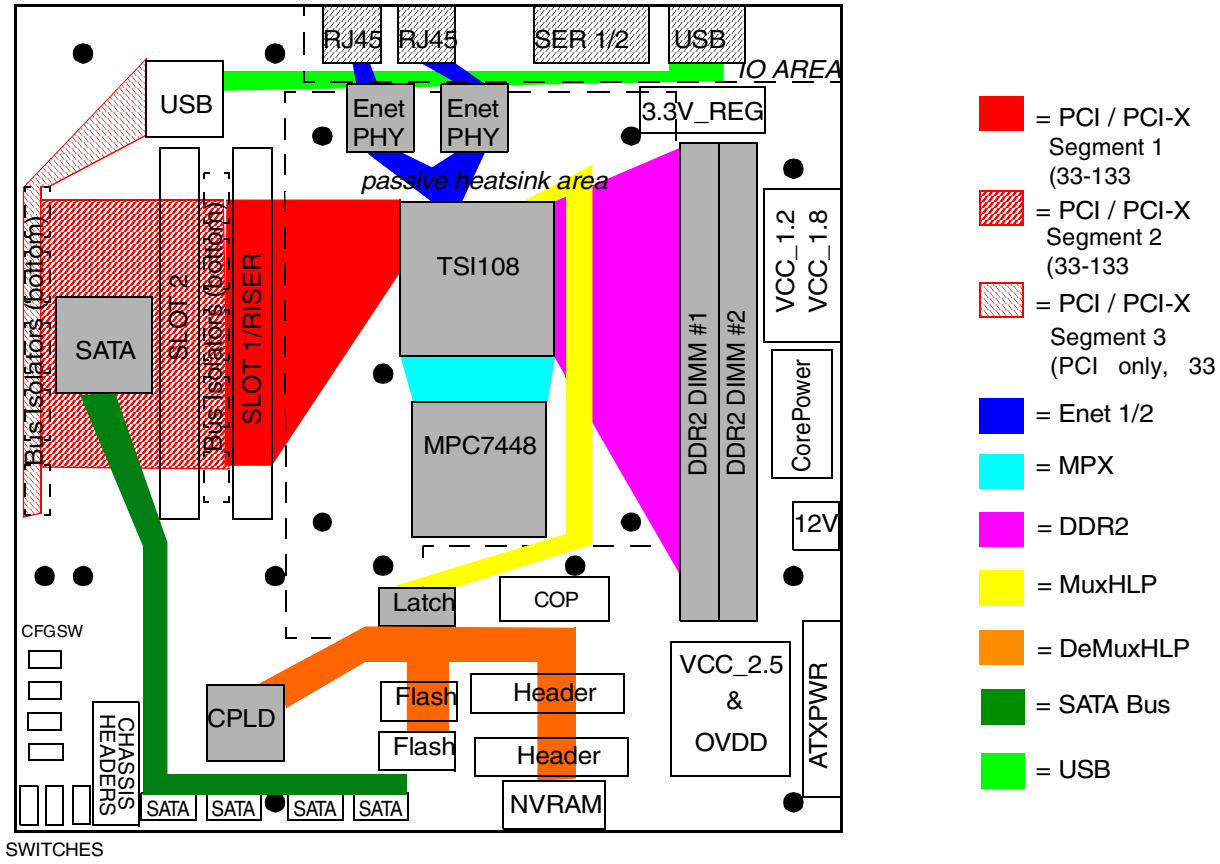

Figure 3. Bus Flow Guide

3.2.4 Routing

Routing is constrained by a combination of electrical classes and differential pair notations. Table 1 lists the electrical classes, and Table 2 lists the differential pairs.

Table 1. Electrical Classes for Routing

Electrical Class Name	Description	Restrictions
1CM_MAX	Restricts traces to 1 cm total.	No vias
2CM_MAX	Restricts traces to 2 cm total.	1 via maximum
1MM_MAX	Restricts traces to 0.1 cm total.	No vias
5MM_MAX	Restricts traces to 0.5 cm total.	No vias
DIFF_SATA	Matched length traces to within 500 µm. in combination with differential pairs SATA[0:3]_[T,R]	Layer 1/2 only No stubs Match to 500 µm 45 degree corners optional
DIFF_USB	Matched length traces to within 100 mil in combination with differential pairs USB[1:4] and USBO[1:4]	Over ground plane. Match to 10 mil.

Table 1. Electrical Classes for Routing (continued)

Electrical Class Name	Description	Restrictions
DIFF_PHY	Matched length traces to within 100 mil in combination with differential pairs PD[00:07]	Layer 1/2 only No stubs
DDRCLK	Same matched length as DDR_CTL in combination with differential pair MCK/MCKT	See Tundra's *TSI108 Hardware Manual* for layout instructions for these signals.
DDRCTL1	DDR2 control signals to DIMM1 before series terminator	
DDTCTL2	DDR2 control signals to DIMM2 before series terminator	
DDRCTL12	DDR2 control signals shared by both DIMMs (no series terminators)	
DDRCTL1T	DDR2 control signals to DIMM1 after series terminator	
DDTCTL2T	DDR2 control signals to DIMM2 after series terminator	
POWER_TRACE	Power connections to multiple components	Min width: 1/10" If connecting to a plane, use power vias.
TSEC(1:2)	Matched lengths to within 100 mil	No stubs due to pullup/pulldown.
MPX	Matched length, within 100 mil	3 vias maximum: 1 at each device to allow for breakout, and 1 along the route to ease routing.
SYSCLK1	Match lengths to MPC7448 and TSI108	
PCI	Match lengths each segment of PCI bus (to each component) and total lengths within 0.3 in.	
PCICLK	Matched length, within 0.1 in.	
PHYCLK	Matched length, within 0.1 in.	
SHORT	Same as 1CM_MAX	
SHORT_POWER	Same as POWER_TRACE, but <= 1 cm.	

Table 2. Differential Pairs for Routing

DiffPair Name	Description	Trace Width/Sep.	Max Vias	Z
SATA[0:3]_[T,R]	SATA differential pairs	6/6/12	0	100Z
USB[1:4]	USB pair (pre-termination)	6/6/12	2	100Z
USBO[1:4]	USB pair (post-termination)	6/6/12	0	100Z
PD(00:07)	PHY pairs	6/6/12	0	100Z
DL[0:8]	DDR2 data pairs and strobes	See the Tundra *TSI108 Hardware Manual*.		
DDRCIK(0:5)	Memory clock	See the Tundra *TSI108 Hardware Manual*.		
DDRFBCLK1 DDRFBCLK2	Memory clock feedback, has specific requirements	See the Tundra *TSI108 Hardware Manual*.		

Table 2. Differential Pairs for Routing (continued)

DiffPair Name	Description	Trace Width/Sep.	Max Vias	Z
MCKOUT	Memory source clock	6/6/12	0	100Z
THERM_DP	Temperature diode differential pair	6/6/12	2	100Z

3.3 Specific Rules

This section provides specific guidance and comments for the components on each schematic page. The page numbers cited below refer to page numbers in the *HPC II Schematics*.

Page 5

- The electrolytic capacitors should be near the ATX power connector, but not so near the locking tab that a human hand cannot easily remove or install it.
- The three switches should be in the lower left and clearly labelled. The chassis switch headers should be nearby but not so close to the switches that they interfere or are a hazard.
- The two three-pin fan headers should be located along the upper right side of the board, outside the area marked “passive heatsink outline”.
- The signal VCC_HOT_5 should be a wide trace (~0.1”).

Page 6

- The nets connected to the SW, HDRV, and LDRV pins should be short and of normal thickness; however, extra trace separation should be used.
- The high-side FETs (upper half of dualFET) derive power from the +12V rail, so +12V will must be substantial (roughly 1.5A per switcher (12W) or 3A total). Most likely a power plane split, but area fill is possible. If it is a plane, several power/no-clean vias to the plane sufficient for 4A are required.
- The low-side FETs (bottom half) should have several power/no-clean vias to ground.
- The common FET path must be a solid area fill sufficient for 6A. No thermal reliefs can be used on the FET or the inductor.
- The resistors sensing the voltage and current should be placed so that they end on the planes. Do not extend the plane to the resistor; move the resistor. Do not allow noisy traces to cross over these lines.
- The output of the inductor should be an area fill that encompasses the lytics/tantalums before dropping down to the split plane. The ceramic capacitors should be distributed at 33 percernt and 66 percent along the length of the plane from the lytic/tantalums. This applies only to points that actually use the plane; planes/split-planes should fill the plane and not have significant voids. If the plane is extended only to prevent voids and not because it is used in a particular area, base the distribution of those capacitors on the vias that actually tie into the plane.
- The nets on the BOOT pins are likely to be noisy and should have extra separation, and be somewhat thicker (say 12 mil).
- The fault LEDs should be nearby.

Page 7

- Same as for page 6.

Page 8–9

- The AVDD filtering must be short.
- The programming header must be <= 3 in. from the device.

Page 11

- PCICLK can be up to 133 MHz. Route these signals to matching lengths within 0.1 in. The series terminations must be close.
- CLK_25_x can be up to 25 MHz. It must be routed to matching lengths within 0.1”. The series terminations must be close.
- The MPC9817 can be placed wherever convenient to routing.
- The crystal must be very close to the MPC9817.

Page 12

- Orient and place the processor so that the CPU bus (MPX class) is the shortest and most easily routed bus. All routes should be matched to within 50 mils.
- Route the following signals on the upper layer: $\overline{\text{TS}}$, $\overline{\text{AACK}}$, $\overline{\text{TA}}$, $\overline{\text{BR0}}$, $\overline{\text{BG0}}$. If there is a special testpad, that will not interfere with routing (no stubs).
- The CPUCLK signal routes to a test point; the associated ground testpoint pad must be 0.1 in. nearby (like a Berg header but not a component).
- The AC termination on the SYSCLK pin should be very near the BGA pad.
- A height clearance zone around the processor is needed to allow the fansink to be mounted.

Page 13

- The high-frequency bypass capacitors for VCORE must be directly connected to the vias to the power and ground pins. Several additional bypass capacitors should be distributed along the VCORE plane between the power supply and the MPC7448.
- The bypass capacitors for OVDD can be placed on the bottom or around the chip (top or bottom).
- The AVDD filter circuit should be as close as possible to the AVDD pin of the CPU.
- The ADT7461 thermal monitor chip should be placed close to the processor so that the temperature measurement path (TEMP_DP electrical class) can be short and quiet.
- The VDD and G6 test points should be on the top layer, adjacent to each other (0.1 in. apart), and outside the fansink mounting area.
- The fault LED should be near the CPU.
- The JTAG header can be anywhere near the processor that does not interfere with mounting the heatsink or attaching PromJets to their headers.

Page 14

- GENERAL: Up to 24 A may flow out of VCORE, so everything between the VCORE plane and the source +5V plane, must be heavy and unrestricted.

- The VCORE power supply must be placed so that a good split is possible between this section and the MPC7448.
- The FETs need heatsink copper added to the source (pins 1–4); these are two separate fills (or four, if the FETs are on opposite sides of the board). The total area is 10cm~2 for a pair, or half if the FETs are top and bottom.
- All current paths from +5V through the high-side FET to the common, through the low-side FET must be substantial, with wide area fills, no thermal relief, and multiple high-current vias to power ground planes. Similar routing is required from the FET common through the inductor and current-measurement resistor into the capacitor array.
- The current measurement amplifier (INA197) can attach across the sense resistor (R506) with traces; do not extend the power planes just to tie into the INA197 (but the device can be placed near the resistor if it does not impede current flow).
- DH and DL are noisy, and nothing critical should be nearby.
- The fault LED should be nearby.

Page 15

- Switches should be placed in the lower left corner of the board in the order shown (from top to bottom); all switches must have the same pin-1 orientation.

Page 16

- AVDD filter circuit should be placed as closely as possible to the TSI108 BGA pads.
- The AC termination on the PB_SYSCLK pin should be very near the BGA pad.

Page 19

- See page 6.

Page 20

- The high-frequency bypass capacitors for the TSI108 should connect directly to the various power and ground pins (avoid traces where possible) and be distributed beneath the device to provide even coverage.

Page 21

- The SMA connector can be placed anywhere that is convenient for routing and accessible; the terminating resistor and two resistor options should be placed as close as possible for the CG_REF pin.
- The series terminators for the clock output signals should be closely to the TS108 pins.
- The AVDD filter circuit should be as close as possible to the AVDD pins of the TSI108.
- The JTAG header for the TSI108 is not normally populated and can be placed in any out-of-the-way location that is convenient for higher-priority placement and layout.

Page 22

- Use a power trace (~0.1 in.) to connect power to the headers through the current-limiting resistor.
- Position the headers with at least 1 in. between them.
- The NVRAM can be placed where convenient but needs clearance of large devices for about 0.5 in. around it (for snap-hat battery install/remove).

Page 23

- If possible, place these resistors on the top of the PCB.

Page 24

- Tundra provides detailed layout guidelines that differ from typical DDR2 layout recommendations. Refer to the TSI108 hardware manual for layout instructions.
- The filter circuit for the AVDD pins should be as close as possible to the TSI108 BGA pads. The bypass capacitors for VREF should be placed near the SD_VREF pins.
- The SMA connector can be placed anywhere that is convenient for routing and accessible.

Page 25

- The VREF power capacitor should be placed adjacent to pin 1 of the DIMM module.
- The DIMM on this page is closest to the TSI108. Orientation can be flipped to achieve best routing conditions.
- Routing conditions are detailed in the TSI108 hardware manual.

Page 26

- The DIMM on this page is furthest from the TSI108. Orientation can be flipped to achieve best routing conditions.
- Otherwise same as page 25.

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- The VTT termination plane must be a solid area fill at least 0.3 in. thick behind the last DIMM module. VTT resistors attaching to this plane must not use a thermal relief (or at least must use one that provides a substantial connection to the power source).
- The VTT power (LP2997) should be located at the center of the VTT plane. All power paths from the 1.8 V plane to the LP2997 must be significant (multiple high-current vias).
- The SP1 splice is a special non-component used to provide means of attaching a signal (in this case, the feedback voltage sense) to a plane or area fill. The splice must be placed approximately where the capacitors exit into the VTT area fill.

- The VTT capacitors should be evenly distributed among the resistors. The capacitors can be placed behind the resistors so as to not interfere with DDR routing.
- The address and command signal terminating capacitors should be placed 0 to 0.5 inches before DIMM 1.

Page 28

- The TSEC1 and TSEC2 are matched-length buses. For signals in each group, TSEC1 can be different than TSEC2.
- The series resistors must be near the device, as noted.
- The overall length of the TSEC(1:2) bus must incorporate the length of the series resistor. Thus, if TSEC1(8) is 15 cm, and P0_TXD0 is 1cm to the series resistor, then TSEC1(0) must be 14 cm long. Sometimes this is best handled by separating TSEC into a series-terminated half and a non-series-terminated half, but Mentor Graphics BS/RE have no over-all intergroup constraints, so that usually leads to more problems.

Page 29

- The 88E1111 (PHY) should be placed near the connector with space for resistors and minimizing trace length on the MDI signals.
- The MDI signals are differential pairs and have matched length requirements. In addition, the 49.9Ω termination resistors must be placed near the 88E1111 MDI pins. Marvell has an application note showing this; essentially, the MDI traces flow through the 49.9Ω resistor pad with no disruption of the trace flow or length. The other side of the resistors are tied and capacitively coupled to ground on the bottom.

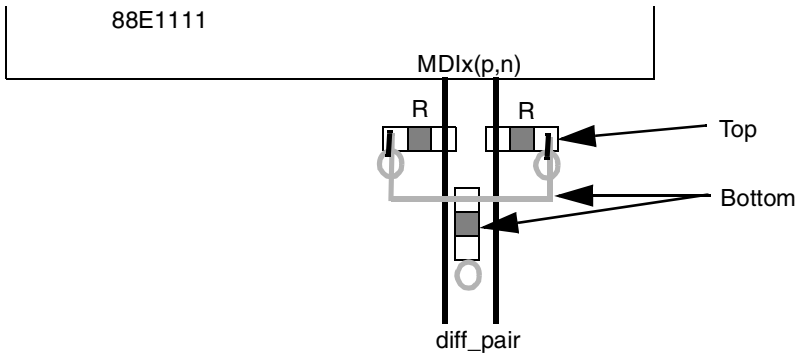

Figure 4. Terminator Placement for MDI Signals

- The resistors can be rotated to assist in routing adjacent MDI pairs.
- The LEDs should be placed near the RJ45 as space permits. The LEDs must have the same stacking order as the other RJ45 LEDs.
- Place the JTRST resistor on the bottom of the board.

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- All same as Page 29.

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- The serial headers should be placed in the ATX IO area to align J11 with a standard gasket alignment and J25 adjacent.

- The serial driver devices (LT1331) should be placed adjacent to the connectors.
- The crystal traces should be very compact and have no adjacent traces.

Page 32

- The AVDD filter circuit should be close to the PCI_PLL_AVDD and PCI_PLL_AVSS pins.
- All PCI bus signals (AD, FRAME, DEVSEL, IRDY, TRDY, STOP, LOCK, PERR, SERR, SREQ64, ACK64, CBE, PAR64, PAR) should be routed to within +/- 0.3 in. Match all trace lengths to each device in the chain so that trace lengths remain matched when portions of the bus are deactivated by the bus switches.

Page 33

- Slot 1 is nearest the TSI108.
- Place the bulk (polarized) capacitors to the left or right of the connector, not above or below where the card edge can protrude. Place the bypass capacitors near corresponding power pins distributed along the length of the connector.

Page 34

- The bus isolation devices should be placed on the bottom of the board between the two PCI slots and arranged to allow best signal layout between the slots.
- See page 32 for notes on trace length matching.

Page 36

- The PLL filtering components (all those on the PAVDD/PAVSS/AV‘DD/AVSS/B*_VAA/B*_VSS pins) must be very short and as near as possible to the BGA pad.
- Power bypass capacitors should be placed on the bottom or secondarily within 1cm of the periphery on the top layer.
- The capacitor on the VREF pin must be very near the BGA pad.

Page 37

- The pins of the SATA connectors must face outward (towards the bottom of the layout) and be in order from left to right. The order can be 0–3 or 3–0, whichever produces a cleaner layout.
- For each SATA connector, route the two pairs of differential pairs on either outer layer (over a ground plane) with no vias. The via count (preferably 0, max of 2) must be the same for all nets on each connector.
- For each SATA port (0:3), place the two corresponding present/activity LEDS near the connector, but do not interfere with the differential-pair routing. The LED signals should be on an inner layer.
- The device failure LED should be placed relatively near the 88SX5040 and labelled accordingly.
- The pullup/pulldown resistors on the JTAG port must be on the bottom.

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- This PCI slot is the furthest from the TSI108, as shown on the layout. Board position is per the ATX/Micro-ATX specifications.

- Place the bulk (polarized) capacitors to the left or right of the connector, not above or below where the card edge can protrude. Place the bypass capacitors near corresponding power pins distributed along the length of the connector.

Page 39

- The bus isolation devices should be placed where convenient. This IC can be placed on the bottom, unlike most other ICs.
- See page 32 for notes on trace length matching.

Page 40

- The USB connector should be placed in the ATX IO area so as to align with a standard ATX gasket.
- The second USB (2×5 header) should be placed on the leftmost side of the board.
- The MIC2077 USB power supplies power to both of the above connectors, so 0.1–0.2” power traces will be needed. The MIC2077 should probably be located about halfway between the sides, near the top of the board.
- The USB signals are differential pairs, with matching lengths. The series resistors should be adjacent to the USB connectors, as shown, and the trace lengths and differential routing applies to both sides. The capacitors to ground and pulldowns must be near the series resistors.
- The crystal and ferrite bead/filters must be short.
- The VCC_2.5 V connection is a split plane.
- The earth ground (also used elsewhere) should be a heavy trace along the ATX IO escape edge.

Page 41

- The LEDs must be grouped as a set, with the legends L1_CLK on the left and L8_SOFT on the right and in order (these have other software functions).
- The second set of LEDs below the above should be placed above in a rectangular array. As with the power monitor, the connection between the LED and the series resistor should be low priority so that the power planes/fills are not extended.
- The 9 mounting holes should be large, plated, grounded mounting holes as described in the micro-ATX specification.
- The test clip points should be placed on each corner of the board. Near the ground pin of the corner bulk capacitors is ideal (not near exposed power pins).
- The I2C header can be placed anywhere convenient and accessible. The pins should be labeled on the top layer silkscreen as noted in the schematic.

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- Place one tantalum in each corner of the board, about 2cm or so (not critical).
- Place the array of 16 bypass capacitors to overlay a grid, about every 5cm or so. Placement is lowest priority over all else (but these can be on the bottom of the board).

4 Document Revision History

Revision	Date	Significant Changes
0	03/10/06	Initial draft

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Europe, Middle East, and Africa:
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81829 Muenchen, Germany
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+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
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Technical Information Center
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