MC34701/2/3 & MC34710) for High End Processors

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1 Purpose
The main purpose of this application note is to highlight the typical requirements (supply voltages, current demands and sequencing) for some high end processors in the market and Freescale’s capabilities of fulfilling those requirements with its power management ICs. Each section will describe the requirements for each of the processors and afterward we will select a Freescale power management IC that could fulfill the requirements for that processor in particular.

2 Scope
The MC34701, MC34702 and MC34703 DC-DC converters combine the capability of having a very efficient synchronous buck converter, typically used to supply the Core voltage on the microprocessors, and a low-dropout (LDO) linear regulator control circuit to provide I/O and bus voltages. Additional to the capability of implementing two DC-DC converters with these devices, they also incorporate specific advanced protection and...
Introduction

describing features for use with high power processors and controllers, including power-up and
power-down sequencing of the I/O and core supply voltages in relation to each other, and voltage
margining.

3 Introduction

Most of the microprocessor units (MPUs) in the market, independent of the end application, are
now requiring several voltage inputs to supply different areas on the device. This need comes
from the trend of increasing the processing capabilities of each of these MPUs, but still
maintaining the same (or even reducing) their power consumption. A typical architecture on
MPUs today is to have the portion of the MPU that is in charge of all the processing, that does
not directly interact with the external world, being supplied by a voltage lower than the one used
by the peripherals in the MCU; this voltage is typically called $V_{\text{CORE}}$, or Logic supply voltage and
can be 1.3V, 1.5V, 1.8V or 2.5V. The supply voltage for the external interfaces, typically called
I/O supply voltage is typically 3.3V or 5V. Sometimes these devices also need to have an
interface with external memories (which could be DDR SDRAM, DDRI SDRAM, DDS SDRAM,
QDR SRAM) requiring an additional voltage supply which typically is 2.5V or 1.5V.

The processors that are going to be analyzed in this application note are:

- AMCC® – NPE405
- AMD® – SC520
- PMC Sierra® - RM7000
- AMCC® - PPC440Gx
- Intel® – IXP45X
- Intel® – IXP2400
- NEC® – VR5500

After showing the characteristics of each of the processors, we will show the basic steps needed
to be performed to configure the power management ICs to have the appropriate output
voltages, sequencing, and how to configure for voltage margining and watchdog configuration.
4 Freescale’s Power Management IC Capabilities

The following table summarizes the basic features of four Freescale power management ICs. As we continue through this document; the reader will see which of the Freescale power management ICs can fulfill the requirements for each of these processors.

<table>
<thead>
<tr>
<th></th>
<th>MC34710</th>
<th>MC34701</th>
<th>MC34702</th>
<th>MC34703</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input voltage range</strong></td>
<td>13V to 32V</td>
<td>2.8V to 6V</td>
<td>2.8V to 6V</td>
<td>2.8V to 13.5V</td>
</tr>
<tr>
<td><strong>Voltage outputs</strong></td>
<td>1 Switching regulator and 1 LDO</td>
<td>1 Switching regulator and 1 LDO</td>
<td>1 Switching regulator and 1 LDO</td>
<td>1 Switching regulator and 1 LDO</td>
</tr>
<tr>
<td><strong>Switching regulator output voltage</strong></td>
<td>(5V or 3.3V)</td>
<td>0.8 V to VIN-Drop-out</td>
<td>0.8 V to VIN-Drop-out</td>
<td>0.8 V to 4.5 V</td>
</tr>
<tr>
<td><strong>Switching regulator current</strong></td>
<td>700mA</td>
<td>1.5A</td>
<td>3A</td>
<td>10 A</td>
</tr>
<tr>
<td><strong>LDO output voltage</strong></td>
<td>Configurable: (3.3V, 2.5V, 1.8V or 1.5V)</td>
<td>Adjustable: 0.8 V to VIN-Dropout</td>
<td>Adjustable: 0.8 V to VIN-Dropout</td>
<td>Adjustable: 0.8 V to 4.5 V</td>
</tr>
<tr>
<td><strong>LDO current capabilities</strong></td>
<td>500mA</td>
<td>1A</td>
<td>1A</td>
<td>2A</td>
</tr>
<tr>
<td><strong>Sequencing</strong></td>
<td>Configurable</td>
<td>Configurable</td>
<td>Configurable</td>
<td>Configurable</td>
</tr>
<tr>
<td><strong>Voltage margining</strong></td>
<td>Not available</td>
<td>Available via I²C</td>
<td>Available via I²C</td>
<td>Available via I²C</td>
</tr>
<tr>
<td><strong>Watchdog</strong></td>
<td>Not available</td>
<td>Available via I²C (window or time-out watchdog)</td>
<td>Available via I²C (window or time-out watchdog)</td>
<td>Available via I²C (window or time-out watchdog)</td>
</tr>
<tr>
<td><strong>Reset timer</strong></td>
<td>Not available</td>
<td>Configurable with external resistor and capacitor</td>
<td>Configurable with external resistor and capacitor</td>
<td>Configurable with external resistor and capacitor</td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td>32 pin SOIC exposed pad</td>
<td>32 pin SOIC</td>
<td>32 pin SOIC</td>
<td>33 terminal PQFN</td>
</tr>
</tbody>
</table>

Table 1. Freescale power management ICs
Using Freescale Power Management ICs to Supply High End Processors

After reviewing the details of each of the processors in Table 1, it can be seen that there are two important features for the MC34701, MC34702 and MC34703 devices’, voltage margining and internal watchdog functionality; both controlled via I²C. The voltage margining functionality allows the user to adjust the output voltage of both the switching regulator and the LDO up to +/- 7%. This feature is particularly useful during system validation. On the other hand, the internal watchdog allows the user to avoid having an IC specifically to perform this task; via the usage of I²C the user can be refreshing the watchdog in two configurations: window watchdog and timeout watchdog.

5 Using Freescale Power Management ICs to Supply High End Processors

In this section, each of the requirements for a set of high end processors in the market are highlighted, showing in a very generic way, how to configure the Freescale power management ICs to supply the voltages and the sequencing needed for those processors.

5.1 Driving the AMCC® – NPE405, AMD® - SC520, PMC Sierra – RM7000 and NEC® - VR5500 microprocessors with the MC34701 or MC34702

The following table highlights the voltage, current and sequencing requirement for these processors:

<table>
<thead>
<tr>
<th>Producer</th>
<th>Processor</th>
<th>Characteristic</th>
<th>Symbol</th>
<th>Voltage</th>
<th>Max. Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMCC®</td>
<td>NPE405H</td>
<td>Logic Supply Voltage</td>
<td>V_DD</td>
<td>2.5 V</td>
<td>1183 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PLL supply Voltage</td>
<td>A_VDD</td>
<td>2.5 V</td>
<td>6.5 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I/O supply Voltage</td>
<td>O_VDD</td>
<td>3.5 V</td>
<td>123 mA</td>
</tr>
<tr>
<td>AMD®</td>
<td>SC520</td>
<td>Core Voltage supply</td>
<td>V_CC_CORE</td>
<td>2.5 V</td>
<td>660 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Real Time Clock Voltage</td>
<td>V_CC_RTC</td>
<td>2.5 V</td>
<td>5 µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Analog Voltage supply</td>
<td>V_CC_ANLG</td>
<td>2.5 V</td>
<td>2.1 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I/O Supply Voltage</td>
<td>V_CC_I/O</td>
<td>3.3 V</td>
<td>120 mA</td>
</tr>
</tbody>
</table>

Sequencing: On the device’s documentation, no voltage sequencing is specified.

Sequencing: Power up Sequence require a 2.5 V (VCC_RTC) power supply to power up before all other VCC, (two 2.5 V and one 3.3 V power supplies are needed), but VCC_RTC is powered from a battery supply. (Review EVB schematics)
Using Freescale Power Management ICs to Supply High End Processors

* Current consumption is not stated on the device’s data sheet. This power dissipation is stated with CPU running at 300Mhz.

Sequencing is: $V_{CCIO}$ should not exceed $V_{CCINT}$ by greater than 2V during the power up sequence.

<table>
<thead>
<tr>
<th>Producer</th>
<th>Processor</th>
<th>Characteristic</th>
<th>Symbol</th>
<th>Voltage</th>
<th>Max. Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMC Sierra ®</td>
<td>RM7000</td>
<td>Supply Voltage internal</td>
<td>$V_{CCINT}$</td>
<td>2.5 V</td>
<td>2.5W total*</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Supply Voltage for PLL</td>
<td>$V_{CCP}$</td>
<td>2.5 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Supply Voltage for I/O</td>
<td>$V_{CCIO}$</td>
<td>3.3 V</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Producer</th>
<th>Processor</th>
<th>Characteristic</th>
<th>Symbol</th>
<th>Voltage</th>
<th>Max. Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>NEC</td>
<td>VR5500</td>
<td>Voltage Supply</td>
<td>$V_{DD}$</td>
<td>1.3 V</td>
<td>2.8W total*</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I/O Voltage Supply</td>
<td>$V_{DDIO}$</td>
<td>3.3 V</td>
<td></td>
</tr>
</tbody>
</table>

Sequencing: Power up sequence requires only that both power supplies are stable within 100 ms.

After reviewing the requirements for each of these processors, the device proposed to supply these microprocessors is the MC34701. The following figure shows the basic configuration needed on the MC34701. If the requirements for the rest of the system increase, Freescale offers a growth path with the MC34702 device (same package and pin assignments); basically the difference between the MC34701 and MC34702 is the output current capabilities for the switching regulator circuitry (as shown in Table 1).
Using Freescale Power Management ICs to Supply High End Processors

For the processors listed previously, some of them require 2.5V and 3.3V and the NEC VR5500 requires 3.3V and 1.3V. Freescale power management ICs give the flexibility of adjusting the output voltage depending on the needs of the application in particular. As shown on Table 1, the MC34701 and the MC34702 can be supplied from 2.8V to 6V and both of its regulator outputs can be configured to supply both the I/O section and the logic or core section.

5.2 Driving the AMCC® – PPC440Gx and the Intel® - IXP45X microprocessor with the MC34702

The following table highlights the voltage, current and sequencing requirement for the AMCC – Npe405 and the Intel IXP45X processors:

<table>
<thead>
<tr>
<th>Producer</th>
<th>Processor</th>
<th>Characteristic</th>
<th>Symbol</th>
<th>Voltage</th>
<th>Max. Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMCC</td>
<td>PPC440Gx</td>
<td>Logic Supply Voltage</td>
<td>VDD</td>
<td>1.5 V</td>
<td>2.2 A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PLL supply Voltage</td>
<td>AXVDD</td>
<td>2.5 V</td>
<td>33 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DDR SDRAM Supply Voltage</td>
<td>SVDD</td>
<td>2.5 V</td>
<td>940 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I/O Supply Voltage</td>
<td>OVDD</td>
<td>3.3 V</td>
<td>111 mA</td>
</tr>
</tbody>
</table>

Sequencing: During chip power-up, OVDD should begin to ramp before VDD. External voltage should not be applied to the chip I/O pins before OVDD is applied to the chip. A power-down cycle should complete (OVDD and VDD should both be below 0.4V) before a new power up cycle is started.
Sequence: Power up sequence required only VCC stable at least 1 \( \mu \)s after VCCp and VCCm.

After reviewing the requirements for each of these processors, the device proposed to supply these microprocessors is the MC34702. The following figure shows the basic configuration needed on the MC34702.

### Table: Voltage Supplies for IXP45X Processor

<table>
<thead>
<tr>
<th>Producer</th>
<th>Processor</th>
<th>Characteristic</th>
<th>Symbol</th>
<th>Voltage</th>
<th>Max. Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel</td>
<td>IXP45X</td>
<td>Voltage supplied to I/O</td>
<td>( V_{CCP} )</td>
<td>3.3 V</td>
<td>2.2 A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Voltage supplied to Oscillator I/O</td>
<td>( V_{CCOSC-P} )</td>
<td>3.3 V</td>
<td>88 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Voltage Supplied to DDR SDRAM</td>
<td>( V_{CCM} )</td>
<td>2.5 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Voltage Supplied to internal Logic</td>
<td>( V_{cc} )</td>
<td>1.3 - 1.5 V</td>
<td>255 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Voltage supplied to analog PLLs</td>
<td>( V_{CCPLLx} )</td>
<td>1.3 - 1.5 V</td>
<td>1630 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Voltage supplied to internal Oscillator</td>
<td>( V_{CCOSC} )</td>
<td>1.3 - 1.5 V</td>
<td></td>
</tr>
</tbody>
</table>

As in this device, there are 3 different voltage supplies needed; the PPC440Gx voltage needs are 3.3V for the I/O supply, 2.5V for the DDR SDRAM interface, and 1.5V for the logic and PLL supplies. Our proposal would be to use a 3.3V LDO to supply the I/O and then use the MC33702 for the 2.5V DDR SDRAM supply and 1.5V for the logic section.
5.3 Driving the Intel – IXP2400 with the MC34703 plus additional LDOs

The following table highlights the voltage, current and sequencing requirement for the Intel – IXP45X processors.

<table>
<thead>
<tr>
<th>Producer</th>
<th>Processor</th>
<th>Characteristic</th>
<th>Symbol</th>
<th>Voltage</th>
<th>Max. Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel</td>
<td>IXP2400</td>
<td>Core Voltage Supply</td>
<td>( V_{CC1.3} )</td>
<td>1.3 V</td>
<td>8.92W (6.86A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PLL Voltage Supply</td>
<td>( V_{CCA1.3} )</td>
<td>1.3 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DDS SDRAM Voltage</td>
<td>( V_{CC2.5} )</td>
<td>2.5 V</td>
<td>3.15W (1.26A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Supply</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>QDR SRAM Voltage</td>
<td>( V_{CC1.5} )</td>
<td>1.5 V</td>
<td>2.67W (1.78A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Supply</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>PCI and Misc. Supply</td>
<td>( V_{CC3.3} )</td>
<td>3.3 V</td>
<td>2.97W (0.9A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reference for DDR DRAM</td>
<td>( D_{v_{REF}} )</td>
<td>1.25 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reference for QDR SRAM</td>
<td>( SN_{V_{REF}} )</td>
<td>0.75 V</td>
<td></td>
</tr>
</tbody>
</table>

Power up Sequence requires: The 3.3V must be brought up before the 1.3V. The 1.3V must be brought up before the 1.5V and 2.5V. The 1.5V must be brought up before or at the same time as the 0.75V. The 2.5V must be brought up before or at the same time as the 1.25V.

After reviewing the voltage, current, and sequencing required for this processor, the MC34703 device can be used for the 1.3V core voltage supply, and the 3.3V PCI, and MISC supply. As in Table 1, the switching regulator current capability for the MC34703 is 10A, and 2A for the LDO; for the 2.5V and 1.5V supplies, typical LDOs could be used. The following diagram shows the typical application diagram for the MC34703.

![Figure 3. MC34703 simplified application diagram](image-url)
Configuring the MC34701, MC34702 and MC34703 to Drive High End Microprocessors

In this section, the basic steps are highlighted to configure the MC34701, MC34702 and MC34703 to fulfill the requirements for the processors listed. Since these 3 devices have the same architecture, the configuration is very similar across the devices, but if there are any differences, they will be highlighted.

All this information has been taken from the datasheets, and also from the application note AN1989 “MC34701 and MC34702 Component Selection Guidelines” The sections we will focus on are:

- How to configure the LDO output voltage and current limit
- How to configure the switching regulator output voltage
- How to configure the MC34701 for proper sequencing
- How to use the margining feature
- How to use the watchdog functionality

There are other portions in the design not focused on; in order to understand these sections please refer to the AN1989 application note or the data sheet of the device. The sections not focused on are:

- Switching regulator compensation loop
- LDO Compensating network
- Boost supply
- Reset capacitor
- Input capacitors
- Output capacitors
- Inductor selection
- LDO Mosfet selection

6.1 How to Configure the LDO Output Voltage and Current Limit

The LDO output voltage is selected by using the appropriate resistive divider for the feedback voltage (LFB, pin 18). In order to properly select the output voltage use the following equation:

\[
V_{LDO} = V_{REF} \left( 1 + \frac{R_U}{R_L} \right)
\]

Equation 1
Configuring the MC34701, MC34702 and MC34703 to Drive High End Microprocessors

Where $V_{\text{REF}}$ is the linear regulator reference voltage ($V_{\text{Ref}} = 0.8 \text{ V} \text{ typ.}$) at the LFB terminal, $V_{\text{LDO}}$ is the LDO selected output voltage, $R_U$ is the “upper” resistor of the LDO resistor divider, $R_L$ is the “lower” resistor of the LDO resistor divider; both $R_U$ and $R_L$ are shown in Figure 1.

![Figure 1. MC34701 and MC34702 Linear regulator circuit](image)

The current limit of the linear regulator can be adjusted by means of an external current sense resistor $R_S$. The voltage drop caused by the regulator output current flowing through the current sense resistor $R_S$ is sensed between the LDO and the CS terminals. When the sensed voltage exceeds 50 mV typical (in case of the MC34703 the typical voltage is 45mV), the current limit timer starts to time out while the control circuit limits the output current. If the overcurrent condition lasts for more than 10 ms, the linear regulator is shut off and turned on again after 100 ms. In order to calculate the value at which the device will have the current limit please refer to the following formula:

$$I_{\text{LIM}} = \frac{50 \text{mV}}{R_S}$$

Equation 2

As an example, we will configure the LDO to supply the I/O section; as has been shown previously, the I/O supply is typically 3.3V. In order to configure the LDO to have a 3.3V output, we first set a value for $R_L$. For this example, we set $R_L$ at 15 kΩ. In order to obtain $R_U$ we solve for $R_U$ in equation 1 yielding to:

$$R_U = \frac{V_{\text{OUT}} - V_{\text{REF}}}{V_{\text{REF}}} = \frac{3.3 - 0.8}{0.8} \times 15k = 46.875k$$
6.2 How to Configure the Switching Regulator Output Voltage

The MC34701 buck regulator output voltage can be set by using the following formula:

\[
V_{OUT} = V_{REF} \left(1 + \frac{R_3}{R_2 \left( \frac{R_3}{R_1} \right)} \right)
\]

Equation 3

For your reference, the buck regulator portion is shown in Figure 5.

We recommend using 1% resistors for better adjustments. For most applications with the MC34701 and MC34702, the following values are suitable:

\[
\begin{align*}
R_3 &= 300 \ \Omega \\
C_2 &= 470 \ \text{pF} \\
R_4 &= 330 \ \text{k}\Omega
\end{align*}
\]

Figure 5. Buck regulator control circuit for the MC34701 and MC34702

Where \(V_{\text{REF}}\) is the buck regulator reference voltage (\(V_{\text{REF}} = 0.8 \ \text{V typ.}\)) at the INV terminal, \(V_O\) is the selected output voltage, \(I_O\) is the output load current, and \(R_L\) is the DC resistance of the inductor L. It is apparent that the buck regulator output voltage is affected by the voltage drop caused by the inductor serial resistance and the regulator output current. In those applications which do not require precise output voltage, setting the formula for calculating selected output voltage can be simplified as follows:

\[
R_2 = \frac{V_{\text{REF}}}{(V_{OUT} - V_{\text{REF}}) \left( \frac{R_1 + R_4}{R_1 \ast R_4} \right)}
\]

Equation 4 Buck regulator output voltage selection
In case you are using the MC34703, an additional compensation network needs to be added. The pin at which this compensation network needs to be added is located on the terminal named COMP (pin 24). Review the data sheet for a more detailed explanation on how to set the compensation network for this device.

We now will configure the Switching regulator to supply the core or logic section of the microprocessor. This voltage could go from 1.3 to 2.5V. If the user wants to have a 2.5V supply for this section, first we set \( R_1 \) to 39k and then solving for \( R_2 \) on equation 3, would lead to the following formula and value for \( R_2 \):

\[
R_2 = \frac{V_{REF}}{(V_{OUT} - V_{REF}) \left( \frac{R_1 + R_4}{R_1 * R_4} \right)} = \frac{0.8}{(2.5 - 0.8) \left( \frac{39k + 330k}{39k * 330k} \right)} = 16.413k
\]

### 6.3 Selecting the appropriate sequencing

Since the typical requirements for the processors are to have the voltage supply for the I/O smaller than the core supply by a certain voltage (i.e. in case of the PMC Sierra RM7000 this would be 2V), and also because the LDO is typically chosen to supply the I/O supply for the microprocessor and the switching regulator to supply the core, the sequencing that has been selected is the standard power sequencing mode. In this mode the switching regulator output is the one that provides the core voltage, and the LDO provides the voltage for the I/O.

The following table highlights the sequencing configurability:

<table>
<thead>
<tr>
<th>EN1</th>
<th>EN2</th>
<th>Operating Mode</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Regulators disabled</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Standard power sequencing</td>
<td>The switching regulator supplies the core voltage and the LDO the I/O voltage</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Inverted power sequencing</td>
<td>The LDO supplies the core voltage and the switching regulator the I/O</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>No power sequencing, regulator enabled</td>
<td>In this case, the sequencing can only be controlled by the input voltages VIN1 and VIN2 are supplied to the IC</td>
</tr>
</tbody>
</table>

Table 2. Operating mode and sequencing selection
6.4 How to use the margining feature

As was shown previously, the voltage margining feature allows the user to adjust the output voltage of both the switching regulator and the LDO. In order to use this function, the user must perform the following steps:

1. Configure the appropriate address for the device. The address for the device is defined by the state of the CLKSEL terminal (A1) and the ADDR terminal (A0).
2. Send the margining programming 1st command (“00100000”).
3. After the address for the device has been appropriately set, the user now needs to communicate via the I2C using the address field “001”, which is the one configured for the voltage margining operation, and the value field required, for either the switching regulator or the LDO. The setting for the value field can be found on the “Command byte definitions” table on the data sheet. For example, if an increase of 6% is needed for the switching regulator, the following command needs to be sent: “00110110”.

If a simultaneous set for both the LDO and the switching regulator is required, the user has to send two commands, one for each supply, in sequence. The following image shows how to send commands. This image shows how to configure the LDO for an increase of 5%.

![Data transfer example - LDO voltage margining](image)

6.5 How to use the internal watchdog

The internal watchdog has the capability of being configured in either window or timeout watchdog. In order to use the internal watchdog the following steps need to be taken:

1. Configure the appropriate address for the device. The address for the device is defined by the state of the CLKSEL terminal (A1) and the ADDR terminal (A0).
2. Send the watchdog programming 1st command.
3. The user now needs to communicate via I2C with the address field for the watchdog (“011”), and the appropriate value for the watchdog timeout and type (window or timeout).

The following image shows how the commands need to be sent to initialize the watchdog in order to have a time-out watchdog configuration.
7 Conclusion

The main purpose of this application note is to show the capabilities of Freescale's power management ICs to supply high end microprocessors. A basic description of the configuration that needs to be done was shown, but of course a more detailed analysis must be performed to adapt the usage of any of Freescale’s power management ICs for any particular application. The designer not only needs to take into account the power requirements for the microprocessor, but also all the other portions of the system. With the flexibility in configuration for the MC34701, MC34702 and MC34703 devices, the designer can easily make the proper arrangements to utilize these devices to achieve the power supply needs of the system.

Finally, the following table summarizes the selection of the Freescale Power management ICs for each of the high end microprocessors shown in this document:

<table>
<thead>
<tr>
<th>High-end Microprocessor</th>
<th>Freescale Power Management IC solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMCC® – NPE405</td>
<td>MC34701 or MC34702</td>
</tr>
<tr>
<td>AMD® – SC520</td>
<td>MC34701 or MC34702</td>
</tr>
<tr>
<td>PMC Sierra® - RM7000</td>
<td>MC34701 or MC34702</td>
</tr>
<tr>
<td>AMCC® - PPC440Gx</td>
<td>MC34702</td>
</tr>
<tr>
<td>Intel® – IXP45X</td>
<td>MC34702</td>
</tr>
<tr>
<td>Intel® – IXP2400</td>
<td>MC34703 + Additional LDOs</td>
</tr>
<tr>
<td>NEC® – VR5500</td>
<td>MC34701 or MC34702</td>
</tr>
</tbody>
</table>

Table 3: Summary of Freescale power management IC assignment for high-end microprocessors
8 References

- MC34701, MC334702, MC34703 and MC34710 data sheets
- AN1989 “MC34701 and MC34702 Component Selection Guidelines”
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