**Freescale Semiconductor**
Application Note

Document Number: AN3287
Rev. 1, 08/2006

# MFR4300 External Reset

by: David Paterson
MCD Applications, East Kilbride, Scotland

## 1 Introduction

Freescale Semiconductor offers a key standalone FlexRay communication controller — MFR4300. This application note describes a known external reset problem with the MFR4300 and details an external hardware workaround.

The mask ID for the MFR4300 device is 0M92D. This can be read in the MVR as 0x3535. Please refer to the *MFR4300 Data Sheet* for further information.

## 2 Objective

The aim of this document is to detail the MFR4300 external reset problem and describe potential hardware and software workarounds. These are examples only and other methods can be considered to synchronize external reset deassertion to the internal clock of the MFR4300.

**Contents**





freescale™ semiconductor

# 3 MFR4300 External Reset Problem Overview

A problem has been identified for the external reset of the MFR4300 ($\overline{\text{RESET}}$). The problem concerns an improper device startup during the external reset procedure.

This problem is caused by an asynchronous external reset signal deassertion which happens at the capturing time of that signal by the MFR4300. The MFR4300 device uses this signal without synchronizing it to its internal clock.

In normal cases, after external reset deassertion, the MFR4300 samples the IF_SEL inputs (TXD_BG[1:2]/IF_SEL[1:0] pins) and after ~70 EXTAL/CLK_CC periods the device starts to drive the TXD_BG function (please refer to the *MFR4300 Data Sheet*, Figure 6-6).

The reported problem happens when the MFR4300 samples the external reset signal at the time it is changing from "0" (asserted) to "1" (deasserted). The frequency of that failure may vary. For example, if the external reset is produced by a manual switch it can reach a ratio of one failure out of 600 cases.

There are two outcomes possible after the external reset deassertion:

- The MFR4300 switches to the TXD_BG output function after a long delay of ~16400 EXTAL/CLK_CC periods; however, samples the IF_SEL inputs **correctly**.
- The MFR4300 switches to the TXD_BG output function after a very short delay of ~8 EXTAL/CLK_CC periods and samples the IF_SEL inputs **incorrectly.**

This problem is caused by the MFR4300 clock and reset generator's (CRG) D-type flip flops (DFFs). An asynchronous signal, which is produced out of the external reset input, is fed to the DFFs which leads to its instability under certain timing conditions when the DFFs sample the changing value.

As a result, the CRG DFFs jump to unpredictable states and generate a too short or too long delay for the TXD_BG[1:2]/IF_SEL[1:0] pins that are switching from IF_SEL input mode to the TXD_BG output mode.

There are two possible workarounds (two external DFFs) which synchronize with:

- The external reset signal to the MFR4300's CLKOUT when a crystal is used
- The external clock CLK_CC if it is fed to the MFR4300

This application note describes the workaround involving synchronizing the external reset signal deassertion to the MFR4300's CLKOUT signal (4/10/40 MHz).

# 4 Potential External Workaround — Hardware

## 4.1 Test Hardware Setup

The test hardware involved uses Freescale's MPC5xx Family of microcontrollers connected with Freescale's standalone FlexRay communication controller, MFR4300. This hardware is available to buy from http://www.freescale.com and comprises the structure shown in Figure 1.

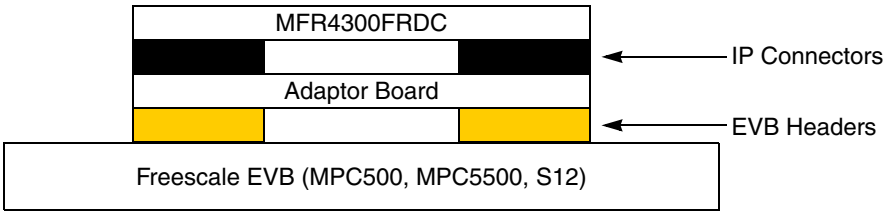


**Figure 1. Freescale Standalone FlexRay Hardware Solution**

The part numbers for the adaptor boards are: FLXRAYADPT500, FLXRAYADPT5500, and SCFLXRAYADPTS12.

A block diagram of the test system for this workaround is shown in Figure 2.

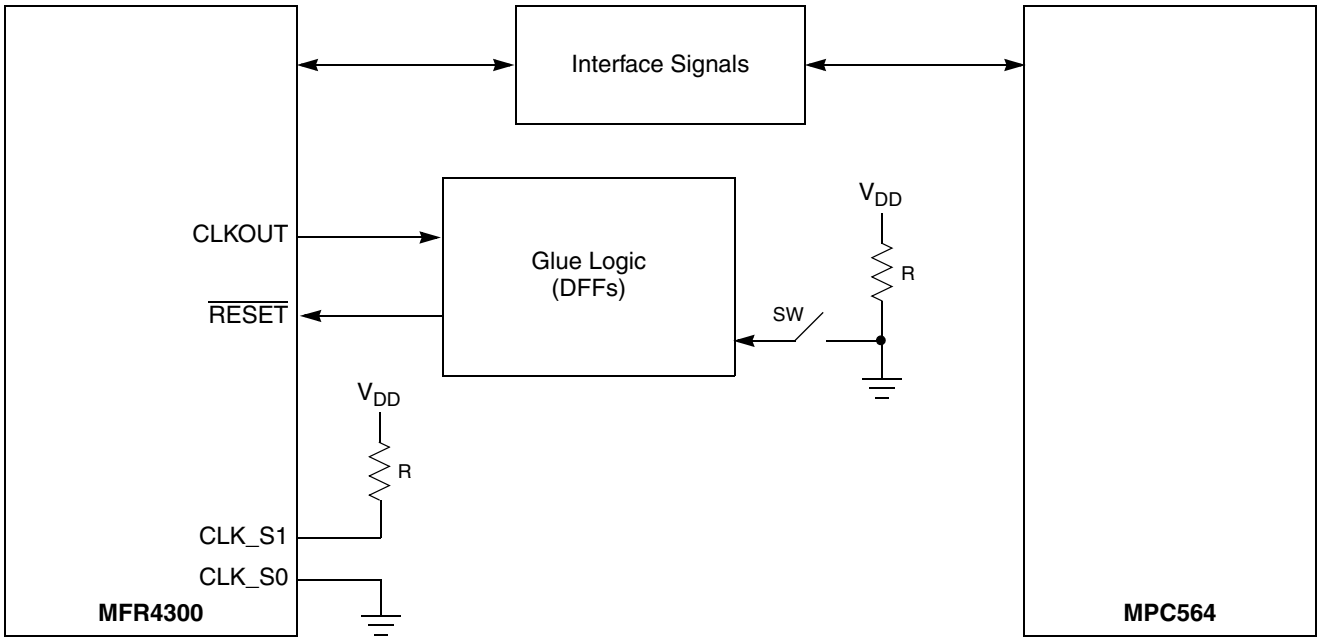


**Figure 2. Test System Block Diagram (with CLKOUT set at 40 MHz)**

## 4.2 Workaround Schematic

The workaround involves connecting Texas Instrument's dual positive-edge-triggered D-type flip-flops with clear and preset (SN74LVC74A) as the glue logic to synchronize the external reset deassertion with the MFR4300's CLKOUT signal (4/10/40 MHz).

The MFR4300 must be set up to output any frequency from CLKOUT — this can either be 4 MHz, 10 MHz, or 40 MHz. This involves setting CLK_S0 and CLK_S1 accordingly. Please see the *MFR4300 Data Sheet* for further information.

Figure 3 shows the test schematic used to verify the workaround. The source of the external reset was set as a push switch to GND. This will have to be changed to another source for working systems.

Please note that appropriate decoupling capacitors must be used in the circuitry.

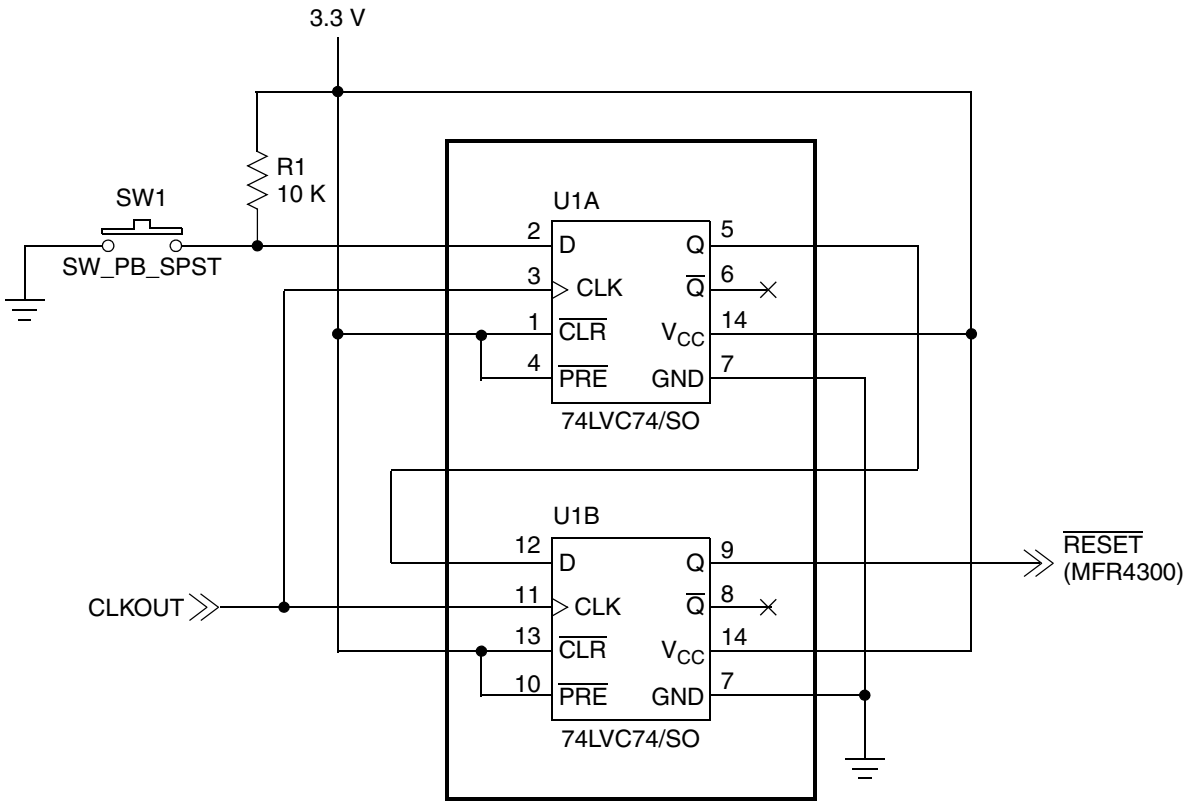


**Figure 3. Suggested Schematic**

## 4.3 Logic Analyzer Snapshots

The following logic analyzer snapshots show the behavior of IF_SEL1 and $\overline{\text{RESET}}$ in the following conditions:

Figure 4 — Normal operation

Figure 5 — Fail case 1 — MFR4300 switches to the TXD_BG output function after a long delay

Figure 6 — Fail case 2 — MFR4300 switches to the TXD_BG output function after very short delay

Figure 7 — DFF fixed operation

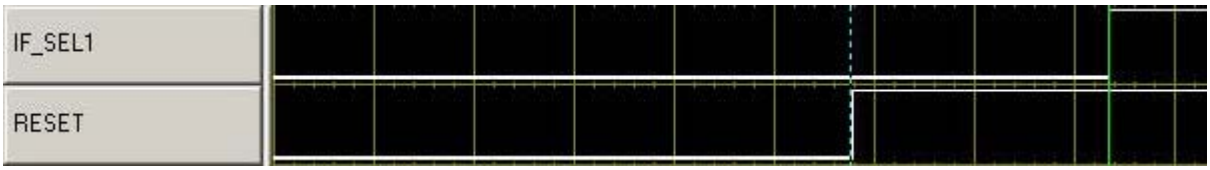


**Figure 4. Normal Operation**

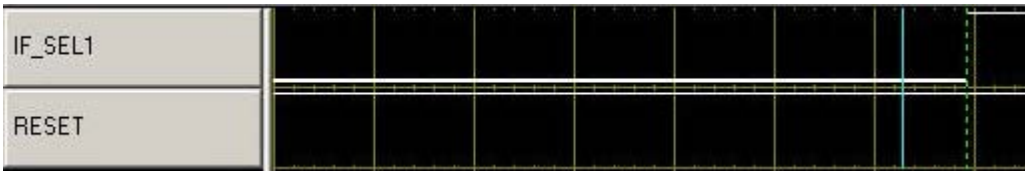


**Figure 5. Fail Case 1 — MFR4300 Switches to the TXD_BG Output Function after a Long Delay**

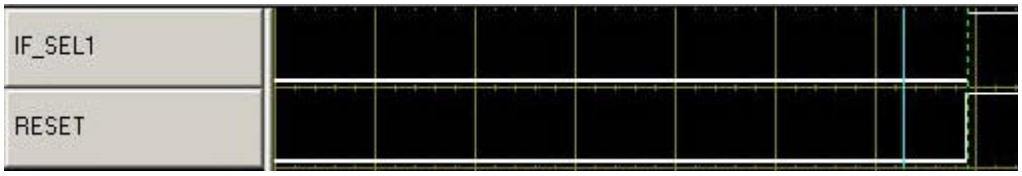


**Figure 6. Fail Case 2 — MFR4300 Switches to the TXD_BG Output Function after Very Short Delay**

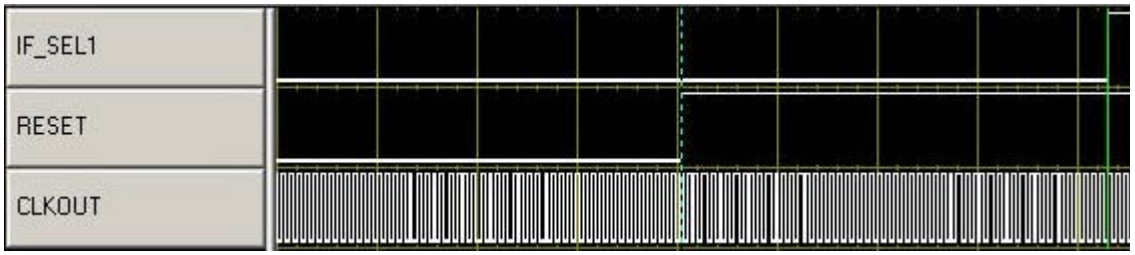


**Figure 7. DFF Fixed Operation**

# 5 Potential External Workaround — Software

For the software workaround, it is mandatory that the software be able to trigger the MFR4300 reset. In this case the software has to check the reset values of the MVR after reset is released (other registers such MBSSUTR, PIDR, and CRSR could also be checked). If this is correct, the MFR4300 is reset correctly. If other values are read, the MFR4300 is not correctly reset and requires another reset attempt. This must be repeated until the registers are read correctly.

If the MFR4300 can not be reset by a software command, this workaround will not work. In this case, an external hardware workaround must be adopted.

The following code snapshot shows a simple software example on how the Module Version Register (MVR) can be used to determine whether the external reset was successful or not.

```
var0 = MVR;
if (var0 == 0x3535)
{Initialize_FlexRay;}      //External reset was successful
else
{Reset_MFR4300;}           //External reset was not successful. Reset the device again.
```

# 6 Conclusions

The external reset problem found on the MFR4300 can be successfully overcome by adding some simple external hardware using DFFs, or by adopting a simple software workaround (if the external reset can be controlled by the host). This allows the external reset signal to be synchronized with the MFR4300's internal clock. Examples were detailed in this application note though other methods can be considered that would perform the same function. The recommended dual DFF from Texas Instruments is available in an ultra small 14-pin TSSOP package.

# 7 References

1. *MFR4300 FlexRay Communication Controller Data Sheet* (MFR4300)
2. Texas Instrument's *Dual Positive-Edge-Triggered D-Type Flip-Flops with Clear and Preset Data Sheet* (SN74LVC74A).

These documents are available on the Freescale Semiconductor web site at http://www.freescale.com and http://www.flexray.com.

More information on Freescale's FlexRay products can be found at http://www.freescale.com/flexray

THIS PAGE IS INTENTIONALLY BLANK

## *How to Reach Us:*

**Home Page:**
www.freescale.com

**E-mail:**
support@freescale.com

**USA/Europe or Locations Not Listed:**
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

**Europe, Middle East, and Africa:**
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

**Japan:**
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

**Asia/Pacific:**
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

***For Literature Requests Only:***
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: AN3287
Rev. 1
08/2006



freescale™
semiconductor