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Application Note

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Using the UTOPIA Interface on the MSC8144 DSP

by *Miguel Liber*

The MSC8144 DSP device includes an ATM controller that supports a UTOPIA level 2 (L2) interface through its QUICC Engine™ technology block. The ATM interface uses the unified communication controller 5 (UCC5) to define the protocols used and maintain data FIFOs and an associated UTOPIA controller (UPC). This document provides basic guidelines for using this interface, including the setup of MSC8144 as a target (slave) device. The document also includes guidelines for configuring an MPC8560 PowerQUICC™ III processor as an initiator (master) device because the MSC8144 can only be configured as a UTOPIA slave device and requires a master device to transfer data across the interface. The examples used in this application note refer to a system using the MPC8560 processor as the master device and the MSC8144 DSP as the slave device.

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1 Introduction

Asynchronous transfer mode (ATM) is defined by a set of internationally recognized protocols. It was designed originally as a compromise to meet the requirements of several networking interconnection systems in Europe and North America. The primary focus of the protocols is to define a fixed length cell-based data transmission system. In addition to data cells, the system uses a special set of operation administration and maintenance (OAM) cells for supervision, testing, and performance monitoring. The OAM cells conform to the cell guidelines set forth by the protocols, but these cells have special structures and meanings and are not used to transfer data payloads. A detailed discussion of cell management, maintenance, and data transmission is beyond the scope of this document.

The universal test and operations physical interface for ATM (UTOPIA) is a set of hardware protocols that support the ATM transmission model with a defined set of address, data, and control lines. The various UTOPIA protocols support different levels of data transmission with different data bus widths and features. This application note focuses on the UTOPIA level 2 interface that is supported by the MSC8144 and describes how to configure and initialize that interface. UTOPIA level 2 interfaces support both level 1 and level 2 operations. UTOPIA level 1 interfaces support 8-bit data transfers with no addressing. UTOPIA level 2 interfaces support both 8-bit and 16-bit data transfers with addressing and single or multi-PHY systems. A PHY is a physical interface that supports interconnecting ports. A single PHY has a single port while a multi-PHY device supports multiple ports.

Basically, the MSC8144 devices support two data bus widths: 8-bit and 16-bit. Except for the data bus width, the interfaces operate the same way. Although UTOPIA protocols define both master (initiator) and slave (target) modes, the MSC8144 can only be configured as a slave device.

2 UTOPIA Interfaces

The following subsections describe how to use the UTOPIA level 2 slave interface on the MSC8144 and the master interface on the MPC8360 processor.

2.1 Using the MSC8144 UTOPIA L2 Interface

The UPC is the UTOPIA media access control (MAC) peripheral in the QUICC Engine subsystem. It supports UTOPIA level 2 for target (slave) mode.The UPC is operated through UCC5. Because it is a MAC, the UPC is not independent from the UCC, which contains the data FIFOs (queues). As a target, the UPC can operate in single PHY or in multi-PHY mode. The device routing is configured through the UCC independently for receive (Rx) and transmit (Tx) interfaces. The UPC receiver block is responsible for the receive data flow. In Slave mode, the receiver checks for FIFO full indication to present the cell available (CLAV) signals. Once it detects a selection condition, the cell/packet is received.

As transmitter, the UPC supports an internal rate mechanism. This mechanism enables allocation of a precise bandwidth to each port in a multi-PHY or single PHY distribution. The transmission rate is determined by the UPC internal rate timers. The source clock of the internal rate timers can use the serial clock, a clock derived from a baud rate generator, or an external clock source. The internal rate works differently for single PHY and for multi-PHY devices. In single PHY mode, the internal rate paces the line rate and the transmit FIFO becomes a leaky bucket. In multi-PHY mode, the internal rate paces the FIFO fill rate (the polling status is qualified by the internal rate, and the FIFO only contains cells for PHYs that

are actively requesting data).In the receive direction, the UPC uses a selection based on programmable priority to prioritize cell transfers from the ports to the UCC. See the *MCS8144 Reference Manual* for details.

There are two bus configurations used by the MSC8144 for connecting the UTOPIA interface, depending on the data bus width. The UTOPIA device configuration requires a total of 36 I/O ports for 8-bit mode and 52 ports in 16-bit mode. Figure 1 shows the MSC8144 UTOPIA signals. Table 1 describes the signals.

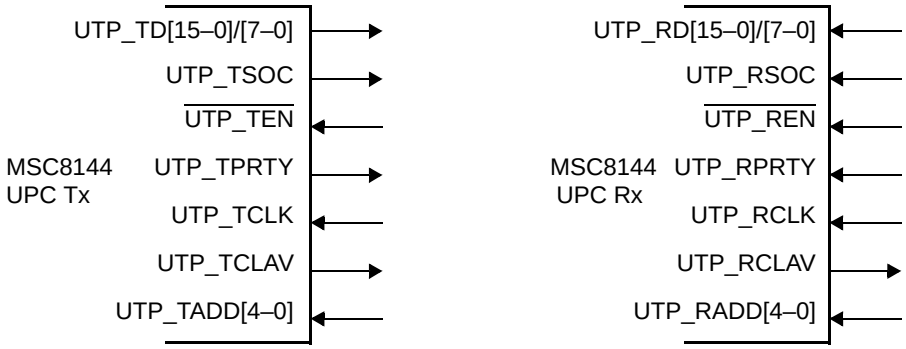

Figure 1. MSC8144 UTOPIA Signals

Table 1. MSC8144 UTOPIA Slave Mode Signal Properties

Name	Function	I/O	I/O Mode
UTP_TD[15–0]/[7–0]	Transmit data from PHY to link layer	O	0,4,5/0,1,3,4,5,6
UTP_TSOC	Transmit start of cell	O	0,1,3,4,5,6
$\overline{\text{UTP\_TEN0}}$	Transmit enable	I	0,1,3,4,5,6
UTP_TCLAV0	Transmit cell available	O	0,1,3,4,5,6
UTP_TPRTY	Transmit parity	O	0,1,3,4,5,6
UTP_TCLK	Transmit clock	I	0,1,3,4,5,6
UTP_TADD[4–0]	Transmit address	I	0,1,3,4,5,6
UTP_RD[15–0]/[7–0]	Receive data from link layer to PHY	I	0,4,5/0,1,3,4,5,6
UTP_RSOC	Receive start of cell	I	0,1,3,4,5,6
$\overline{\text{UTP\_REN0}}$	Receive enable	I	0,1,3,4,5,6
UTP_RCLAV0	Receive cell available	O	0,1,3,4,5,6
UTP_RPRTY	Receive parity	I	0,1,3,4,5,6
UTP_RCLK	Receive clock at 50MHz	I	0,1,3,4,5,6
UTP_RADD[4–0]	Receive address	I	0,1,3,4,5,6

NOTE

Users familiar with the UTOPIA interface of the CPM in the MSC8101, MPC82xx, and MPC85xx should note that the external signal naming convention used in the MSC8144 follows the UTOPIA standard. The naming convention used for the CPM retains the Master mode signal naming for the Slave mode. For example, the CPMs transmit the SOC signal in Slave mode as TSOC. The MSC8144 transmit SOC in Slave mode as RSOC. When connecting between UPCs based on QUICC Engine technology, always connect signals between Master and Slave by name.

2.2 Using the MPC8560 UTOPIA L2 interface

The MPC8560 supports UTOPIA level 2 for both Master and Slave modes. In Master mode, the receiver data bus is identified as RXD[0–7] or RXD[0–15] and transfers data from the PHY to the FCC. The PHY is the physical device used to interface the MPC8560 with the external system. The PHY converts the digital signals of the UTOPIA to those required externally and handles all the line signaling. The Transmitter data bus is identified as TXD[0–7] or TXD[0–15] and transfers data from the FCC to the PHY. When the PHY has a cell ready to transfer to the FCC, it indicates it by asserting the RX cell available signal. The FCC indicates to the PHY that it will sample the receive data and receiver start of cell signals on the next cycle by asserting RX enable. RXSOC indicates that the receiver data lines contain the first valid byte of the cell. It is a tri-state signal used for multi-PHY operation. The PHY asserts the transmit cell available signal (TXCLAV) to indicate that it has room for a cell to transmit. The FCC indicates to the PHY that valid data is on the transmit data bus with the transmit enable signal ($\overline{\text{TXENB}}$), and indicates that the first byte of the cell is on the bus with the transmit start of cell signal (TXSOC). The remaining signals are the receiver and transmitter address signals that provide five pins each for selecting the required PHY in a multi-PHY environment, and the receiver and transmitter parity indicating odd parity for each data bus. UTOPIA L2 allows for the connection of multiple PHYs and address polling. It is possible to connect up to 31 PHYs to the FCC. The 32nd address option is a null address function used for part of the transfer. All signals are sampled on positive edges of the clock. An address (Tx or Rx) is placed on the address lines on one clock, and the addressed PHY asserts the appropriate cell available signal if it has room for a cell or has a cell to transfer. The cell available signals are sampled on the next clock, at which time the null address (0x1F) is asserted on the address lines. In this way, the controller polls all active PHYs, starting at address zero. Data can be transferred on the data lines during polling. The UTOPIA clock can be generated internally or externally. If the UTOPIA clock is generated internally, the user should assign one of the baud-rate generators to supply the UTOPIA clock. See the *MPC8560 Reference Manual* for more information. Figure 2 shows the MPC8560 UTOPIA master signals. Table 2 is a list of signal descriptions.

Figure 2. MPC8560 UTOPIA Master Mode Signals

Table 2. MCP8560 UTOPIA Master Mode Signal Descriptions

Signal	Description
TxDATA[0–15]/[0–7]	Carries transmit data from the ATM controller to a PHY device. TxDATA15/7 is the msb when using UTOPIA 16/8, TxDATA0 is the lsb.
TxSOC	Transmit start of cell. Asserted by the ATM controller when the first byte of a cell is sent on TxDATA lines.
$\overline{\text{TxENB}}$	Transmit enable. Asserted by the ATM controller when valid data is placed on the TxDATA lines.
TxCLAV	Transmit cell available. Asserted by the PHY device to indicate that the PHY has room for a complete cell.
TxPRTY	Transmit parity. Asserted by the ATM controller. It is an odd parity bit over the TxDATA bits.
TxCLK	Transmit clock. Provides the synchronization reference for the TxDATA, TxSOC, $\overline{\text{TxENB}}$, TxCLAV, TxPRTY signals. All the above signals are sampled at low-to-high transitions of TxCLK.
TxADD[0–4]	Transmit address. Address bus from the ATM controller to the PHY device used to select the appropriate multi-PHY device. Each multi-PHY device needs to maintain its address. TxADD4 is the msb.
RxDATA[0–15]/[0–7]	Carries receive data from the PHY to the ATM controller. RxDATA15/7 is the msb when using UTOPIA 16/8, RxDATA0 is the lsb.
RxSOC	Receive start of cell. Asserted by the PHY device as the first byte of a cell is received on RxDATA.
$\overline{\text{RxENB}}$	Receive enable. An ATM controller asserts to indicate that RxDATA and RxSOC will be sampled at the end of the next RxCLK cycle. For multiple PHYs, $\overline{\text{RxENB}}$ is used to three-state RxDATA and RxSOC: at each PHYs output. RxDATA and RxSOC should be enabled only in cycles after those with $\overline{\text{RxENB}}$ asserted.
RxCLAV	Receive cell available. Asserted by a PHY device when it has a complete cell to give the ATM controller.
RxPRTY	Receive parity. Asserted by the PHY device. It is an odd parity bit over the RxDATA. If there is a RxPRTY error and the receive parity check FPSMR[RxP] is enabled, the cell is discarded. See FCC Protocol-Specific Mode Register (FPSMR).
RxCLK	Receiver clock. Synchronization reference for RxDATA, RxSOC, $\overline{\text{RxENB}}$, RxCLAV, and RxPRTY, all of which are sampled at low-to-high transitions of RxCLK.
RxADD[0–4]	Receive address. Address bus from the ATM controller to the PHY device used to select the appropriate multi-PHY device. Each multi-PHY device needs to maintain its address. RxADD4 is the msb.

3 UTOPIA L2 Configuration in the MSC8144 and MPC8560

This section describes configurations for bringing up a basic MPC8560 and MSC8144 based UTOPIA L2 system that supports single PHY or multi-PHY operations using an 8-bit data bus. Operation using a 16-bit data bus is identical, but you must configure the transmit and receive bus width for 16-bit operation (see the *MSC8144 Reference Manual* and the *MPC8560 Reference Manual* for details).

3.1 Basic Single PHY with an 8-Bit Data Bus

The example shows how to configure the MSC8144 and the MPC8560 UTOPIA L2 interface for basic single PHY 8-bit mode, with the MPC8560 TX/RX as master and the MSC8144 TX/RX as slave.

3.1.1 MSC8144 UTOPIA Configuration

Table 3 shows the register settings used to configure the MSC8144 as a UTOPIA slave using an 8-bit L2 data bus.

Table 3. MSC8144 Register Settings for UTOPIA 8-Bit Level 2 Single-PHY Operation

Register	Configured Value
UPC General Configuration Register (UPGCR)	0x6000_0000
UPC Last PHY Address (UPLPA)	0x0
UPC HEC Register (UPHEC)	0x0
UPC UCC Configuration (UPUC)	0x0
UPC Device 1 Configuration (UPDC1)	0x000A_C000
UPC Device 1 Internal Rate Configuration (UPRP1)	0x0

Example 1. Code to Configure the MSC8144 as a UTOPIA 8-Bit Slave Single PHY Device

```
# UPC Registers set
mm fee02e00 6000_0000; # UPGCR -> Tx slave, Rx slave
mm fee02e04 0000_0000; # UPLPA -> > Tx/Rx Last Phy = 0
mm fee02e08 0000_0000; # UPHEC -> Hec value = 0
mm fee02e0c 0000_0000; # UPUC -> Single PHY Mode
mm fee02e10 000a_C000; # UPDC1 -> UPC1(UCC5), En Tx, En Rx
mm fee02e70 00000000; #


# Other relevant registers
mm 0xfff7801c 0x00000080; # QECR: TxS, RxS, utp_en
mm fee00420 0xyy000000;# CMXUPCR ucc is connected to yy
```

The following subsections describe the two registers that are not used with the default settings. The field descriptions indicated the selected functionality in this configuration.

3.1.1.1 UPC General Configuration Register (UPGCR)

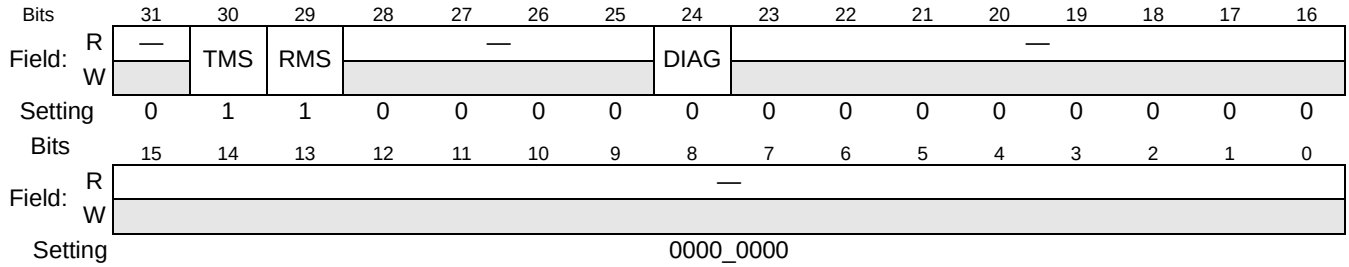

Figure 3. UPC General Configuration Register (UPGCR)

Table 4 describes UPGCR fields

Table 4. UPGCR Register Field Descriptions

Bits	Name	Description	Setting
31	—	Reserved. Must be cleared.	
30	TMS	**Transmit Master/Slave Mode**	1 Transmit slave mode is selected.
29	RMS	**Receive Master/Slave Mode**	1 Receive slave mode is selected.
28–25	—	Reserved. Must be cleared.	
24	DIAG	**Diagnostic Mode**	0 Normal mode.
23–0	—	Reserved. Must be cleared.	

3.1.1.2 UPC Device 1 Configuration Register (UPDC1)

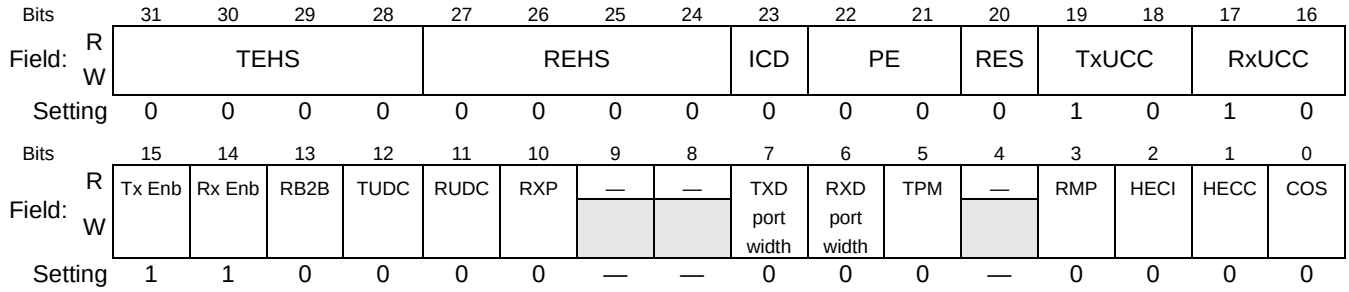

Figure 3-4. UPC Device 1 Configuration Register in ATM Protocol (UPDC1)

Table 5 describes UPDC1 fields.

Table 5. UPDC1 in ATM Protocol Field Descriptions

Bits	Name	Description	Settings
31–28	TEHS	**Transmit Extra Header Size** Used only in user-defined cell mode to hold the Tx user-defined cells extra header size. Values between 0–11 are valid.	0 generates 1 byte of extra header ... 11 generates 12 bytes of extra header.
27–24	REHS	**Receive Extra Header Size** Used only in user-defined cell mode to hold the Rx user-defined cells extra header size.	0 expects 1 byte of extra header ... 11 expects 12 bytes of extra header.
23	ICD	**Idle Cells Discard**	0 Discard idle cells (GFC/VPI/VCI/PTI =0).
22–21	PE	**Port Enable**	00 Master: UPER has no affect: All ports are enabled. Slave: UPER has no affect, port0 is enabled regardless of Phy address.
20	—	Reserved. Must be cleared	
19–18	TxUCC	**Transmit UCC**	10 UCC5 (UPC1
17–16	RxUCC	**Receive UCC**	10 UCC5 (UPC1)
15	Tx Enb	**Transmit Enable**	1 Tx Enabled
14	Rx Enb	**Receive Enable**	1 Rx Enabled
13	RB2B	**Receive Back to Back**.	0 Do not attempt Receive B2B from this device.
12	TUDC	**Transmit User-Defined Cells**	0 Regular 53-byte cells.
11	RUDC	**Receive User-Defined Cells**	0 Regular 53-byte cells.
10	RXP	**Receive Parity Check**	0 Check Rx parity line.
9–8	RES	Must be cleared	
7	TXD port width	**Transmit Data Bus Width Device/SPHY**	0 8-bit data bus width
6	RXD port width	**Receive Data Bus Width Device/SPHY**	08-bit data bus width
5	TPM	**Tx Selection Priority Mode** This controls the priority by which PHYs are serviced.	0 Round Robin. After a PHY has been selected, the selection resumes from the next PHY.
4	RES	Must be cleared	
3	RMP	**Receive Multiple PHY Mode**	0 Receive from SPHY device (CLAV/PTA is always assumed valid, PHY address must be 0)
2	HECI	**HEC Included** Used in UDC mode only.	0 HEC octet is not included when UDC mode is enabled.
1	HECC	**HEC Check**	0 Do not check Rx HEC
0	COS	**Coset Mode on the HEC**	0 Do not use Coset Mode on the HEC

3.1.2 MPC8560 UTOPIA Configuration

Table 6 shows the register settings used to configure the MPC8560 as a UTOPIA master using an 8-bit L2 data bus.

Table 6. MPC8560 Register Settings for UTOPIA 8-Bit Level 2 Operation

NAME	VALUE
FPSMR1	0000_0000

Example 2. Code to Configure the MPC8560 as a UTOPIA 8-Bit Master Single PHY Device

```
rm fcc1.fpsmr1 0000_0000; # FPSMR1:utopia rx /tx in Master mode

# Others relevant registers:

# Programing PIO register (TX/RX Master,sphy,16bitdata)
rm io_port.podra 0
rm io_port.pdira 0x0000_3fcd; # Slave 0x00003fe5
rm io_port.ppara 0x003f_ffff
rm io_port.psora 0

rm io_port.podrc 0
rm io_port.pdirc 0x00e00000;#0x00e00400 - clk12 txin, brg6:brgo rxout.
#0x00e00000 - external clk clk12 txin, clk11 rxin.
rm io_port.pparc 0x00e00c00;#
rm io_port.psorc 0

rm io_port.podrd 0
rm io_port.pdird 0x0600_8248
rm io_port.ppard 0x0603_cff8
rm io_port.psord 0

rm cpm_mux.cmxfcr 0xYY000000;#Rx and Tx FCC1 serial clocks from YY
```

The following subsections describe the two significant registers used to define this configuration. The field descriptions indicated the selected functionality in this configuration.

3.1.2.1 FCC Protocol-Specific Mode Register (FPSMR)

Bits	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	TEHS				REHS				ICD	TUMS	RUMS	LAST PHY/PHY ID				
Setting	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Field:			TPRI	TUDC	RUDC	RXP	TUMP		TSIZE	RSIZE	UPRM	UPLM	RUMP	HECI		
Setting	—	—	0	0	0	0	0		0	0	0	0	0	0	—	—

Figure 5. FCC Protocol-Specific Mode Register (FPSMR)

Table 7. FPSMR Register Field Descriptions

Bits	Name	Description	Settings
0-3	TEHS	**Transmit Extra Header Size** Used only in user-defined cell mode to hold the Tx user-defined cells extra header size. Values between 011 are valid. **Note:** When working with a 16-bit UTOPIA interface, TEHS must represent an even number of header bytes (so the actual programmed value should be odd)	0 generates 1 byte of extra header ... 11 generates 12 bytes of extra header.
4-7	REHS	**Receive Extra Header Size** Used only in user-defined cell mode to hold the Rx user-defined cells extra header size. Values between 011 are valid. **Note:** When working with a 16-bit UTOPIA interface, REHS must represent an even number of header bytes (so the actual programmed value should be odd).	0 expects 1 byte of extra header ... 11 expects 12 bytes of extra header.
8	ICD	**Idle Cells Discard**	0 Discard idle cells (GFC/VPI/VCI/PTI = 0).
9	TUMS	**Transmit UTOPIA Master/Slave Mode**	0 Transmit UTOPIA master mode is selected.
10	RUMS	**Receive UTOPIA Master/Slave Mode**	0 Receive UTOPIA master mode is selected.
11-15	LAST PHY/ PHY ID	**Last PHY** (Multiple PHY master mode only.) The UTOPIA interface polls all PHYs starting from PHY address 0 and ending with the PHY address specified in LAST PHY. (The number of active PHYs are LAST PHY + 1). LAST PHY should be specified in both multiplex and direct-polling modes. **PHY ID** (Multiple PHY slave mode only.) Determines the PHY address of the ATM controller when configured as a slave in a multiple PHY ATM port.	
16-17	—	Reserved, should be cleared.	

Table 7. FPSMR Register Field Descriptions (continued)

Bits	Name	Description	Settings
18	TPRI	**Transmitter Priority** Used to adjust the default priority of the FCC transmitter. It is strongly recommended to set TPRI when in multi-PHY mode; for other modes, it should remain cleared.	0 High priority (default operation)
19	TUDC	**Transmit User-Defined Cells**	0 Regular 53-byte cells.
20	RUDC	**Receive User-Defined Cells**	0 Regular 53-byte cells.
21	RxP	**Receive Parity Check**	0 Check Rx parity line.
22	TUMP	**Transmit UTOPIA Multiple Phy Mode**	0 Transmit UTOPIA single PHY mode is selected.
23	—	Reserved, should be cleared.	
24	TSIZE	**Transmit UTOPIA Data Bus Size**	0 UTOPIA 8-bit data bus size.
25	RSIZE	**Receive UTOPIA Data Bus Size**	0 UTOPIA 8-bit data bus size.
26	UPRM	**UTOPIA Priority Mode**	0 Round robin. Polling is done from PHY zero to the PHY specified in LAST PHY. When a PHY is selected, the UTOPIA interface continues to poll the next PHY in order.
27	UPLM	**UTOPIA Polling Mode** Polling is done using RxAdd[04] and Clav[0]. Selection is done using RxAdd[04]. Up to 31 PHYs can be polled.	0 Multiplex polling
28	RUMP	**Receive UTOPIA Multiple PHY Mode.**	0 Receive UTOPIA single PHY mode is selected.
29	HECI	**HEC Included** Used in UDC mode only.	0 HEC octet is not included when UDC mode is enabled.
30-31	—	Reserved, should be cleared.	

3.1.2.2 Other Registers

Refer to the *MPC8560 Reference Manual* for details on configuring the other registers listed in Section 3.1.2, “MPC8560 UTOPIA Configuration” on page 9.

3.2 Basic Multi-PHY with an 8-Bit Data Bus

The example shows how to configure the MSC8144 and the MPC8560 UTOPIA L2 interface for basic multi-PHY 8-bit mode, with the MPC8560 TX/RX as master and the MSC8144 TX/RX as slave.

3.2.1 MSC8144 Configuration

Table 8 shows the register settings used to configure the MSC8144 as a UTOPIA slave using an 8-bit L2 data bus.

Table 8. MSC8144 Register Settings for UTOPIA 8-Bit Level 2 Multi-PHY Operation

NAME	VALUE
UPC General Configuration Register (UPGCR)	0x6000_0000
UPC Last PHY Address (UPLPA)	0x0404_0000
UPC HEC Register (UPHEC)	0x_0
UPC UCC Configuration (UPUC)	0x0000_8000
UPC Device 1 Configuration (UPDC1)	0x000a_c008
UPC Device 1 Internal Rate Configuration (UPRP1)	0x0

Example 3. Code to Configure the MSC8144 as a UTOPIA 8-Bit Slave Multi-PHY Device

```
# UPC Registers set
mm fee02e00 6000_0000;# UPGCR -> Tx slave, Rx slave
mm fee02e04 0404_0000;# UPLPA -> > Tx/Rx Last Phy=4
mm fee02e08 0000_0000;# UPHEC -> Hec value =0
mm fee02e0c 0000_8000;# UPUC -> Tx Mphy
mm fee02e10 000a_C008;# UPDC1 -> UPC1(UCC5),En Tx, En Rx, Rx Mphy
mm fee02e70 00000000;#

# Others relevant registers
mm 0xfff7801c 0x00000080; # QECR: TxS, RxS, utp_en
mm fee00420 0xyy00000;# CMXUPCR ucc is connected to yy
```

3.2.1.1 UPC General Configuration Register (UPGCR)

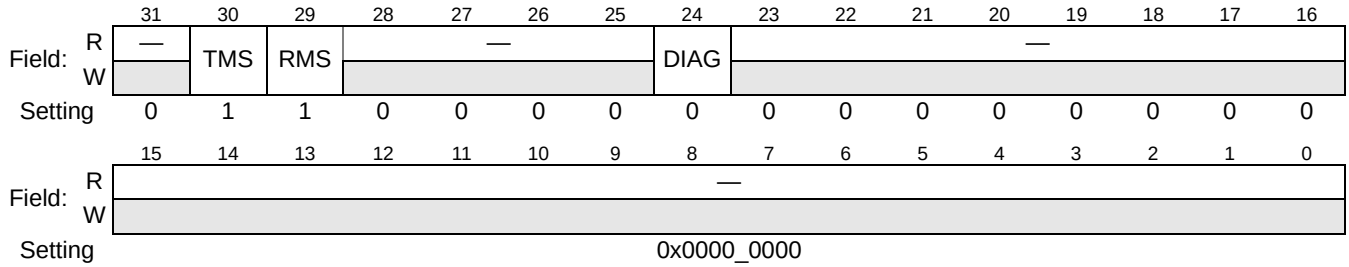

Figure 6. UPC General Configuration Register (UPGCR)

Table 9 describes UPGCR fields

Table 9. UPGCR Register Field Descriptions

Bits	Name	Description	Setting
31	—	Reserved. Must be cleared.	
30	TMS	**Transmit Master/Slave Mode**	1 Transmit slave mode is selected.
29	RMS	**Receive Master/Slave Mode**	1 Receive slave mode is selected.
28–25	—	Reserved. Must be cleared.	
24	DIAG	**Diagnostic Mode**	0 Normal mode.
23–0	—	Reserved. Must be cleared.	

3.2.1.2 UPC Last PHY Address Register (UPLPA)

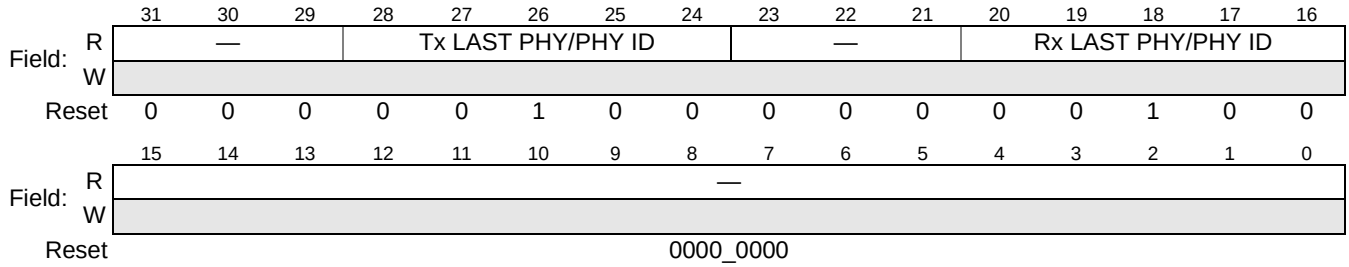

Figure 7. UPC Last PHY Address Register (UPLPA)

Table 10 describes UPLPA fields.

Table 10. UPLPA Register Field Descriptions

Bits	Name	Description	Setting
31–28	—	Reserved, should be cleared.	
3-7	Tx LAST PHY/PHY ID	**Master mode: Tx Last PHY** This is the last polled PHY addr (MPHY Master mode only) 5 lsb. The interface polls all PHYs starting from PHY address 0 and ending with the PHY address specified in LAST PHY. (The number of active PHYs are LAST PHY+1).	• Default MPHY mode: Maximal value = 31 • 6-bit addressing MPHY mode: Maximal value = 15 (Addr[4] is not valid). Common value for device pairs A,B. • Slave mode: Tx PHY address
8-10	—	Reserved, should be cleared.	
11-15	Rx LAST PHY/PHY ID	**Master mode: Rx Last PHY** This is the last polled PHY addr (MPHY Master mode only) 5 lsb. The interface polls all PHYs starting from PHY address 0 and ending with the PHY address specified in LAST PHY. (The number of active PHYs are LAST PHY+1).	• Default MPHY mode: Maximal value = 31 • 6-bit addressing MPHY mode: Maximal value = 15 (Addr[4] is not valid). Common value for device pairs A,B. • Slave mode: Rx PHY address
16-31	—	Reserved, should be cleared.	

3.2.1.3 UPC UCC Configuration Register (UPUC)

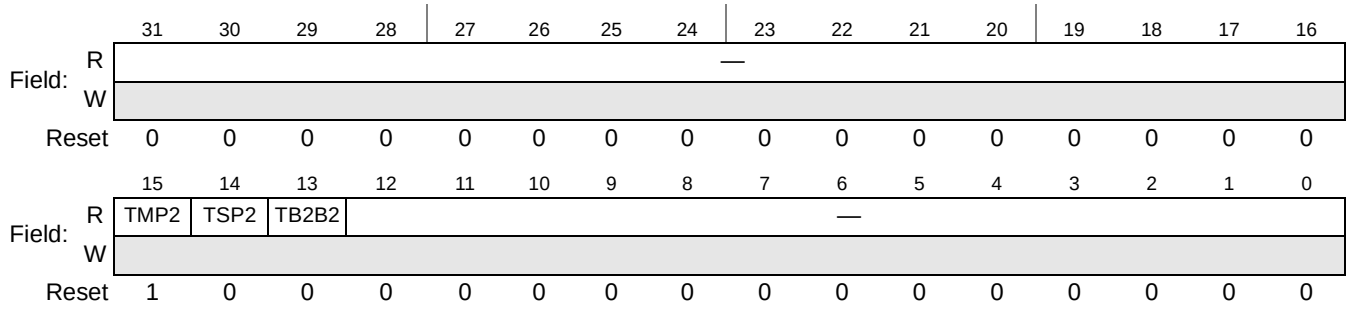

Figure 8. UPC UCC Configuration Register (UPUC)

Table 11 describes UPUC fields.

Table 11. UPUC Register Field Descriptions

Bits	Name	Description	Settings
31–16	—	Reserved, should be cleared.	
15	TMP_x	**Transmit Multiple PHY Mode** This mode should be set when a device with several PHYs are routed to this UCC.	UPC Tx Slave mode: 1 MPHY system (Output CLAV is a response for polling, Tri-state outputs)
14	TSP_x	**Transmit Single PHY Mode** This mode is valid only if TMP = 0:	0 Single EP: Internal address of this PHY must be 0. As slave, the internal rate enables the assertion of CLAV when the FIFO is not empty.
13	$TB2B_x$	**Transmit Back To Back** (valid only in master mode)	0 Do not attempt Transmit B2B from this UCC.
12–0	—	Reserved, should be cleared.	

3.2.1.4 UPC Device 1 Configuration Register (UPDC1)

Bits		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field:	R	TEHS				REHS				ICD	PE		RES	TxUCC		RxUCC	
	W																
Setting		0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field:	R	Tx Enb	Rx Enb	RB2B	TUDC	RUDC	RXP	—		TXD port width	RXD port width	TPM	—	RMP	HECI	HECC	COS
	W																
Setting		1	1	0	0	0	0	—	-	0	0	0	—	1	0	0	0

Figure 9. UPC Device 1 Configuration Register in ATM protocol (UPDC1)

Table 12 describes UPDC1 fields.

Table 12. UPDC1 in ATM Protocol Field Descriptions

Bits	Name	Description	Settings
31–28	TEHS	**Transmit Extra Header Size** Used only in user-defined cell mode to hold the Tx user-defined cells extra header size. Values between 0–11 are valid.	0 generates 1 byte of extra header ... 11 generates 12 bytes of extra header.
27–24	REHS	**Receive Extra Header Size** Used only in user-defined cell mode to hold the Rx user-defined cells extra header size.	0 expects 1 byte of extra header ... 11 expects 12 bytes of extra header.
23	ICD	**Idle Cells Discard**	0 Discard idle cells (GFC/VPI/VCI/PTI =0).
22–21	PE	**Port Enable**	00 Master: UPER has no affect: All ports are enabled. Slave: UPER has no affect, port0 is enabled regardless of PHY address.
20	—	Reserved. Must be cleared	
19–18	TxUCC	**Transmit UCC**	10 UCC5 (UPC1)
17–16	RxUCC	**Receive UCC**	10 UCC5 (UPC1)
15	Tx Enb	**Transmit Enable**	1 Tx Enabled
14	Rx Enb	**Receive Enable**	1 Rx Enabled
13	RB2B	**Receive Back to Back**.	0 Do not attempt Receive B2B from this device.
12	TUDC	**Transmit User-Defined Cells**	0 Regular 53-byte cells.
11	RUDC	**Receive User-Defined Cells**	0 Regular 53-byte cells.
10	RXP	**Receive Parity Check**	0 Check Rx parity line.
9–8	RES	Must be cleared	
7	TXD port width	**Transmit Data Bus Width Device/SPHY**	0 8-bit data bus width
6	RXD port width	**Receive Data Bus Width Device/SPHY**	0 8-bit data bus width
5	TPM	**Tx Selection Priority Mode** This controls the priority by which PHYs are serviced.	0 Round Robin. After a PHY has been selected, the selection resumes from the next PHY.
4	RES	Must be cleared	
3	RMP	**Receive Multiple PHY Mode**	1 Receive from MPHY device/s UPC Rx Slave mode: 1 MPHY system

Table 12. UPDC1 in ATM Protocol Field Descriptions (continued)

Bits	Name	Description	Settings
2	HECI	**HEC Included** Used in UDC mode only.	0 HEC octet is not included when UDC mode is enabled.
1	HECC	**HEC Check**	0 Do not check Rx HEC
0	COS	**Coset Mode on the HEC**	0 Do not use Coset Mode on the HEC

3.2.2 MPC8560 Configuration

Table 13. MPC8560 Register Settings for UTOPIA 8-Bit Level 2 Multi-PHY Operation

NAME	VALUE
FPSMR	0x0004_0208

Example 4. Code to Configure the MPC8560 as a UTOPIA 8-Bit Master Multi-PHY Device

```
rm fcc1.fpsmr1 0004_0208; # FPSMR1:utopia rx /tx in master mode

# Others relevant registers:

# Programing PIO register (TX/RXmaster,MPHY(ADD),16bitdata)
rm io_port.podra 0
rm io_port.pdira 0x0000_3fcd;# Slave 0x00003fe5
rm io_port.ppara 0x003f_ffff
rm io_port.psora 0

rm io_port.podrc 0
rm io_port.pdirc 0x03ef0000 ; #0x00e00400 -clk12 txin, brg6:brgo rxout.
#0x00e00000 - external clk clk12 txin, clk11 rxin.
rm io_port.pparc 0x03ef0c00;#
rm io_port.psorc 0x030f0000

rm io_port.podrd 0
rm io_port.pdird 0x0700_b24c
rm io_port.ppard 0x0703_cffc ; #0x0703fffc with add[4], 0x0703cffc without add[4]
rm io_port.psord 0x0100_0004


rm cpm_mux.cmxfcr 0xyy000000;#Rx and Tx FCC1 serial clocks from yy
rm cpm_mux.cmxuar 0x0000f100;# Address [0-3]
```

3.2.2.1 FCC Protocol-Specific Mode Register (FPSMR)

Bits	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	TEHS				REHS				ICD	TUMS	RUMS	LAST PHY/PHY ID				
Setting	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Field:			TPRI	TUDC	RUDC	RXP	TUMP		TSIZE	RSIZE	UPRM	UPLM	RUMP	HECI		
Setting	—	—	0	0	0	0	1	—	0	0	0	0	1	0	—	—

Figure 10. FCC Protocol-Specific Register (FPSMR)

Table 14. FPSMR Register Field Descriptions

Bits	Name	Description	Settings
0–3	TEHS	**Transmit Extra Header Size** Used only in user-defined cell mode to hold the Tx user-defined cells extra header size. Values between 0–11 are valid. **Note:** When working with a 16-bit UTOPIA interface, TEHS must represent an even number of header bytes (so the actual programmed value should be odd)	0 generates 1 byte of extra header ... 11 generates 12 bytes of extra header.
4–7	REHS	**Receive Extra Header Size** Used only in user-defined cell mode to hold the Rx user-defined cells extra header size. Values between 0–11 are valid. **Note:** When working with a 16-bit UTOPIA interface, REHS must represent an even number of header bytes (so the actual programmed value should be odd).	0 expects 1 byte of extra header ... 11 expects 12 bytes of extra header.
8	ICD	**Idle Cells Discard**	0 Discard idle cells (GFC/VPI/VCI/PTI = 0).
9	TUMS	**Transmit UTOPIA Master/Slave Mode**	0 Transmit UTOPIA master mode is selected.
10	RUMS	**Receive UTOPIA Master/Slave Mode**	0 Receive UTOPIA master mode is selected.
11–15	LAST PHY/ PHY ID	**Last PHY.** (Multiple PHY master mode only.) The UTOPIA interface polls all PHYs starting from PHY address 0 and ending with the PHY address specified in LAST PHY. (The number of active PHYs are LAST PHY + 1). LAST PHY should be specified in both multiplex and direct-polling modes. **PHY ID**. (Multiple PHY slave mode only.) Determines the PHY address of the ATM controller when configured as a slave in a multiple PHY ATM port.	
16–17	—	Reserved, should be cleared.	

Table 14. FPSMR Register Field Descriptions (continued)

Bits	Name	Description	Settings
18	TPRI	**Transmitter Priority** Used to adjust the default priority of the FCC transmitter. It is strongly recommended to set TPRI when in multi-PHY mode; for other modes, it should remain cleared.	0 High priority (default operation)
19	TUDC	**Transmit user-defined cells**	0 Regular 53-byte cells
20	RUDC	**Receive User-Defined Cells**	0 Regular 53-byte cells
21	RxP	**Receive Parity Check**	0 Check Rx parity line.
22	TUMP	**Transmit UTOPIA Multiple PHY Mode**	1 Transmit UTOPIA multiple PHY mode is selected.
23	—	Reserved, should be cleared.	
24	TSIZE	**Transmit UTOPIA Data Bus Size**	0 UTOPIA 8-bit data bus size.
25	RSIZE	**Receive UTOPIA Data Bus Size**	0 UTOPIA 8-bit data bus size.
26	UPRM	**UTOPIA Priority Mode**	0 Round robin. Polling is done from PHY zero to the PHY specified in LAST PHY. When a PHY is selected, the UTOPIA interface continues to poll the next PHY in order.
27	UPLM	**UTOPIA Polling Mode**	0 Multiplex polling. Polling is done using RxAdd[04] and CLAV[0]. Selection is done using RxAdd[04]. Up to 31 PHYs can be polled.
28	RUMP	**Receive UTOPIA Multiple PHY Mode**	1 Receive UTOPIA multiple PHY mode is selected.
29	HECI	**HEC Included** Used in UDC mode only.	0 HEC octet is not included when UDC mode is enabled.
30-31	—	Reserved, should be cleared.	

3.2.2.2 Other Registers

See the *MPC8560 Reference Manual* for details on configuring the other registers listed in Section 3.2.2, “MPC8560 Configuration” on page 17.

4 References

1. *The ATM Forum, Utopia Level 2*, Version 1.0, June, 1995
2. *MPC8560 Reference Manual*.
3. *MCS8144 Reference Manual.*

Appendix A UPC Register Summary

Table 15. MPC8560 UPC Register Summary

Offset [1]	Register	Access	Reset Value	Size (bytes)
General configuration Registers				
0x0	UPGCR - General Config	R/W	0x0000_0000	1
0x4	UPLPA - Last PHY Addr	R/W	0x0000_0000	2
0x8	UPHEC - UL2 HEC config	R/W	0x0000_0000	2
0xC	UPUC - UCC Configuration	R/W	0x0000_0000	4
0x10	UPDC1 - Device1 Config	R/W	0x0000_0000	4
0x14–0x2F	Reserved			
Port Registers				
0x30	UPDRS1_H - Device1 Rate Select	R/W	0x0000_0000	4
0x34	UPDRS1_L - Device1 Rate Select	R/W	0x0000_0000	4
0x38–0x4F				
0x50	UPDRP1 - Device1 Receive Priority	R/W	0x0000_0000	4
0x54–0x5F				
Event Registers				
0x60	UPDE1 - Device1 Event	R/W	0x0000_0000	4
0x64–0x6F				
Internal Rate Registers				
0x70	UPRP1 - Device 1Internal Rate configuration	R/W	0x0007	2
0x72–0x7f				
0x80	UPTIRR1_0 - Device1 Transmit Internal Rate 0	R/W	0x0000_0000	2
0x82	UPTIRR1_1 - Device1 Transmit Internal Rate 1	R/W	0x0000_0000	2
0x84	UPTIRR1_2 - Device1 Transmit Internal Rate 2	R/W	0x0000_0000	2
0x86	UPTIRR1_3 - Device1 Transmit Internal Rate 3	R/W	0x0000_0000	2
0x88–0x9F				
0xA0	UPER1 - Device 1 Port Enable	R/W	0x0000_0000	4
0xA4–0xFF				

1 0x2E00 for UPC1

Table 16. MSC8144 UPC Register Memory Map

Address	Register Name	Acronym
0xFEE02E00	UPC General Configuration Register	UPGCR
0xFEE02E02–0xFEE02E03	reserved	

Table 16. MSC8144 UPC Register Memory Map

Address	Register Name	Acronym
0xFEE02E04	UPC Last PHY Address	UPLPA
0xFEE02E06– 0xFEE02E07	reserved	
0xFEE02E08	UPC HEC Register	UPHEC
0xFEE02E0C	UPC UCC Configuration	UPUC
0xFEE02E10	UPC Device 1 Configuration	UPDC1
0xFEE02E14– 0xFEE02E2F	reserved	
0xFEE02E30	UPC Device 1 Rate Select High	UPDRS1H
0xFEE02E34	UPC Device 1 Rate Select Low	UPDRS1L
0xFEE02E38– 0xFEE02E4F	reserved	
0xFEE02E50	UPC Device 1 Receive Priority Low	UPDRS1L
0xFEE02E54– 0xFEE02E5F	reserved	
0xFEE02E60	UPC Device 1 Event	UPDE1
0xFEE02E64– 0xFEE02E6F	reserved	
0xFEE02E70	UPC Device 1 Internal Rate Configuration	UPRP1
0xFEE02E72– 0xFEE02E7F	reserved	
0xFEE02E80	UPC Device 1 Transmit Internal Rate 0	UPTIRR1_0
0xFEE02E82	UPC Device 1 Transmit Internal Rate 1	UPTIRR1_1
0xFEE02E84	UPC Device 1 Transmit Internal Rate 2	UPTIRR1_2
0xFEE02E86	UPC Device 1 Transmit Internal Rate 3	UPTIRR1_3
0xFEE02E88– 0xFEE02E9F	reserved	
0xFEE02EA0	UPC Device 1 Port Enable Register	UPER1
0xFEE02EA4– 0xFEE03EFF	reserved	

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