Freescale Semiconductor
Application Note

Document Number: AN3406
Rev. 1, 04/2007

TV-Out Extension on the i.MX31 using the Chrontel CH7024 TV Encoder

MCIMX31 and MCIMX31L

by: Emily Hartman

1 Abstract

This document provides information to set-up and use the television output (TV-Out) of the Chrontel CH7024 daughter board with the MCIMX31 ADS Application Development System (i.MX31 ADS). The Chrontel CH7024 daughter board provides an interface between the i.MX31 LCD Controller and a TV set by converting LCD signals to TV signals.

This document presents an architectural description of the TV-Out and i.MX31 connections, an overview of the i.MX31 IPU module and the Chrontel CH7024 chip, and a sample i.MX31-CH7024 solution.

AN3406SW TV-Out Extension on the i.MX31 software file is intended to be use with this application note. See Section 6, "Reference Documentation."

This document applies to the following devices, collectively called i.MX31 throughout:

- MCIMX31
- MCIMX31L

Contents

© Freescale Semiconductor, Inc., 2007. All rights reserved.

2 Architectural Description

The i.MX31 ADS sends an image from the display buffer of its LCD Controller (LCDC) which is connected to the digital data input of the CH7024 daughter board. This includes LCD signals such as the LCD databus, HSYNC, VSYNC, and a data enable signal. The received image is converted into an analog format that can be displayed on a TV monitor.

The i.MX31 ADS uses the I^2C bus to program the registers on the CH7024 TV encoder chip by sending register read and write commands to the appropriate slave address of the CH7024 device.

The i.MX31 ADS is responsible for sending the data clock signal to the TV encoder chip. The CH7024 Evaluation Board available from Chrontel also has an on-board 13 MHz crystal used as its own reference frequency.

Figure 1 is a high-level architectural block diagram of the i.MX31 ADS and CH7024 daughter card configuration.

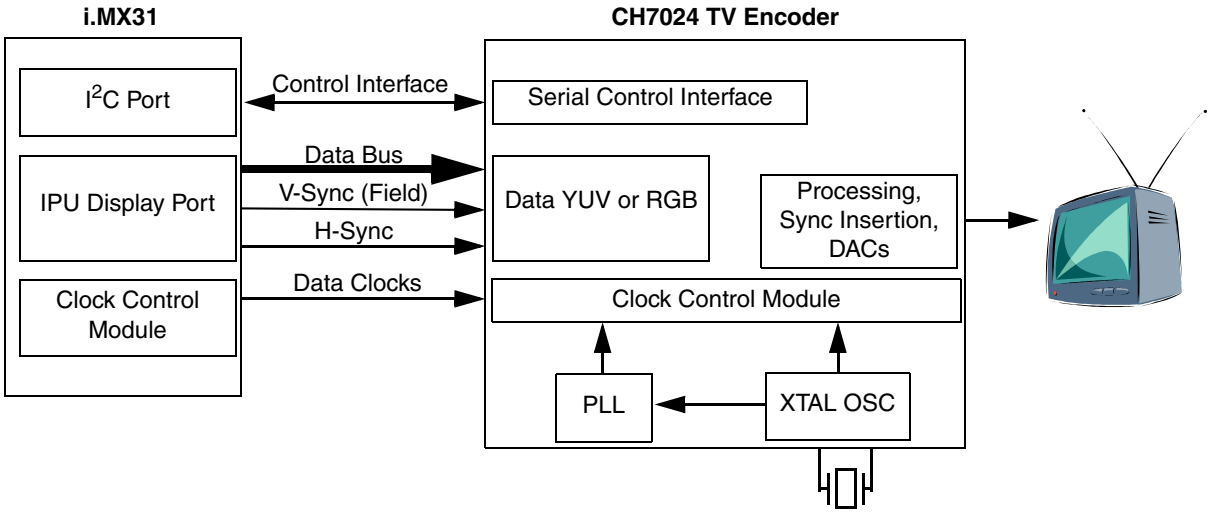

Figure 1. TV Output on i.MX31 ADS Concept Diagram

3 MCIMX31 Interfacing

3.1 MCIMX31 Display Interface

The i.MX31 processor's Display Interface simultaneously supports a synchronous interface to the display 3 and asynchronous interfaces to the displays 0, 1, and 2. The display 0 interface is only parallel while the displays 1 and 2 interfaces can be parallel or serial.

The i.MX31 processor's TV encoder interface and synchronous (dumb) display interface share the same display interface (display 3), and thus both cannot be active at the same time. The user must choose either an image on the TV or an image on the dumb LCD display.

3.2 Data Lines and Pixel Formats

The i.MX31 processor has 18 LCD data lines (LD0 – LD17). This is because most displays are 18-bit or 24-bit. However, no OS supports 18-bits as a pixel format because it does not fit into an even byte size. Thus bpp (bits per pixel) is usually 16 or 24 bpp. It is not recommended to use 24 bpp with a VGA+ sized framebuffer as flickering is likely due to the heavier bus load with 24-bpp. Because of this, 16 bpp is the preferred pixel format. When using 16 bpp, the user must pack the most significant bits of data. For example, when using the 16 bpp format of RGB565, the datalines R0 and B0 are unused.

Nonetheless, to use the full 18-bits of color, the framebuffer should be set to 24 bpp and the IPU will pack the data to 18-bits. Table 1 shows a signal map of how to double-up 18-bit signals to a 24-bit LCD interface.

Table 1. Interfacing i.MX31 Processor's 18 LCD Data Lines to a 24-bit Interface

i.MX31 IPU Signal	Color Signal	<->	24-bit LCD
IPU_LD17	R5	<->	R7
		<->	R1
IPU_LD16	R4	<->	R6
		<->	R0
IPU_LD15	R3	<->	R5
IPU_LD14	R2	<->	R4
IPU_LD13	R1	<->	R3
IPU_LD12	R0	<->	R2
IPU_LD11	G5	<->	G7
		<->	G1
IPU_LD10	G4	<->	G6
		<->	G0
IPU_LD9	G3	<->	G5
IPU_LD8	G2	<->	G4
IPU_LD7	G1	<->	G3
IPU_LD6	G0	<->	G2
IPU_LD5	B5	<->	B7
		<->	B1
IPU_LD4	B4	<->	B6
		<->	B0
IPU_LD3	B3	<->	B5
IPU_LD2	B2	<->	B4
IPU_LD1	B1	<->	B3
IPU_LD0	B0	<->	B2

3.3 i.MX31 Clock Controller Module (CCM) – Master Mode

The i.MX31 in the i.MX31-CH7024 TV-Out solution runs in Master Mode. Master mode is when the i.MX31 processor's LCD Controller is driving the clock to the TV encoder. The i.MX31 Image Processing Unit does not support slave mode, where a clock is sent to the IPU unit from the TV encoder platform that drives the image data bus.

To run i.MX31 in Master Mode:

Using a high frequency clock source on CKIH:

- Clock comes in from the CKIH pin
- PCRS register in CCMR register (0x53F80000) = 10 (binary)
- Jumper JP1 to 2-3 on the i.MX31 ADS

Using a low frequency clock source on CKIL:

- Clock comes from CKIL pin to the Frequency Pre-Multiplier (FPM)
- PCRS register in CCMR register (0x53F80000) = 01 (binary)
- Jumper JP1 to 1-2 on the i.MX31 ADS

4 About Chrontel CH7024 Chip

The CH7024 is a TV encoder device targeting handheld, portable video applications such as digital still cameras and similar portable embedded systems. The device is able to encode the video signals and generate synchronization signals for NTSC and PAL standards.

4.1 Supported TV Formats

Supported TV output formats are NTSC-M, NTSC-J, NTSC-433, PAL-B/D/G/A/I, PAL-M, PAL-N and PAL-60. The CH7024 provides video output support for CVBS or S-video.

4.2 Supported Input Data Formats

The device accepts different data formats including RGB and YCrCb (for example, RGB565, RGB666, RGB888, ITU656 like YCrCb, and so on) via 24-bit/18-bit/16-bit/15-bit non-multiplexed and 12-bit/8-bit multiplexed digital inputs. The I/O interface voltage between the CH7024 and the LCD controller can be selected by the I/O supply voltage (VDDIO). The I/O supply voltage range is from 1.2V to 3.3 V. When using the CH7024 daughter card with the i.MX31 ADS, the I/O supply voltage is generally ~3.0 V.

4.3 Image Scaling

The CH7024 does not automatically stretch an image vertically, so the user must determine the most effective pixel clock frequency, active screen size, and total screen size. If using a low resolution image (such as a QVGA image), the picture could appear stretched and thin on the screen with upper and lower bars. To fix this, use a lower pixel clock frequency so that there is minimal difference between the total screen size and the active screen size. This will be covered more in Section 5, "Example i.MX31-CH7024 Solution."

4.4 Clock Capabilities

While the i.MX31 can only run with the CH7024 in slave mode, the CH7024 has flexible clocking capabilities, and can operate in Master or Slave Mode. The general targeted pixel clock is around 27 MHz.

4.5 Packaging

The CH7024 chip is offered in both a 48-pin LQFP package (7 × 7 mm) and a 49-pin TFBGA package (6 × 6 mm). The CH7024 48-pin LQFP package comes with fixed single serial port address while the 49-pin TFBGA package provides two user-selectable serial port addresses via the AS pin pull-up or pull-down option. Refer to application note *AN-98* available from Chrontel (http://www.chrontel.com) for more information.

For more information on the Chrontel chip's functionality, please refer to the *CH7023/CH7024 TV Encoder Brief Summary* and the *CH7023/CH7024 TV Encoder Datasheet,* which can be obtained by contacting Chrontel (http://www.chrontel.com).

5 Example i.MX31-CH7024 Solution

With all the input data formats possible on the CH7024, this application note focuses on providing an example of the most popular input pixel format, 16-bit RGB565. This example sends data of a VGA resolution (640 × 480) to the CH7024 chip. Sample stand-alone code for this particular example can be found Section Appendix A, "Sample Stand-Alone Code."

Step 1: Connect the i.MX31 ADS to the CH7024 daughter card

Table 2 lists the connections to be made between the i.MX31 ADS and the CH7024. First make these connections from the i.MX31 ADS to the CH7024 daughter card. Note that if the CH7024 daughter card has a jumper for selecting the voltage for VDDIO to be either 1.8 V or 3.3 V, jumper this voltage to the 3.3 V option or leave the jumper floating. The reason to chose the 3.3V option or the floating option is to better match the voltage of the LCD data signals from the i.MX31 processor.

Table 2. i.MX31 ADS to CH7024 Signal Connections

Chrontel Signal Name	i.MX31 ADS Pin	i.MX31 Signal Name
D[0]	25	LD1 (B1)
D[1]	10	LD2 (B2)
D[2]	9	LD3 (B3)
D[3]	8	LD4 (B4)
D[4]	7	LD5 (B5)
D[5]	28	LD6 (G0)
D[6]	27	LD7 (G1)
D[7]	14	LD8 (G2)
D[8]	13	LD9 (G3)

Table 2. i.MX31 ADS to CH7024 Signal Connections (continued)

Chrontel Signal Name	i.MX31 ADS Pin	i.MX31 Signal Name
D[9]	12	LD10 (G4)
D[10]	11	LD11 (G5)
D[11]	29	LD13 (R1)
D[12]	18	LD14 (R2)
D[13]	17	LD15 (R3)
D[14]	16	LD16 (R4)
D[15]	15	LD17 (R5)
D[16]	NO CONNECT	NO CONNECT
D[17]	NO CONNECT	NO CONNECT
H	5	HSYNC
V	4	VSYNC3
DE	3	DRDY0
SPC	J16 - pin 3	I2C_CLK
SPD	J16 - pin 5	I2C_DAT
XCLK	6	FPSHIFT
GND	2	GND
3.3 V Power	1	3.3 V Power

Step 2: Configure the i.MX31 Clock Controller Module to run in Master Mode (with CH7024 running in Slave Mode)

As stated in Section 4.4, "Clock Capabilities," the CH7024 can run in Slave Mode or Master Mode. This example will run the CH7024 in Slave Mode and thus the i.MX31 processor in Master Mode and provide the clock signal to the CH7024 chip. To run the CH7024 in Slave Mode, configure the Clock Controller Module register and the i.MX31 ADS as follows:

- Set PCRS register in CCMR register (0x53F80000) = 01 (binary)
- Jumper JP1 to 1-2 on the i.MX31 ADS (so clock comes from FPM)

Step 3: Choose the Pixel Clock Speed

The MCU main clock feeds the HSP_CLK of the i.MX31 processor. The HSP_CLK is then divided to form the pixel clock (signal FPSHIFT on the i.MX31).

- The MCU main clock is controlled by the MPCTL register (0x53F80010)
- The HSP_CLK is controlled by the HSP_PODF register in the PDR0 register (0x53F80004)
- The pixel clock (FPSHIFT) is controlled by the DISP3_IF_CLK_PER_WR register in the DI_DISP3_TIME_CONF register (0x53FC015C)

In this example, the MCU main clock is set to 532 MHz, the HSP_CLK is set to 133 MHz (MCU main divided by 4), and the pixel clock is set to 26.6 MHz (HSP_CLK divided by 5). In the accompanying sample code, the MCU and HSP_CLK are set in the initialization script and the pixel clock register is set in the code.

For more information on these registers, please refer to the *MCIMX31 and MCIMX31L Applications Processors Reference Manual*, available from the i.MX website (http://www.freescale.com/imx).

Step 4: Determine Active Screen Size and Total Screen Size

An active screen size and a total screen size must be programmed in the i.MX31 processor and the CH7024 chip. The active screen size is simply the resolution of the image. For example, if the image is of a VGA resolution, the active screen width would be 640 and the active screen height would be 480.

The total screen size is adjustable and is used to meet the correct TV frames per second requirement with the given pixel clock. In TV-Out encoding, it is important that the TV screen is refreshed at a rate of approximately 60 frames per second for NTSC and 50 frames per second for PAL. Thus, with a given frames per second, the variables a user can tweak are the pixel clock, the total screen width, and the total screen height. These variables must be chosen such that Equation 1 is correct:

Eqn. 1

$$\text{Total Screen Width} \times \text{Total Screen Height} \times \text{Frame Rate} = \text{Pixel Clock}$$

where Frame Rate is 59.94 Hz for NTSC and 50 Hz for PAL

In this example, a pixel clock of 26.6 MHz is used. Thus the Total Screen size is rather arbitrary so that it correctly completes this equation. For this example, the Total Screen Width is 915 and the Total Screen Height is 485 and is applied to NTSC. Chrontel provides a register setting tool which outputs possible total screen values when given the pixel clock.

A rule to select a good total screen height is:

Total Screen Height should approximate: [Active Screen Height X Total Active Ratio X (1.1)]

where Total Active Ratio is 525/480 for NTSC and 625/576 for PAL

In the CH7024, the active screen size can be programmed in the Input H active and Input V active registers, and the total screen size can be programmed in the Input H total and the Input V total registers. In the i.MX31 processor, the total screen width can be programmed in the SDC_HOR_CONF register (0x53FC00D0) and the total screen height can be programmed in the SDC_VER_CONF register (0x53FC00D4).

Step 5: Configure the various settings of the CH7024 register's via the i.MX31's I^2C bus

The settings for the CH7024 registers are programmed via the I^2C bus. The user must broadcast the device's slave address on the I^2C bus, followed by read or write commands. Application note AN98 is available from Chrontel upon request and describes the slave address to be used for the CH7024. For this example, the following slave addresses are used for the CH7024 for reading and writing:

Write slave address = 0xEC

Read slave address = 0xED

This example has the following characteristics that must be programmed into the CH7024. The registers in which to program these settings, as well as the values used in the stand-alone code example are provided in Table 3.

Table 3. CH7024 Register Settings

Setting	CH7024 Register	Register Value
S-Video	0x0A	0x60
CH7024 in Slave mode	0x0E	0x0C
26.6 MHz Pixel Clock	Various registers	See CH7024 datasheet and CH7024.c
640x480 resolution	0x11, 0x12, 0x17, 0x18	0x9A, 0x80, 0x05, 0xE0
RGB565 - SWAP[2:0] = 110b	0x0D	0x33
RGB565 - IDF[2:0] = 011b	0x0D	0x33
MULTI = 0	0x0C	0x00
REVERSE = 0	0x0D	0x33
HIGH = 0	0x0D	0x33

For a full list of CH7024 register settings, see the sample stand-alone code in CH7024.c in *AN3406SW* that accompanies this application note. For more information on programming the CH7024 registers, please review the *CH7023/CH7024 TV Encoder Brief Datasheet,* which can be obtained by contacting Chrontel http://www.chrontel.com.

6 Reference Documentation

For more information about the i.MX31 devices refer to the following documents. Freescale documents are located at: http://www.freescale.com/imx.

MCIMX31 Applications Processors Reference Manual (document number MCIMX31RM)

AN3406SW TV-Out Extension on the i.MX31 (document number AN3406SW)

For more information about the Chrontel CH7024 daughter board, please refer to the following documents. Chrontel documents are located at: http://www.chrontel.com.

CH7023/CH7024 TV Encoder Brief Datasheet,

Appendix A Sample Stand-Alone Code

The sample stand-alone code for the i.MX31 ADS requires the ARM Realview® development tools (IDE and Multi-ICE®) to run. This code displays the image of two Sumo wrestlers on a TV screen. It has the characteristics described in Section 5, "Example i.MX31-CH7024 Solution." See Section 6, "Reference Documentation for information on locating the AN3406SW file.

To load this demo, please follow these steps:

1. Unzip the stand-alone code, go to the TOOL folder, and open the RVDS folder. Open the RVD_MX31_DDR_CHRONTEL.inc file for editing. This is where certain modules are initialized, such as the clock controller module and the SDRAM. Go down to the bottom line and enter the correct path name on your PC that points to this file. From the top of the stand-alone code directory, this Sumo .bin file can be found at \SDK\TEST\SUMO\BIN.
2. Ensure that the i.MX31 ADS Jumper 1 (JP1) is set to 1-2 on the CPU card. Connect to the CH7024 daughter card as described in Table 2, and connect the CH7024 card via S-video cable to a television. Power on the board and the TV.
3. In the ARM Realview Debugger tool, connect to the i.MX31 ADS board. Load the script described in step 1.
4. Load the mx31.axf file located from the top of the stand-alone directory at \PROJECT\MX31ADS\DebugRAM and press go to run the code. You will see the SUMO image loaded on the television.

Figure 2 shows the file tree for this project. This code tree can be viewed by opening the MX31.mcp file in the /PROJECT/MX31ADS/ folder of the unzipped content.

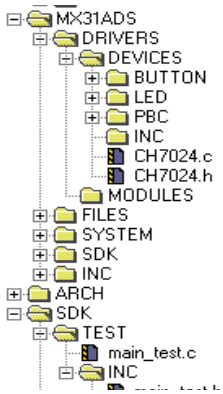

Figure 2. Project File Tree

The following code can be found in the unzipped AN3406SW file:

main_test.c – Location of the main() executable

CH7024.c – Location of where the CH7024 registers are programmed

\MX31\Drivers\Modules\IPU\ipuSdc.c – Location of where IPU values are set, such as HSYNC, VSYNC, screen resolution, and IPU DMA settings.

7 Revision History

Changes from Rev. 0 to this current revision are identified in Table 4.

Table 4. Revision History

Location	Description of Change
Section 2, “Architectural Description	Replaced paragraph 3.
Figure 1	Removed arrow “Reference Clock” between i.MX31 and the CH7024 TV Encoder.
Section 3.3, “i.MX31 Clock Controller Module (CCM) – Master Mode	Changed heading from i.MX31 Clock Module (CCM) – Slave Mode Versus Master Mode to current heading.
Section 3.3, “i.MX31 Clock Controller Module (CCM) – Master Mode	Replaced all text within section.
Section 4.4, “Clock Capabilities	Replaced paragraph.
Section 5, “Example i.MX31-CH7024 Solution	Step 2: Changed cross reference from Section 3.3 to Section 4.4.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

***For Literature Requests Only*:**
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals”, must be validated for each customer application by customer’s technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. ARM, the ARM Powered logo, Multi-ICE, and Realview are registered trademarks of ARM Limited.

© Freescale Semiconductor, Inc. 2007. All rights reserved.

Document Number: AN3406
Rev. 1
04/2007