

# MSC8144 CLKIN and PCI\_CLK\_IN Board Layout

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This application provides an example that implements a layout design for the MSC8144 DSP CLKIN circuit. The same guidelines apply to the PCI\_CLK\_IN circuit.

The example layout uses the following components:

- Oscillator: PRECIDIP part 11093-30841-001.
- Clock Buffer: ICS part ICS551MLF.

## NOTE

These parts are identified for example purposes only. Use of these part in this application note does not imply a requirement or recommendation for individual system designs.

## NOTE

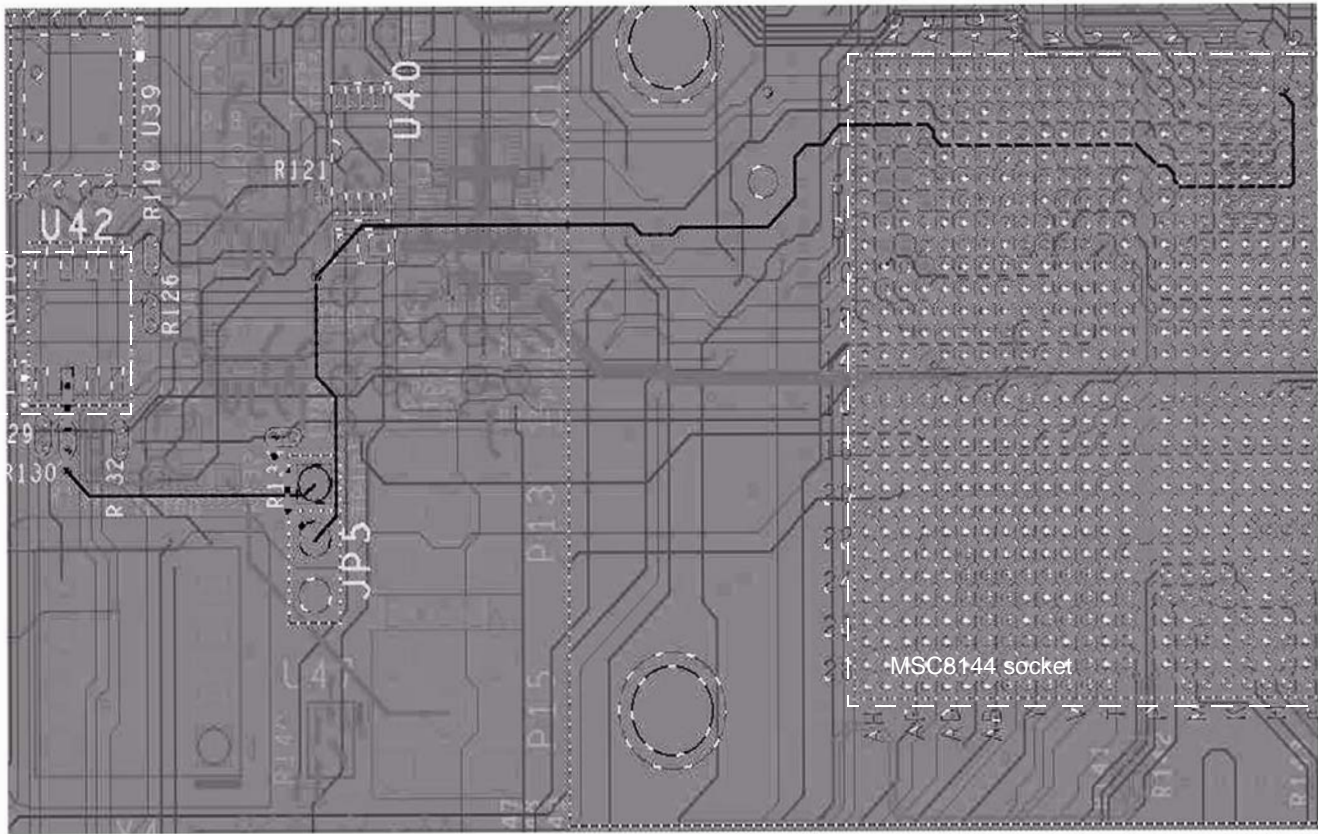
While this application note is specific for the MSC8144, it also applies to the MSC8144E and MSC8144EC devices.

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# 1 CLKIN Signal Layout Example

Figure 1 shows an example layout for the CLKIN signal path.



- Note:** Trace length is about 4 inches.
- U42 is the serial clock buffer.
  - R130 is a 33  $\Omega$  serial termination resistor.
  - J5 is a jumper connection.
  - R131 is an optional parallel termination resistor.

**Figure 1. Route from Buffer to CLKIN Signal Connection**

## 2 Route from the Oscillator to the Clock Buffer

Figure 2 shows an example layout for the signal path route from the oscillator to the clock buffer.

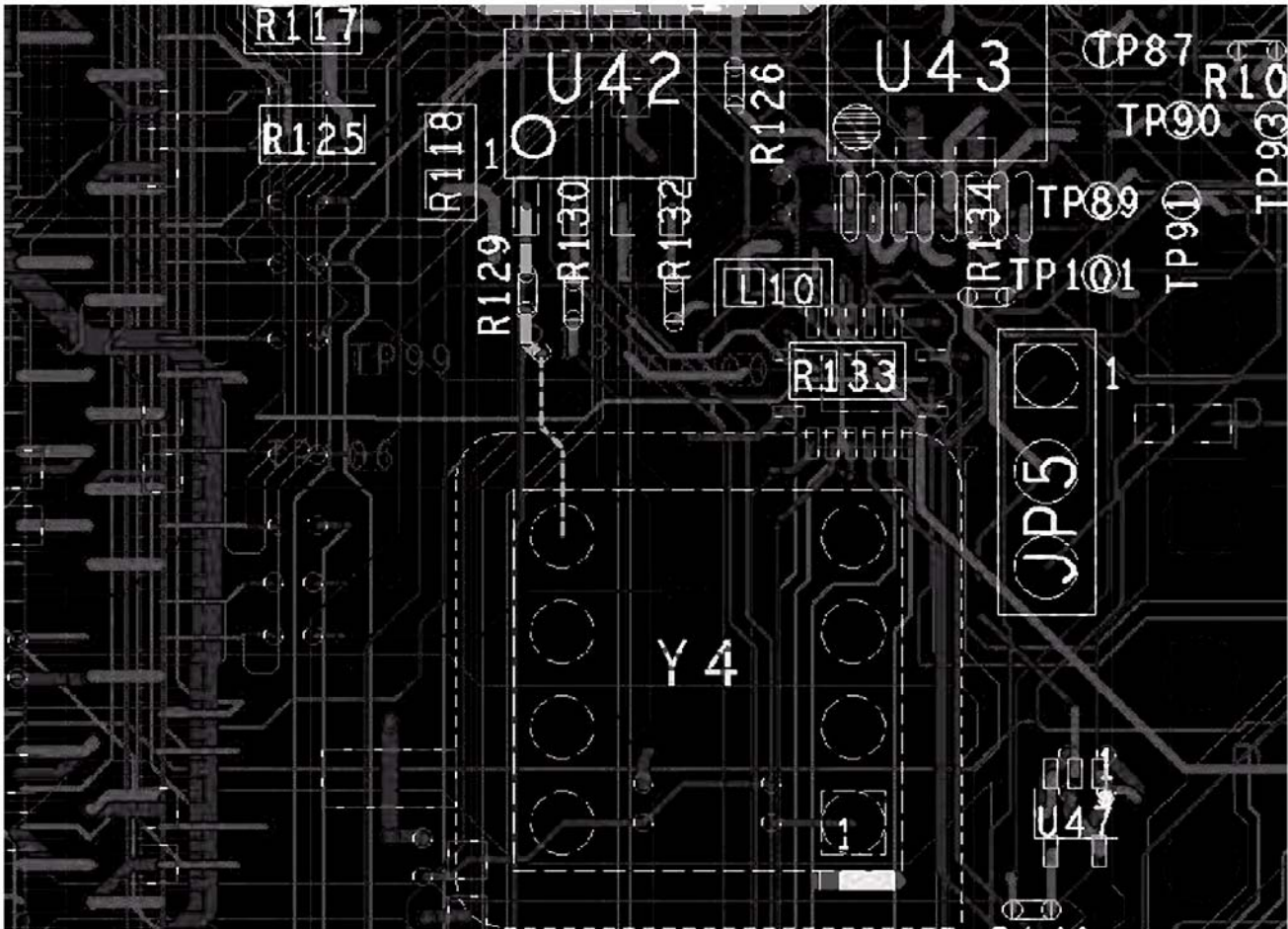


Figure 2. Oscillator to Clock Buffer Signal Route

## 3 Guidelines

1. Route clock traces with 50  $\Omega$  impedance.
2. To prevent signal reflection, use a serial termination resistor placed close to the CLKIN buffer. Use the following equation to compute the required termination value ( $R_{term}$ ):

$$R_{term} = R_{im} - R_{buf} \quad \text{Eqn. 1}$$

where  $R_{im}$  = trace characteristic impedance  
 $R_{buf}$  = clock buffer internal impedance.

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