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Application Note

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Migrating from the MC68HC908QT4 to the MC9S08QD4

by: Han Lin
8-Bit Applications Engineering
Microcontroller Division
Austin, Texas

1 Introduction

This document provides guidelines on migrating from an MC68HC908QT4 to an MC9S08QD4. Freescale's 8-pin MC9S08QD4 is an easier to use, cost effective, higher performance upgrade from the 8-pin MC68HC908QT4. The MC9S08QD4 is the low-cost entry point to Freescale's HCS08 family. Migrating to the MC9S08QD4 eases migration to other higher performance HCS08 series, all the way up to the 32-bit ColdFire® V1 Family.

This application note describes similarities and differences between the MC68HC908QT4 and the MC9S08QD4. Some of the sections require more in-depth discussions than is provided in this application note. Related supplementary application notes are referenced at www.freescale.com. For details, consult the MC9S08QD4 reference manual and data sheet.

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NOTE

Except mask set errata documents, if any other Freescale document contains information conflicting with the device data sheet, the data sheet must be considered to have the most current and correct data.

2 Feature Comparisons

Table 1. Feature Comparisons

MCU Features		MC68HC908QT4	MC9S08QD4
Core		M68HC08	HCS08
CPU clock sources	Built-in	12.8 MHz (generates up to 3.2 MHz internal bus frequency)	16 MHz (generates up to 8 MHz internal bus frequency)
	External	Yes	Not available
Development support		(Monitor module) MON	(Background debug controller) BDC
Power supply		2.7 to 5.5 V[1]	2.7 to 5.5 V
RAM (bytes)		128	256
Flash (bytes)		4096	4096
Low power modes		Wait, stop	Wait, stop2, stop3
COP		Yes	Yes
Low voltage detection		Yes (LVI)	Yes (LVD)
Analog-to-digital converter (ADC)		One 4-ch 8-bit	One 4-ch 10-bit
Keyboard interrupt (KBI)		6 channels	4 channels
Timer		2-ch 16-bit (TIM1)	2-ch 16-bit (TPM1)
			1-ch 16-bit (TPM2)
Packages		8-pin: PDIP/SOIC/DFN	8-pin: PDIP/SOIC

[1] If you are migrating from the low power MC68HLC908QT4 series that has a lower operational voltage supply (Vdd) range than the MC9S08QD4. A Vdd compatible upgrade can be an MC9S08QG4 or an MC9S08QG8 which is similar to the MC9S08QD4 but has a lower Vdd range (1.8V – 3.6V).

2.1 Major Benefits of Migrating to the MC9S08QD4

- Cost effective
- Higher internal bus speed with no need for an external clock source; faster internal clock source and CPU
- Advance I/O that enables slew rate control and drive strength control
- Twice the RAM space

- Improved EMC
- Fast ADC with 10-bit resolution
- A built-in temperature sensor in the ADC module
- Reduced current draw during operation (less run I_{DD})
- Non-intrusive on-chip debugging system
- Less frequency deviation on internal clock source
- One additional 16-bit timer module (TPM2)

2.2 Potential Incompatibilities of Migrating to an MC9S08QD4

- External crystal not supported
- No DFN package
- Depending on the user´s application, a 4-pin KBI in the MC9S08QD4 may not meet the 6-pin KBI requirement from the MC68HC908QT4
- Pinout differences

2.3 Pin-to-Pin Conversion

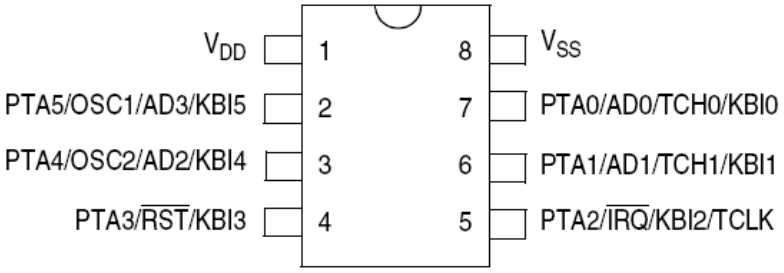

Figure 1. MC68HC908QT4 PDIP/SOIC 8-Pin Assignment

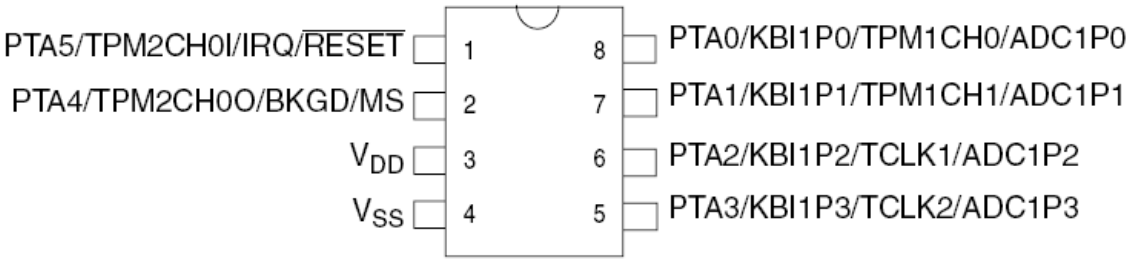

Figure 2. MC9S08QD4 DIP/SOIC 8-Pin Assignment

The multiplexed functions on each pin of the MC68HC908QT4 are different than the MC9S08QD4. The available functions are similar. In the case of the V_{SS} and V_{DD}, a hardware connection reroute is necessary.

3 Interrupt Request (IRQ)

The MC68HC908QT4 $\overline{\text{IRQ}}$ responds to falling-edge events only or falling-edges and low-level events. The MC9S08QD4 IRQ has selectable internal pull-up or pull-down modes allowing responses for falling-edge, low-level, rising-edge, and high-level sensitive events. The IRQ is default to falling-edge-triggered out of reset for both the MC68HC908QT4 and the MC9S08QD4.

The MC68HC908QT4 has interrupt request ($\overline{\text{IRQ}}$) and reset ($\overline{\text{RST}}$) on separate pins. The MC9S08QD4 has IRQ and $\overline{\text{RESET}}$ multiplexed on the same pin (pin 1). When $\overline{\text{RESET}}$ is enabled on pin 1, the IRQ loses its functionality to $\overline{\text{RESET}}$. $\overline{\text{RESET}}$ has a higher functional priority than the IRQ. To compensate the loss of the IRQ function, use a KBI from other pins as an IRQ. The enhanced KBI for the MC9S08QD4 has a similar functionality to an IRQ that triggers interrupts after detecting rising-edge, falling-edge, high-level or low-level events. MC68HC908QT4 $\overline{\text{IRQ}}$ settings are configured through the INTSCR and CONFIG2 registers. MC9S08QD4 IRQ settings are configuring through the IRQSC.

4 Watchdog Computer Operating Properly (COP)

Both the MC9S08QD4 and MC68HC908QT4 have a COP to force a system reset back to a known starting point if the application software fails to execute as expected.

The COP in the MC68HC908QT4 runs from only one oscillator output signal (BUSCLKX4). The system clock also shares this signal.

The COP in MC9S08QD4 has a software selectable clock source to run either from the bus clock or a low power internal 1 kHz clock source. The benefit of using the 1 kHz clock source is because it is independent from the system clock. If the system clock is out of order, the COP is still able to force a reset. The MC68HC908QT4 COP can rely only on the system clock.

5 Development Support

The MC68HC908QT4 uses a monitor module (MON). The MC9S08QD4 uses a background debug controller (BDC).

Both BDC and MON modules provide ways to analyze an MCU operation during software development, such as debugging application code.

The MC9S08QD4 BDC has the following major benefits over the MC68HC908QT4 MON:

- BDC — is a single-pin interface that simplifies the hardware set up process. The MON uses only one pin to communicate, but requires several pins to be controlled to enter MON mode.
- BDC — has self-clocking capability, and does not require a specific baud rate to communicate to the MCU.
- BDC — can read the MCU address in real time where an MC68HC908QT4 must halt the application to read address contents.
- BDC — requires only one power source Vdd to enter active background mode. MON requires two power sources one to the Vdd pin and another on the $\overline{\text{IRQ}}$ pin to enter normal monitor mode if the reset vector is not blank.

See application note AN2497: *HCS08/RS08 Background Debug Mode versus HC08 Monitor Mode*. This application note provides guidelines for migration that also apply to the MC68HC908QT4 and MC9S08QD4.

6 Voltage Supply Range

Both the MC68HC908QT4 and the MC9S08QD4 have the same operating voltage range, from 2.7 V to 5.5 V.

The MC9S08QD4 is part of the HCS08 family. It can operate in low-voltage/low-power performance without sacrificing CPU performance. The MC9S08QD4 can maintain maximum bus speed across the entire voltage operating range (2.7V – 5.5V).

7 Low-Voltage Detect System

Both the MC9S08QD4 and the MC68HC908QT4 have systems to protect against low-voltage conditions, preserve memory contents, and control the MCU operation during supply voltage variations. The MC9S08QD4 uses a low-voltage detect (LVD) module. The MC68HC908QT4 uses a low-voltage inhibit (LVI) module.

The LVI and LVD have two low voltage detection points:

- The MC9S08QD4 LVD typical trip falling voltage is 2.56 V or 4.3 V.
- The MC68HC908QT4 LVI typical trip falling voltage is 2.55 V or 4.2 V.
- The LVD and LVI modules force a reset when the V_{DD} voltage falls below the trip falling voltage.

Key enhancements of the MC9S08QD4 LVD:

- MC9S08QD4 — has a choice of low-voltage warning thresholds that set a warning flag (LVWF). This flag indicates the supply voltage is approaching the low-voltage condition. The MC68HC908QT4 LVI does not have this feature.
- MC9S08QD4 — low-voltage detect flag (LVDF) can be configured to generate an interrupt other than reset when the lower voltage trip point is detected. The MC68HC908QT4 LVI resets itself and the flag.
- MC9S08QD4 — the LVD is configured using the system power management status and control registers (SPMSC1 and SPMSC2). The MC68HC908QT4 LVI is configured using CONFIG1 register.

8 Low-Power Modes

The MC68HC908QT4 has wait and stop mode.

The MC9S08QD4 has wait, stop2, and stop3 mode.

Wait — This is a mode available in both the MC68HC908QT4 and MC9S08QD4. They behave the same and are entered by executing an assembly WAIT instruction. In wait mode, the CPU is not clocked, reducing power consumption. The CPU's condition code register (CCR) interrupt mask bit (I) is cleared when the CPU enters the wait mode, enabling interrupts from peripherals. When an interrupt is requested

by one of the peripherals, the CPU exits the wait mode and resumes processing, beginning with the stacking operations leading to the interrupt service routine.

Stop — This is a mode in the MC68HC908QT4 and behaves the same as the stop3 mode in the MC9S08QD4. In stop3 mode, the internal regulator is put into a loose regulation mode in which it consumes little current but also supports the static state of RAM and registers. One difference between stop3 and stop mode is how the recovery is managed.

Stop recovery on the MC68HC908QT4 is a timed event lasting 32 or 4096 BUSCLKX4 cycles, plus the time the oscillator source uses to start. On the MC9S08QD4, stop3 recovery is based on the voltage regulator's time to power up and return to full regulation.

Stop2 — This is the lowest power mode available for the MC9S08QD4. In this mode, RAM content is retained. Recovery on the MC9S08QD4 always takes the reset vector regardless of the method to wake the MCU from stop2. After reset from stop2, the system and all peripherals reset to default. To recover, it is necessary to first save the registers content to the RAM prior entering stop2 and then copy the content from the RAM back to the registers after stop2 is reset.

To distinguish a stop2 recovery from a normal reset, examine the status of the partial power down flag (PPDF) in the system power management status and control register 2 (SPMSC2). The PPDF is automatically set after waking from stop2. The flag may be used to direct user code to go to a stop2 recovery routine. The PPDF remains set and the I/O pins remain latched until a 1 is written to the partial power down acknowledge (PPDACK) bit in the SPMSC2.

9 Auto Wakeup (AWU) vs. Real-Time Interrupt (RTI)

Both the RTI in the MC9S08QD4 and the AWU in the MC68HC908QT4 provide clocking mechanisms to generate periodic interrupts to wake the MCU from low power modes.

For the MC68HC908QT4, the AWU is active only in stop mode and shares the KBI interrupt vector. The AWU has only two selectable interrupt periods (650 ms or 16 ms when the Vdd = 5V, 875 ms or 22 ms when the Vdd = 3V).

For the MC9S08QD4, the RTI is active for all modes (run, wait, stop2, and stop3) and the RTI interrupt vector is independent from the KBI interrupt vector. The RTI operates using either the low power 1 kHz internal clock or the 32 kHz internal reference clock (ICSIRCLK). The RTICLKS bit in the SRTISC is used to select either clock source. Both the 1 kHz internal clock and the internal reference clock (ICSIRCLK) can be used when the MCU is in run, wait or stop3 mode. Only the internal 1 kHz clock source can be selected to wake the MCU from stop2 mode. The RTI has seven selectable interrupt periods (8 ms, 32 ms, 64 ms, 128 ms, 256 ms, 512 ms, and 1.024 s).

10 Peripherals

10.1 Clock Sources

MC68HC908QT4 runs from an external clock source or a built-in internal clock source through its oscillator (OSC) module. The MC9S08QD4 runs only from a built-in internal source called internal clock

source (ICS) module. The MC68HC908QT4 built-in internal clock has a 5% of deviation. The MC9S08QD4 built-in internal clock has a 2% of deviation, offering a more accurate clock source.

The MC68HC908QT4 OSC supports external oscillators, quartz crystals, ceramic resonators, or resister-capacitor (RC) circuits that provide an external clock source to the MCU. When the OSC is configured to use an internal clock source, the OSC incorporates a built-in internal oscillator. On the MC68HC908QT4, the internal bus clock frequency is always one fourth of any of the OSC source options. On the MC9S08QD4, the internal bus clock frequency is always one half of the ICS generated frequency.

The MC68HC908QT4 and the MC9S08QD4 are limited to run at a maximum of 8 MHz bus speed. Applications run on MC68HC908QT4 using the internal oscillator run only up to a maximum of 3.2 MHz bus speed (INTCLK divided by 4). To run at a maximum of 8MHz bus speed, the MC68HC908QT4 OSC module requires Vdd at 5V and incorporates an external 32 MHz reference clock such as the canned crystal oscillator. When the Vdd is at 3V, the MC68HC908QT4 OSC can run only at a maximum of 4MHz bus speed with a 16 MHz external reference clock. The need of the external reference clock requires a larger board design and higher power supply.

The MC9S08QD4 eliminates the need for an external oscillator by providing an internal ICS module capable of a higher bus frequency and accuracy. After porting to the MC9S08QD4, applications can run up to a maximum of 8 MHz bus speed (ICSOUT/2) using only the internal clock. The MC9S08QD4 ICS can maintain maximum bus speed across the entire voltage operating range (2.7V – 5.5V).

The MC9S08QD4 does not support the external clock source. Applications run on the MC68HC908QT4 from an external clock source must be converted to run on the MC9S08QD4 internal ICS module.

10.2 Timer

Table 2. Key Differences Between the MC9S08QD4 and MC68HC908QT4

Timer	MC9S08QD4	MC68HC908QT4
Quantity	Two timers (TPM1 and TPM2)	Only one timer (TIM)
TPM external input clock source	TCLK1 and TCLK2	TCLK
Counter mode	Up/down counter	Only up counter
Output compare	Yes	Yes
Input capture	Yes	Yes
PWM edge-aligned	Yes	Yes
PWM center-aligned	Yes	No
Clock sources	3	2
Operating modes	Run, wait	Run, wait
Clock prescalers	8 (divide by 1, 2, 4, 8, 16, 32, 64, or 128)	7 (divide by 1, 2, 4, 8, 16, 32, or 64)

The MC9S08QD4 uses a new timer called the timer/ PWM module (TPM), designed for the HCS08 family. It performs all the functions of the M68HC08 family's timer interface module (TIM) used by the MC68HC908QT4. The HCS08 TPM also reduces the complexity of the M68HC08 TIM functions and improves the use of the MCU resources.

Key enhancements of the MC9S08QD4 timer:

- The MC9S08QD4 has two timer modules, TPM1 and TPM2. The TPM1 and TPM2 have their separate external clock sources from TCLK1 and TCLK2. The MC68HC908QT4 has only one TIM1 module with one external TIM1 clock source TCLK.
- The TPM has an up/down count mode. The TIM counts only up. Center-aligned PWM signals are created with the TPM. This is not possible with the TIM.
- TPM clock source can be selected from either the bus clock, external clock TCLKn, or the fixed system clock (XCLK). The TIM clock source is limited to the bus clock or an external clock.
- The selected TPM clock source is divided by eight prescalers: 1, 2, 4, 8, 16, 32, 64, or 128. The TIM clock source has seven prescalers: 1, 2, 4, 8, 16, 32, and 64.
- Any single channel can be configured for the buffered PWM on the TPM.
- The TIM requires two channels to generate a buffered PWM.
- The register interface has been modified to make programming the TPM easier.

Please refer to AN2717 -- *M68HC08 to HCS08 Transition* section 6.4. This section provides steps to configure the TPM that is applicable to the MC9S08QD4 TPM.

10.3 Analog-to-Digital Converters

Table 3. Key Differences Between MC9S08QD4 and MC68HC908QT4

Analog-to-Digital Converters	MC9S08QD4	MC68HC908QT4
Resolution	10-bit or 8-bit	8-bit only
Conversion clock frequency	Up to 8 MHz	Up to 1 MHz
Built-in temperature sensor	Yes	—
Hardware trigger	Yes	—
Automatic compare function	Yes	—
Operating modes	Run, wait, stop3	Run, wait
Bandgap voltage reference	Yes	—
Clock sources	3	2
ADC pin control	Yes	—
Single conversion time (max)	~3.1 S (8-bit); ~3.5 S (10-bit)	~16 S (8-bit)
Clock prescalers	4 (divide by 1, 2, 4, or 8)	5 (divide by 1, 2, 4, 8, or 16)

Key enhancements of the MC9S08QD4 ADC:

- Output is formatted in a 10- or 8-bit right-justified format.
- A temperature sensor is included in the MC9S08QD4 ADC module. The temperature sensor output is attached to one of the ADC analog input channels (AD26) AN3031: *Temperature Sensor for the HCS08 Microcontroller Family* has useful guidelines for implementing the temperature sensor feature.
- The MC9S08QD4 ADC hardware trigger (ADHWT) is output from the real-time interrupt (RTI) counter. The RTI counter is clocked by either the ICSERCLK or a nominal 32 kHz clock source

within the RTI block. When enabled, the hardware trigger initiates a conversion on an RTI overflow.

- The automatic compare function of the MC9S08QD4 is configured to check for an upper or lower limit. If the compare condition is met, the conversion complete flag (COCO) is set and an interrupt occurs, if the ADC interrupt is enabled. If the compare condition is not met, the conversion complete flag is not set. The automatic compare function monitors a voltage on a channel in either wait or stop3 mode. When the compare condition is met, the resulting ADC interrupt (if enabled) wakes the MCU.
- The ADC's clock source can be selected either from the MCU bus clock, the bus clock divided by two, or the local asynchronous clock (ADACK) within the module. The alternate clock (ALTCLK) input for the MC9S08QD4 Series MCU devices are not implemented.
- The ADACK is within the ADC module. When ADACK is selected as the clock source, this clock remains active while the MCU is in wait or stop3 mode and allows conversions in these modes for lower noise operation. The ADC with ADACK selected can also wake the MC9S08QD4 from wait and stop3 modes.
- The MC9S08QD4 ADC pin control feature is used to disable the I/O port control of the pins used as analog inputs. The pin control register(APCTL1) gives each ADC pin a control bit allowing pins used by the ADC to be reserved, by disabling the I/O port control of the pins used as analog inputs. This also masks pins that are not to be used as ADC inputs so they cannot accidentally be selected by the ADC input channel select.

Please refer to AN2717 -- *M68HC08 to HCS08 Transition* section 6.9. This section provides a detailed ADC module that is generally used in the HCS08 MCUs.

10.4 Parallel Input/Output Control

The MC9S08QD4 has a total of four bidirectional I/O pins, one output-only pin, and one input-only pin. The MC68HC908QT4 has a total of five bidirectional I/O pins and one input only pin.

Key enhancements of the MC9S08QD4 I/O pins:

- Each port pin can be enabled for slew rate control by setting the corresponding bit in the PTxSEn register. Slew rate control limits the rate at that an output signal can transition to reduce EMC emissions. Slew rate control has no effect on pins that are configured as inputs.
- Each output pin can be enabled for high output drive strength by setting the corresponding bit in the PTxDSn register. Enabling the high drive strength function allows a pin to source and sink greater current. Enabling I/O high drive, the user must ensure that the total current source and sink limits for the MCU are not exceeded. The drive strength selection is intended to affect the DC behavior of I/O pins. The AC behavior is also affected. High drive allows a pin to drive a greater load with the same switching speed as a low-drive-enabled pin into a smaller load. Enabling pins as high drive may affect EMC emissions.

10.5 KBI

The MC68HC908QT4 uses a keyboard interrupt (KBI) module to provide six independently external interrupt pins. The MC9S08QD4 has four.

The MC68HC908QT4 and MC9S08QD4 KBI external interrupt pins can be enabled or disabled individually.

Key enhancements of the MC9S08QD4 KBI:

- Each keyboard interrupt pin is programmable for interrupt sensitivity at falling-edge, rising-edge, falling-edge and low-level, or rising-edge and high-level. The MC68HC908QT4 is falling-edge or falling-edge and low-level interrupt only.
- The interrupt sensitivity of each KBI pin is configured by the KBISC register and KBIES register.

11 Conclusion

Freescale's MC9S08QD4 offers similar functions and allows easy migration from the MC68HC908QT4 modules. The MC9S08QD4 enhancements include a faster internal clock source, doubled RAM size, lower power consumption mode, a simpler background debugger controller, enhanced ADC with a built-in temperature sensor, I/O drive strength and slew rate controls, KBI rising/falling-edge detections, and two timer modules capable of PWM center-aligned output signal. These upgrades allow programmers or designers to enhance the applications by migrating to the cost-effective MC9S08QD4.

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+1-800-521-6274 or +1-480-768-2130
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Europe, Middle East, and Africa:
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+44 1296 380 456 (English)
+46 8 52200080 (English)
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+33 1 69 35 48 48 (French)
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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
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support.asia@freescale.com

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