Freescale Semiconductor
Application Note

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Using an External DMA Controller with Freescale Processors that Support Serial RapidIO® Technology

This application note describes an example of how to use an external DMA engine with a Serial RapidIO® interface.The discussion includes the following:

- A reference design showing the design benefits
- Block diagrams illustrating the data and configuration paths
- An evaluation of the implementation throughput

The design is portable and can accelerate system design time.

Contents

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1 Intermediate Buffering for Processing Elements

In a WiMAX baseband communication system, an FPGA can be used with a StarCore®-based DSP to perform application-specific tasks such as interpolation or filtering, as shown in Figure 1.

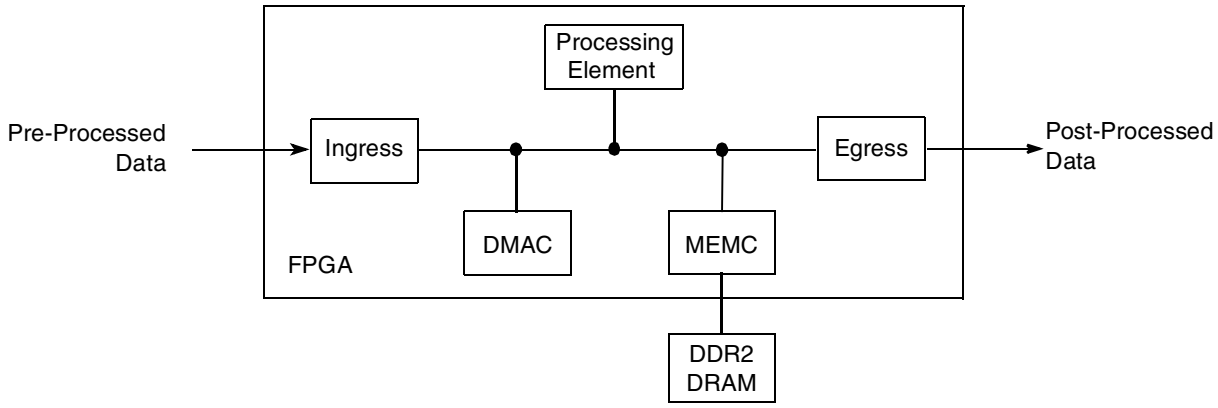

Figure 1. Example Communication System

The FPGA allows use of a local DDR2 memory controller to buffer data and a local DMA engine to transfer data between the StarCore processor and the FPGA. If the DDR2 memory is a lookaside buffer, then the ingress data, processed data, and egress data must share the memory access bandwidth. Because a typical communication system has both consistent uplink and downlink data streams with an occasional control packet, the bandwidth and latency management for buffering becomes complicated and demanding.

2 Serial RapidIO High-Speed Interconnect

Low latency, high bandwidth, and low gate count are key benefits of RapidIO technology. Serial RapidIO implementations extend the idea further to lower pin count and increased scalability.

Massive amounts of data can be transferred across RapidIO interfaces and switches effectively. Because the data path is well-scheduled and pipelined, intermediate buffering may not be required for the system if Freescale devices are interconnected using the Serial RapidIO interface, together with an efficient DMA scheme.

3 Superior DDR2 Memory Access Performance

The Freescale DDR2 memory controller has superior features and performance. When compared with any DDR2 controller implemented in an FPGA, its greatest advantage is the number of open logical banks (pages). Extensive logic would be required to support multiple open pages in an FPGA; by contrast, the Freescale DDR2 controller supports the maximum number of open pages.

In a communication system, it is vital to have multiple open memory pages to support different data streams and for secondary buffering. Page misses degrade performance greatly. In addition, the higher

operating frequency, the switch fabric, pipelining, and IP interconnection inside Freescale devices make the overall performance and sustained data transfer rates superior.

4 External DMA Reference Design

Using the Freescale memory controller with in-line data flowing through the Serial RapidIO interface is a cost-effective, high-throughput approach. To make use of the memory managed by the StarCore/PowerQUICC™ III device, the DMA can be used. However, an external processing element such as an FPGA does not have access to the memory status of the Freescale device. Therefore, an external DMA is required at the FPGA to implement the proposed approach.

A reference platform was designed and built to prove the concept and to evaluate the baseline performance of the data path.

4.1 Block Diagrams

The Altera Stratix® FPGA was selected as the reference platform. A ×1 serial lane, 1.25-Gbaud rate was used for the implementation. Multiple serial lanes with higher serial data rate can be realized without major architectural modification.

The reference design contains two main blocks: the Serial RapidIO block and the DMA engine, as shown in Figure 2.

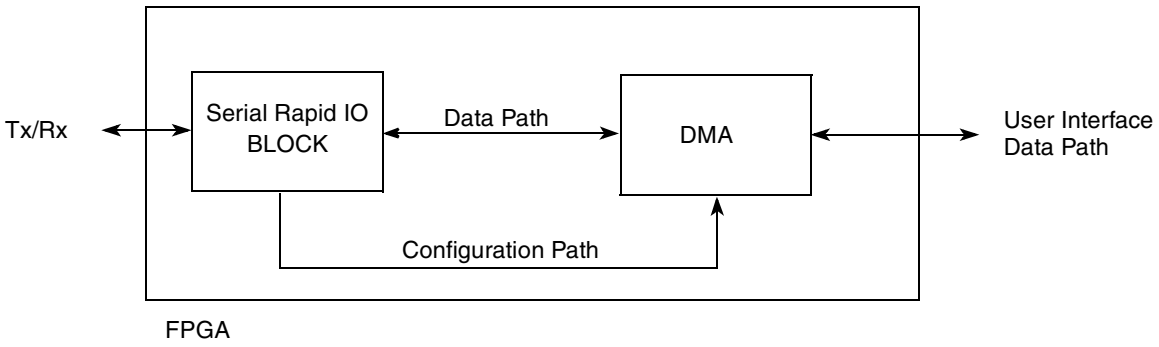

Figure 2. Reference Design Block Diagram

4.1.1 Serial RapidIO Block

The Serial RapidIO block has a transmit (Tx) connection and a receive (Rx) connection, shown in Figure 3. The internal connections consist of the I/O interface for the data path, the maintenance interface for configuration, and the doorbell interface for exceptions. All of these are in the *Avalon Interface Specifications (see* Section 7, "References.") Only the major functional groups are shown in Figure 3.

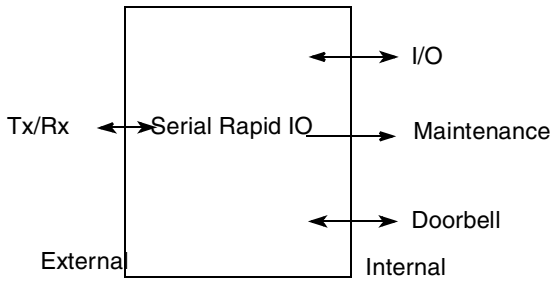

Figure 3. Serial RapidIO Functional Groups

4.1.2 The DMA Engine

The DMA engine consists of three major components: the DMA controller (DMAC), the buffer descriptor (BD), and the gasket.

The DMAC used in this design has high throughput and supports automatic Serial Rapid IO packet fragmentation. The DMAC has four physical channels, but only two were used for the downlink and uplink.

The Altera RAM block was used for BD storage. It can be accessed by the DMAC or through the configuration path by the external hosts.

The gasket interfaces the DMAC and BD with the configuration path, as shown below in Figure 4.

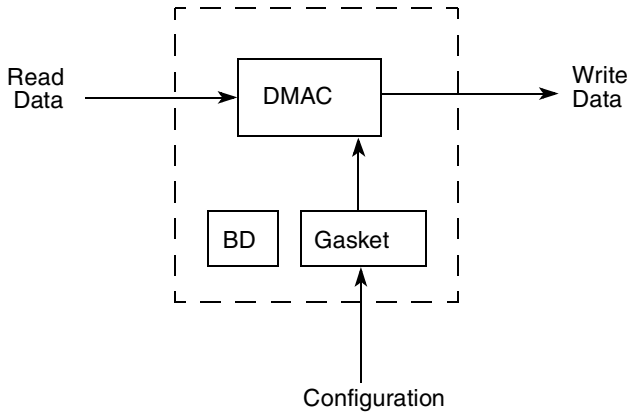

Figure 4. DMA Engine Block Diagram

4.1.3 Miscellaneous Blocks

To illustrate the overall concept more clearly, some vital blocks are not shown in the main block diagram. The following subsections describe those blocks.

4.1.3.1 The User Interface

The user interface is a FIFO-oriented interface and is implemented in the Avalon ST specification. There are two ports for source and sink operations, which can be used as downlink and uplink data streams. There is a 512-byte FIFO between the DMAC and each user's interface. Pointers are in word granularity; handshaking is carried out at the word level to maximize FIFO utilization.

4.1.3.2 Synchronization and Bus Sizing

The DMAC data bus is 64 bits wide, and the Avalon interfaces are 32 bits wide. The latter is clocked at twice the rate of the former for consistent data flow. Bus sizing is also required to interface between them. If a 4× Serial RapidIO or higher serial link speed is desired, the Avalon interface can support 64-bit-wide bus, but the synchronization technique should be modified to a simpler synchronization from the one in this design.

4.1.3.3 DMAC Data Path Arbitration

There are three request sources for the DMAC data path: BD fetch, downlink data transfer, and uplink data transfer. The logic arbitrates the DMAC data path usage.

4.1.3.4 Configuration and Doorbell

External hosts such as StarCore/PowerQUICC III configure the DMA through maintenance packets. They can configure the BDs, DMAC registers, DMA registers, or the Altera IP.

A doorbell interface is available. Users can make use of the inbound message for FPGA internal control and outbound message for interrupting external hosts.

5 Baseline Performance

At the test bench, two Altera Serial Rapid IO blocks are connected back-to-back through the Serial Rapid IO link, as shown in Figure 5.

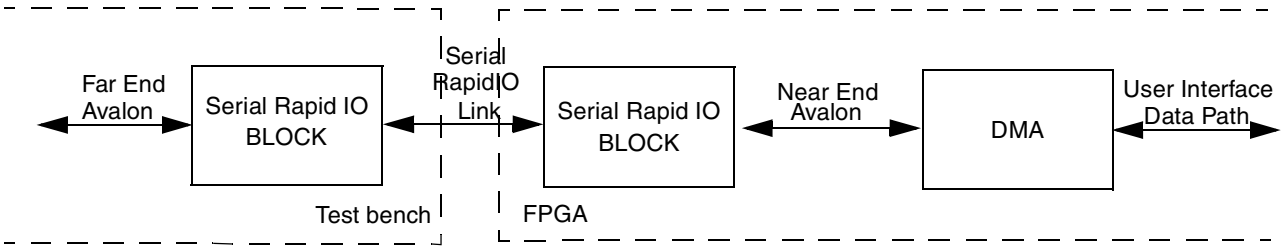

Figure 5. Test Bench Connection

5.1 Configuration One

In configuration one, 256 bytes are sent from the user interface and received at the far-end Avalon interface. For this configuration, 59 Avalon clocks are required to travel from the user interface to the near-end Avalon interface. This path includes the user interface plus the DMA controller. The latency of the Altera IP is not included.

5.2 Configuration Two

In configuration two, 256 bytes are sent from the far-end Avalon interface. For this configuration, 21 Avalon clocks are required to travel from the near-end Avalon interface to the user interface. This path includes the DMA controller plus the user interface. The latency of the Altera IP is not included. The best timing results when the user interface is always ready to accept data.

5.3 Assumptions

This measurement is taken under the most favorable conditions, when all FIFOs are empty and the far end is always ready to accept data.

6 Deliverables

For Altera, a 31.25MHz, 32-bit wide databus is used for interfacing the Altera IP and the DMA.

For Xilinx, 100MHz system clock is used for Xilinx Rocket IO. A 15.625MHz, 64-bit wide databus is used for interfacing the Xilinx IP and the DMA.

The Avalon bus clock speed is 31.25 MHz. The implementation is in Verilog HDL format; all the logic and test bench design data except the Altera IP and the DMA controller core are distributed in source code under NDA.

7 References

1. Latest RapidIO specification: http://www.rapidio.org/specs/current
2. PowerQUICC III DMA controller: Chapter 15, “DMA Controller” of the *MPC8548E PowerQUICC III Integrated Processor Family Reference Manual*
3. PowerQUICC III DDR controller: Chapter 9, “DDR Memory Controller” of the *MPC8548E PowerQUICC III Integrated Processor Family Reference Manual*
4. Altera serial RapidIO: http://www.altera.com
5. Xilinx serial RapidIO: http:www.xilinx.com

8 Revision History

Table 1 provides a revision history for this application note.

Table 1. Document Revision History

Rev. Number	Date	Editor/ Writer	Substantive Change(s)
0	04/15/2008	MW	Initial release
1.0	10/22/08	ML	Xilinx SRIO IP support.

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Freescale Semiconductor, Inc.
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Europe, Middle East, and Africa:
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Schatzbogen 7
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+46 8 52200080 (English)
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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
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+1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

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