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Application Note

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Interfacing an LCD with the MC9S08LG32

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1 Introduction

The MC9S08LG32 is a member of the Freescale HCS08 family. It uses the HCS08 core and integrated peripherals such as LCD, ADC, IIC, SPI, TPM, and RTC. This application note:

- Describes how the LCD module works for the MC9S08LG32
- Provides an example that illustrates the hardware connections and software driver for the LCD
- Explains configuration of the LCD module
- Describes use of the LCD glass with the MC9S08LG32

Figure 1 shows the block diagram for the LCD. The MC9S08LG32 contains 45 pins for LCD frontplane and backplane operation that are totally configurable. This means any pin can be configured for use with either the frontplane or the backplane.

Contents

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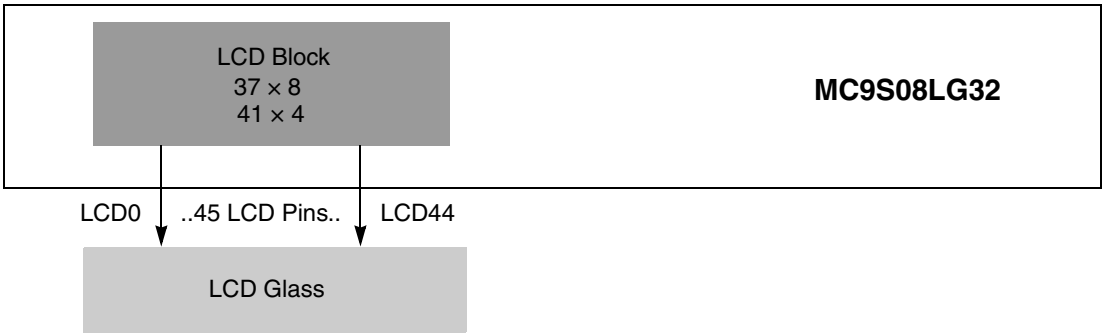

Figure 1. LCD Block Diagram

2 Hardware Interface Description

Table 1 describes the LCD pins and their directions.

Table 1. LCD Pin Description

Pins	Direction	Description
LCD[0:44]	Output	LCD data pins You can configure these pins as frontplane or backplane.
V_{LL1}	Output	LCD bias voltage
V_{LL2}	Output	LCD bias voltage
V_{LL3}	Input	LCD bias voltage See Section 5, "Options for V_{LL3}," for more details.
V_{LL3_2}	Input	Provides current enhancement at V_{LL3} **Note:** This PIN must be shorted with V_{LL3}.
V_{CAP1}	N/A	Provides storage capacitance for LCD operation on internal charge pump mode
V_{CAP2}	N/A	

2.1 Frontplane and Backplane Pin Connections

These pin connections identify the number of backplanes and frontplanes supported in the LCD glass and connect each LCD glass pin to the corresponding LCD pin at MC9S08LG32 SoC.

NOTE

In the LCD software driver configuration, you must configure as backplane the SoC LCD block pins that connect to the backplane of the LCD glass.

2.2 Voltage Pin Connections

Figure 2 and Figure 3 show the recommended connections for the voltage supply pins of the SoC LCD block. Add a capacitor on the V_{LL3} pin to filter noise from the V_{DD} input and on V_{LL1}, V_{LL2}, V_{CAP1}, and

V_{CAP2} pins for LCD operation in charge pump mode. No capacitor is required for LCD operation in resistor bias mode on V_{LL1}, V_{LL2}, V_{CAP1}, and V_{CAP2} pins.

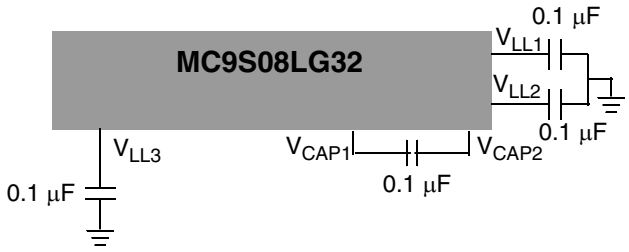

Figure 2. LCD Voltage PIN Connections for Charge Pump Mode

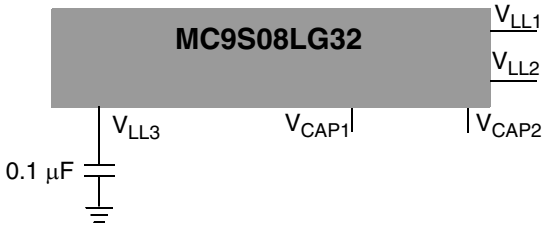

Figure 3. LCD Voltage PIN Connections for Resistor Bias Mode

2.3 Hardware Abstraction Layer

This section contains the LCD registers. These registers configure:

- Pins used for the LCD display
- Pins used as backplane or frontplane
- Pins for transferring display data to the LCD glass
- Voltage and current specifications

2.3.1 Frontplane and Backplane Configuration

2.3.1.1 LCD Pin Enable Registers

These registers specify the number of pins used for the LCD display.

		7	6	5	4	3	2	1	0
LCDPEN0	R W	PEN7	PEN6	PEN5	PEN4	PEN3	PEN2	PEN1	PEN0
	Reset	Indeterminate after reset							
LCDPEN1	R W	PEN15	PEN14	PEN13	PEN12	PEN11	PEN10	PEN9	PEN8
	Reset	Indeterminate after reset							
LCDPEN2	R W	PEN23	PEN22	PEN21	PEN20	PEN19	PEN18	PEN17	PEN16
	Reset	Indeterminate after reset							
LCDPEN3	R W	PEN31	PEN30	PEN29	PEN28	PEN27	PEN26	PEN25	PEN24
	Reset	Indeterminate after reset							
LCDPEN4	R W	PEN39	PEN38	PEN37	PEN36	PEN35	PEN34	PEN33	PEN32
	Reset	Indeterminate after reset							
LCDPEN5	R W				PEN44	PEN43	PEN42	PEN41	PEN40
	Reset	Indeterminate after reset							

Unimplemented or Reserved

Figure 4. LCDPEN Registers

Table 2. LCDPEN[0:5] Field Descriptions

Field	Description
LCDPEN[44:0]	**LCD Pin Enable** 0 LCD operation disabled 1 LCD operation enabled

2.3.1.2 Backplane Enable Registers

These registers specify the number of pins used as backplane. If the BPEN bits are cleared for a corresponding pin, then it acts as a frontplane pin.

		7	6	5	4	3	2	1	0
LCDBPEN0	R W	BPEN7	BPEN6	BPEN5	BPEN4	BPEN3	BPEN2	BPEN1	BPEN0
	Reset	Indeterminate after reset							
LCDBPEN1	R W	BPEN15	BPEN14	BPEN13	BPEN12	BPEN11	BPEN10	BPEN9	BPEN8
	Reset	Indeterminate after reset							
LCDBPEN2	R W	BPEN23	BPEN22	BPEN21	BPEN20	BPEN19	BPEN18	BPEN17	BPEN16
	Reset	Indeterminate after reset							
LCDBPEN3	R W	BPEN31	BPEN30	BPEN29	BPEN28	BPEN27	BPEN26	BPEN25	BPEN24
	Reset	Indeterminate after reset							
LCDBPEN4	R W	BPEN39	BPEN38	BPEN37	BPEN36	BPEN35	BPEN34	BPEN33	BPEN32
	Reset	Indeterminate after reset							
LCDBPEN5	R W				BPEN44	BPEN43	BPEN42	BPEN41	BPEN40
	Reset	Indeterminate after reset							

Unimplemented or Reserved

Figure 5. LCDBPEN Registers

Table 3. LCDBPEN[0:5] Field Descriptions

Field	Description
LCDBPEN[44:0]	**Backplane Enable** 0 Frontplane operation enabled 1 Backplane operation enabled

2.3.2 Control and Voltage Supply Configuration

This section describes the registers that configure the voltage and control specifications of the LCD block.

2.3.2.1 LCD Control Register 0 (LCDC0)

	7	6	5	4	3	2	1	0
R W	LCDEN	SOURCE	LCLK2	LCLK1	LCLK0	DUTY2	DUTY1	DUTY0
Reset	0	0	0	0	0	0	1	1

Figure 6. LCD Control Register 0 (LCDC0)

Table 4. LCDC0 Field Descriptions

Field	Description
7 LCDEN	**LCD Driver Enable** 0 LCD disabled 1 LCD enabled
6 SOURCE	**LCD Clock Source Select** 0 Selects the OSCOUT (external clock reference) as the LCD clock source 1 Selects the alternate clock as the LCD clock source
5:3 LCLK[2:0]	**LCD Clock Prescaler** — Used as a clock divider to generate the LCD module frame frequency.
2:0 DUTY[2:0]	**LCD Duty Select** — These bits select the duty cycle of the LCD module driver.

2.3.2.2 LCD Control Register 1 (LCDC1)

	7	6	5	4	3	2	1	0
R	LCDIEN	0	0	0	0	FCDEN	LCDWAI	LCDSTP
W								
Reset	0	0	0	0	0	0	0	0

Figure 7. LCD Control Register 1 (LCDC1)

Table 5. LCDC1 Field Descriptions

Field	Description
7 LCDIEN	**LCD Module Frame Frequency Interrupt Enable** 0 LCD interrupt disabled 1 LCD interrupt enabled
2 FCDEN	**Full Complementary Drive Enable** 0 Shared GPIOs are open drain 1 Shared GPIOs are full complementary
1 LCDWAI	**LCD Module Driver and Charge Pump Stop When in Wait Mode** 0 LCD is operating in WAIT mode 1 LCD is not operating in WAIT mode
0 LCDSTP	**LCD Module Driver and Charge Pump Stop When in Stop2 or Stop3 Mode** 0 LCD is operating in STOP modes 1 LCD is not operating in STOP modes

2.3.2.3 LCD Voltage Supply Register (LCDSUPPLY)

	7	6	5	4	3	2	1	0
R	CPSEL		LADJ1	LADJ0	0		VSUPPLY1	VSUPPLY0
W								
Reset	0	0	1	1	0	1	0	1

Unimplemented or Reserved

Figure 8. LCD Voltage Supply Register (LCDSUPPLY)

Table 6. LCDSUPPLY Field Descriptions

Field	Description
7 CPSEL	**Charge Pump or Resistor Bias Select** 0 Resister bias selected 1 Charge pump selected
5:4 LADJ[1: 0]	**LCD Module Load Adjust** For CPSEL = 1 Adjust the clock source for the charge pump 00 — Fastest clock source for charge pump (LCD glass capacitance 8000 pF or lower) 01 — Intermediate clock source for charge pump (LCD glass capacitance 6000 pF or lower)) 10 — Intermediate clock source for charge pump (LCD glass capacitance 4000 pF or lower) 11 — Slowest clock source for charge pump (LCD glass capacitance 2000 pF or lower) For CPSEL = 0 Adjust the resistor bias network for different LCD glass capacitance 00 — Low load (LCD glass capacitance 2000 pf or lower) 01 — Low load (LCD glass capacitance 2000 pf or lower) 10 — High load (LCD glass capacitance 8000 pf or lower) 11 — High load (LCD glass capacitance 8000 pf or lower)
1:0 VSUPPLY[1:0]	**Voltage Supply Control** 01 — Drive V_{LL3} internally 11 — Drive V_{LL3} externally Others — Reserved

2.3.3 Data Waveform Registers

2.3.3.1 LCD Waveform Registers (LCDWF[63:0])

		7	6	5	4	3	2	1	0
LCDWF0	R W	BPHLCD	BPGLCD	BPFLCD	BPELCD	BPDLCD	BPCLCD	BPBLCD	BPALCD
	Reset	Indeterminate after reset							

Figure 9. LCDWF Registers

Table 7. LCDWF Field Descriptions

Field	Description
BP[x]LCD[y] x — A:H y — 0:44	**Segment on frontplane operation** — If the LCD[y] pin is enabled and configured to operate as a frontplane pin, these bits control the on or off state for the LCD segment connected between LCD[y] and BP[x]. 0 LCD segment off 1 LCD segment on **Segment on backplane operation** — If the LCD[y] pin is enabled and configured to operate as a backplane pin, these bits control the phase (A-H) in which the LCD[y] pin is active. 0 LCD BP[x] inactive for LCD[y] 1 LCD BP[x] active for LCD[y]

2.4 LCD Operating Modes

Figure 10 shows the internal circuitry for controlling the modes of operation for LCD block.The switches shown control all modes of bias voltage generation.

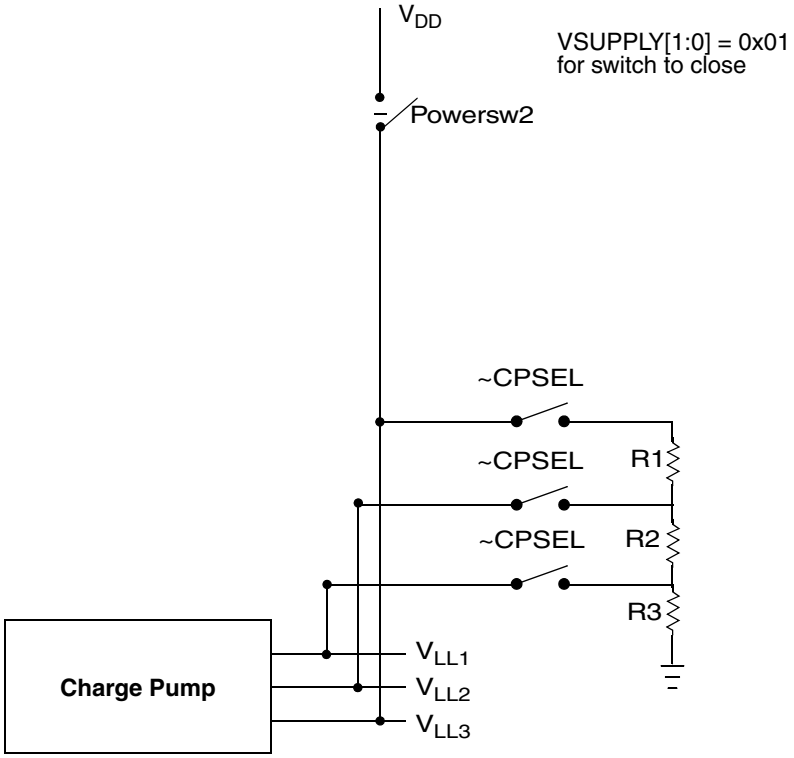

Figure 10. Generation of Bias Voltage in Different Modes

Table 8 describes all possible configurations for charge pump/resistor network mode selection.

Table 8. LCD Operating Modes

VSUPPLY[1:0]	CPSEL	Configuration
01	0	Drive V_{LL3} internally from V_{DD} and V_{LL1}. Drive V_{LL2} from resistor bias.
11	0	Drive V_{LL3} externally from V_{DD} and V_{LL1}. Drive V_{LL2} from resistor bias.
01	1	Drive V_{LL3} internally from V_{DD} and V_{LL1}. Drive V_{LL2} from charge pump.
11	1	Drive V_{LL3} externally from V_{DD} and V_{LL1}. Drive V_{LL2} from charge pump.

2.4.1 Resistor Bias (R-Bias) Mode

In this mode, the bias voltages, V_{LL1} and V_{LL2}, are generated by an internal resistor bias circuit. In this mode, you can provide V_{LL3} or drive it internally from V_{DD}. The internal bias network has multiple drive variants (see Table 9). See Table 10 to configure register bias mode.

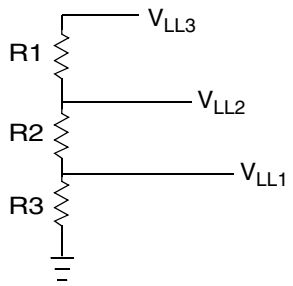

Figure 11. Bias Voltage in Resistor Bias Mode (R1 = R2 = R3)

Table 9. Drive Variants in Internal Register Bias

	LADJ[1:0]	Description
Low Drive	0X	Up to 992 kW resistor ladder (three 992 kW resistors)
High Drive	1X	Up to 92 kW resistor ladder (three 92 kW resistors)

Table 10. Resistor Bias Mode Configuration

	Value	
Register Bit(s)	**V_{LL3} Internally**	**V_{LL3} Externally**
LCDSUPPLY_CPSEL	0	0
LCDSUPPLY_VSUPPLY[1:0]	01	11

2.4.2 Charge Pump Mode

In this mode, the bias voltages V_{LL1} and V_{LL2} are generated using an internal charge pump. For the charge pump to work properly, storage capacitors (0.1 µF) are required on V_{LL1}, V_{LL2}, V_{CAP1}, and V_{CAP2} external pins. See Section 2.2, "Voltage Pin Connections," for details. In this mode, you can provide V_{LL3} externally or derive it internally from V_{DD} based on the configuration.

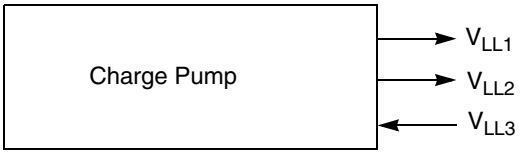

Figure 12. Bias Voltages in Charge Pump Mode

Table 11. Charge Pump Mode Register Configuration

	Value	
Register Bit(s)	**V_{LL3} Internally**	**V_{LL3} Externally**
LCDSUPPLY_CPSEL	1	1
LCDSUPPLY_VSUPPLY[1:0]	01	11

3 Software Interface Description

This section describes the external APIs available. These APIs use the LCD block functionality in the software driver.

Table 12. Software Interfaces

Interface	Description
lcd_Init	Provides LCD initial configuration based on flags that you define.
lcd_PrintString	Takes a string as input and displays it on the alphanumeric character space on the LCD, starting from first alphanumeric character.
lcd_PrintStringPos	Takes a string as input and displays it on the alphanumeric character space on the LCD, starting from alphanumeric character as per the argument passed as pos.
lcd_SlideString	Takes a string as input and displays it on the alphanumeric character space on the LCD, sliding the string from right-most digit to the left-most digit.
lcd_DispHexVal	Takes a number as input and displays it in hexadecimal format on the alphanumeric character space on the LCD, starting from alphanumeric character passed as startloc.
lcd_DispDecVal	Takes a float number as input and displays it in decimal base format on the alphanumeric character space on the LCD, starting from alphanumeric character passed as startloc.
lcd_DispVal	Takes an integer number as input and displays it in decimal base format on the alphanumeric character space on the LCD, starting from alphanumeric digit passed as startloc.
lcd_StopBlinking	Turns off the blinking feature of the LCD on the current display.
lcd_SetAltDisplay	Turns on the alternate blinking mode with the display switching between the two strings that were passed as arguments.
lcd_Clear	Clears all the LCD segments.
lcd_ActivateBlink	Activates LCD blink functionality for the current LCD display.
lcd_TestSpecialChars	A test routine for all the special characters supported in LCD.

3.1 Interfacing LCD Glass with MC9S08LG32

This section describes an example of interfacing the LCD glass (40 × 4) with the MC9S08LG32 in auto applications. The LCD block of the SoC is configured in resistor bias mode, and uses the external voltage supply on the V_{LL3} pin for LCD supply as well as external contrast control. Figure 13 shows the hardware connections for this example.

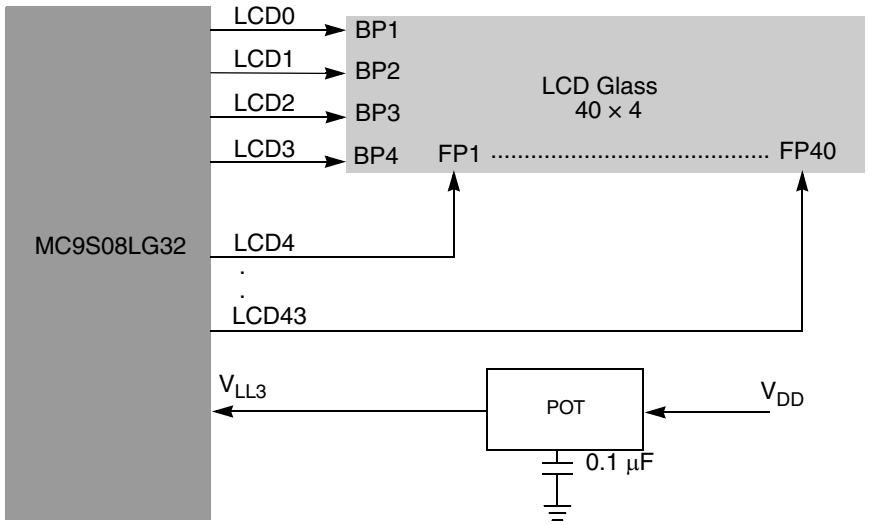

Figure 13. Example of Hardware Connections for Interfacing LCD Glass with MC9S08LG32

3.2 Register Configuration

Table 13 shows the control, voltage supply pins, and waveform data register configurations for operating the LCD glass in 40 × 4 mode:

Table 13. LCD Register Configurations for 40 × 4 Mode

Register	Value	Configuration Description
LCDC0	0x83	Source clock from external oscillator LCLK — Clock divider is 0 DUTY — Duty cycle is 3 (because mode is 4×)
LCDC1	0x00	LCD Interrupt — Off LCD interrupt — On in wait and stop modes
LCDVSUPPLY	0x33	CPSEL — Charge pump off LADJ[1:0] — 0x3 high drive (see Table 9) VSUPPLY — V_{LL3} externally supplied
LCDPEN0	0xFF	Use 44 SoC pins for LCD operation.
LCDPEN1	0xFF	
LCDPEN2	0xFF	
LCDPEN3	0xFF	
LCDPEN4	0xFF	
LCDPEN5	0x0F	

Table 13. LCD Register Configurations for 40 × 4 Mode (continued)

Register	Value	Configuration Description
LCDBPEN0	0x0F	Use LCD[0:3] as backplane and all other LCD pins (LCD[4:43]) as frontplane.
LCDBPEN1	0x00	
LCDBPEN2	0x00	
LCDBPEN3	0x00	
LCDBPEN4	0x00	
LCDBPEN5	0x00	
LCDWF[0:43]	0x00	Initialize the waveform registers. These registers contain the data for the LCD display.

NOTE

You must configure all registers as described in Table 13 before enabling LCD (setting the LCDC0_LCDEN bit).

4 Initialization Procedure

Obey the instructions below to configure the LCD block of the SoC to operate with an LCD glass, and to operate in resistor bias mode with external voltage supply on the V_{LL3} pin and external contrast control.

1. Disable clock gating for the LCD module.
   SCGC2_LCD = 1
2. Write LCDC0 register bits to configure the LCD module to use the clock from an external oscillator and to use clock divider and the duty cycle (number of backplanes – 1).
   LCDC0 = 0x03
3. Write LCDC1 register bits to configure LCD interrupt as off and to make LCD functional in wait and stop low-power modes.
   LCDC1 = 0x00
4. Write in LCD supply register (LCDCSUPPLY) to configure resistor bias mode operation and external voltage application on V_{LL3} pin.
   LCDSUPPLY = 0x33
5. Configure the number of pins to be used for LCD operation (44 SOC pins in LCDPEN register).
6. Configure the backplane pins — LCD[0:3] as backplane and all other LCD pins as frontplane in LCDBPEN register.
   LCDBPEN = 0x0F
7. Clear the LCDWF register to avoid the display of unwanted data on the LCD.
8. Enable the LCD module in the SoC by setting the LCDC0_LCDEN bit.
   LCDC0 = 0x83

4.1 Operating Modes Summary

Table 14 summarizes the operating modes, associated hardware connections, and register configurations for the LCD block of MC9S08LG32:

Table 14. LCD Operating Modes Summary

Operating Temperature Range	Current Consumption (mA)	Operating Mode	Hardware Connections	Register Configurations	Applications
–40 °C to 85 °C	X (Lower current consumption)	Charge Pump	Supply 0.1μF capacitor for charge storage on V_{LL1}, V_{LL2}, V_{CAP1}, and V_{CAP2}	LCDSUPPLY_CPSEL = 1 LCDSUPPLY_LADJ = 0x3	Consumer appliances like washing machine, microwave, etc.
–40 °C to 105 °C	X + (20 μA)	Register Bias	No capacitor needed	LCDSUPPLY_CPSEL = 0 LCDSUPPLY_LADJ = 0x3	Automotive applications like auto cluster, HVAC, etc.

5 Options for V_{LL3}

Table 15 describes the configurations for V_{LL3} in MC9S08LG32.

NOTE

V_{LL3} and V_{DD} if different at power ramp, will cause current leakage.

Table 15. V_{LL3} Configurations for LCD

Configuration	Conditions
V_{LL3} connected to external supply	This configuration applies if you: • Use any of the 45 LCD pins as a full complementary digital GPIO. • Vary V_{DD} through board regulator to enable> the LCD contrast control feature. • Select register bias mode or charge pump operating mode.
V_{LL3} connected to V_{DD} internally	This configuration applies if you: • Use any of the 45 LCD pins as a full complementary digital GPIO. GPIOs toggling as outputs must be configured as open drain. You can use digital input functions for these GPIOs. • Vary V_{DD} through board regulator to enable the LCD contrast control feature. • Select register bias mode or charge pump operating mode.
V_{LL3} connected to an external independent source through potentiometer network	This configuration applies if you: • Use all 45 pins as LCD pins. You can also use digital input functions for GPIOs. • Vary V_{DD} through the external potentiometer to control the LCD contrast. • Charge pump mode is preferred in this scenario. If using register bias mode, you must ensure that the potentiometer resistance is less than the register bias network values selected by setting LCDSUPPLY_LADJ bits. This is required to avoid a drop in V_{LL3} if internal register bias is activated.

6 References

See S08LG Product Summary Page for more information and the documents released for MC9S08LG32.

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