

Using GCR4 to Adjust Ethernet Timing in MSC8144 DSPs

This application note assists board designers to implement Ethernet interfaces in systems using MSC8144 DSP devices. In addition to configuring the MSC8144 DSP for the specific interface and processing configuration (MII, RMII, SMII, RGMII, or SGMII mode; packet filtering; RISC utilization; and line speed), the designer must also meet the specified signal delay for the protocol.

The reader should note that this application note does not apply to SGMII; SGMII uses the separate SerDes interface.

For demonstration purposes, this application note focuses on the Reduced Gigabit Media Independent Interface (RGMII). The application note does not reproduce the entire interface specification, but focuses on timing and delay specifications. As such, the readers must research and develop a general understanding of the general principles of RGMII and the other interfaces for proper system design implementation.

NOTE

MSC8144 includes MSC8144, MSC8144E, and MSC8144EC DSP devices.

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1 Ethernet Timing Related Specifications

The functionality provided by General Configuration Register 4 (GCR4) enables the MSC8144 to meet timing specifications related to clock and signal delay and skew as they are written in the standards for MII, RMII, SMII, and RGMII. As noted in the introduction, this note focuses on RGMII, so for further information on the other standards as they relate to the MSC8144, refer to the MSC8144 Technical Data Sheet and the relevant specifications listed below:

- a) **MII** is described in the **IEEE**[®] 802.3[®] Standard for Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications.
- b) **RMII** is described in the specification found at http://www.national.com/appinfo/networks/files/rmii_1_2.pdf
- c) **SMII** is described in the specification found at http://www.angelfire.com/electronic2/sharads/protocols/MII_Protocols/smii.pdf

2 RGMII

As an alternative to the **IEEE** 802.3z[™] (GMII) Ethernet standard that discuss general Ethernet interfacing, the RGMII Specification Reduced Pin-count Interface for Gigabit Ethernet Physical Layer Devices provides a method for Gigabit throughput while saving pins/board space. The RGMII Specification is managed by Broadcom, Marvell, and Hewlett-Packard, and is available on the Hewlett-Packard website at:

http://www.hp.com/rnd/pdfs/RGMIIV2_0_final_hp.pdf

To maintain Gigabit speed while reducing the number of data signals in half, the RGMII specification makes use of both the positive and negative edges of the clock. Because of this, meeting the RGMII specification requires careful attention to timing and delays.

2.1 RGMII Specified Delays

The RGMII specification explicitly states how to manage output and input data-clock skew from an Ethernet Controller MAC to a Physical Ethernet Interface (PHY) as described in the following subsections.

2.1.1 Connecting to PHY Interfaces (non-MAC)

Clock and data signals are generated simultaneously by the source in this system. In such a system, there are two scenarios: transmitting and receiving data. Figure 1 shows the timing for the two scenarios.

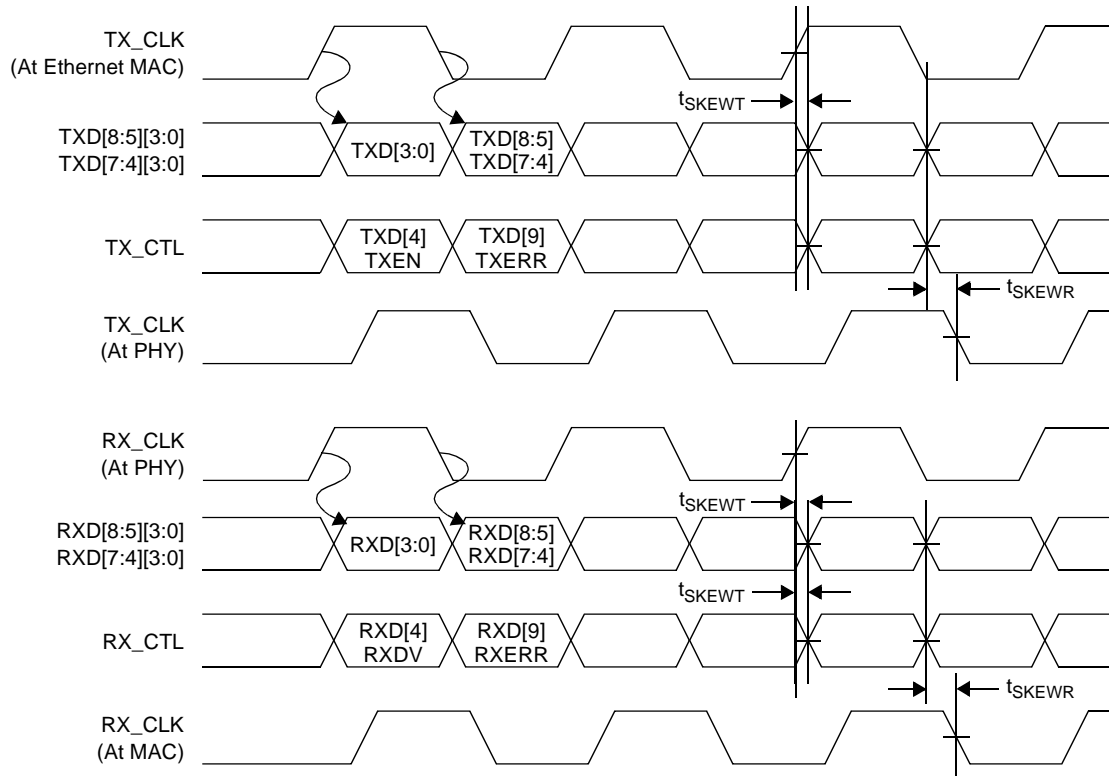


Figure 1. RGMII AC Timing

2.1.1.1 MAC to PHY (Transmit)

In the *transmit case*, the Ethernet MAC transmits data to the Ethernet PHY. The Ethernet MAC sends data with t_{skewT} (the timing of TXC at the MAC) that meets the RGMII specification.

$t_{skewT} = -500 \text{ ps to } +500 \text{ ps}$ skew window for Transmitter to drive data

According to the RGMII standard, clocks must be routed such that an additional trace delay of greater than 1.5 ns and less than 2 ns is added to the associated clock signal. To meet this standard without adding trace delays, most of the PHYs in the industry and the MSC8144 already include delay logic that can compensate this need for such on-board delay. Therefore, this type of PHY can manage a t_{skewR} of $\pm 500 \text{ ps}$ (the skew for TXC data sampling seen inside the PHY).

The PHY or the on-board delay must delay the clock signal by 1.5 to 2.0 ns so that $tskewR$ is sampled at 1.0 to 2.6 ns. Figure 2 indicates where the delays must occur.

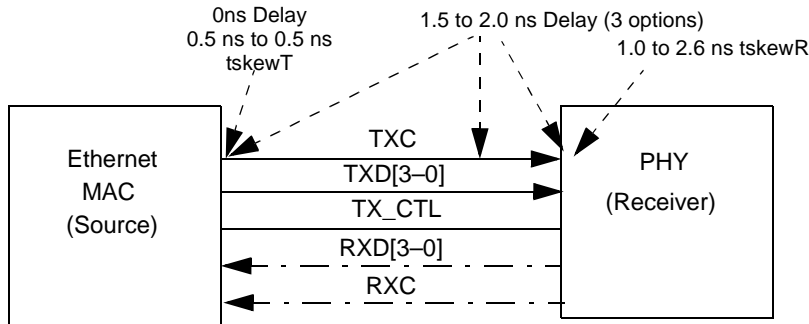


Figure 2. MAC to PHY Delay Diagram (Transmitting Data)

2.1.1.2 PHY to MAC

In the *receive case*, the Ethernet MAC receives data from the Ethernet PHY. Just as in the *transmit case*, trace delay of greater than 1.5 ns and less than 2 ns must be added to the associated clock signal, as required by the RGMII specification. Also similar to the transmit case, most of the PHYs in the industry and the MSC8144 already include delay logic that can compensate this need for the RXC clock as well.

As shown in Figure 3, the MAC, trace, or the PHY can be used to generate the required 1.5–2.0 ns delay to RXC and 1.0–2.6 ns $tskewR$. The methods to add delay are defined in detail in Section 2.2, *On-Board Delay Model (Standard Model)* and Section 2.3, *No On-Board Delay Model*.

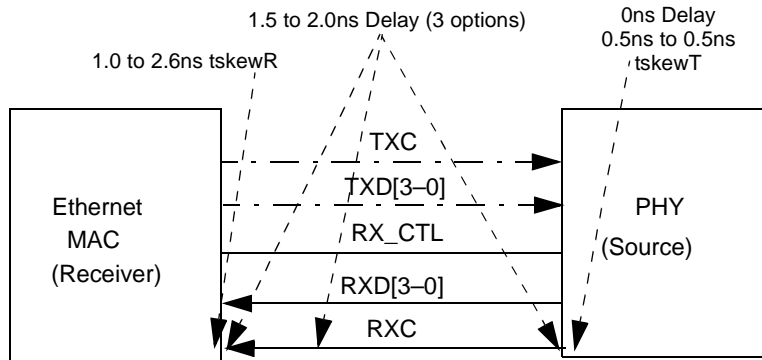


Figure 3. PHY to MAC Delay Diagram (Receiving Data)

2.1.2 For MAC2MAC/Switch Interfaces (non Specified)

Because an Ethernet switch is simply a means to connect the Ethernet controller to another endpoint, such as another controller, MAC2MAC interfaces are not specifically described in the RGMII specification. Because of this, it is the responsibility of the board designer either to design a board using a switch that can mimic the timing implemented by an RGMII PHY, or, to ensure that the switch and other Ethernet ICs connecting to the switch have compatible timing.

Take the case of a DSP Ethernet MAC and a Switch; they could be connected as shown in [Figure 4](#).

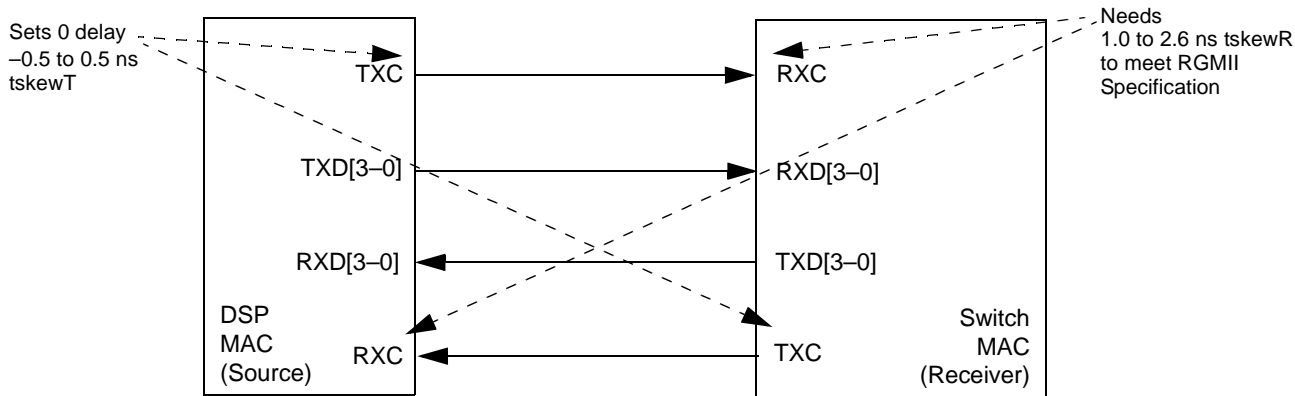


Figure 4. DSP MAC to Ethernet Switch Connection

The situation shown in [Figure 4](#), like the MAC-PHY interface, has a two modes of managing the requirement for delay and skew. These modes are defined in the following sections: [Section 2.2, On-Board Delay Model \(Standard Model\)](#) and [Section 2.3, No On-Board Delay Model](#).

2.2 On-Board Delay Model (Standard Model)

In the on-board delay model, as defined from the perspective of an Ethernet device (the DSP in this case) the Ethernet MAC assumes all timing delay is generated externally to the device (at the board level). In this case, the MAC is only required to meet the requirements of the RGMII specification, as far as timing is concerned. The designer has the choice of placing delays on the board or in the PHY.

If we take [Figure 4](#) as an example, how can the designer use the on-board delay model to meet timing requirements? The solution is: the board designer must either set up on-board delays to make this true, or use the timing registers in the Ethernet switch/PHY to add delays of 1.5–2.0 ns and tskewR of 1.0–2.6 ns to the switch TX signals to mimic a PHY (as per [Figure 5](#))

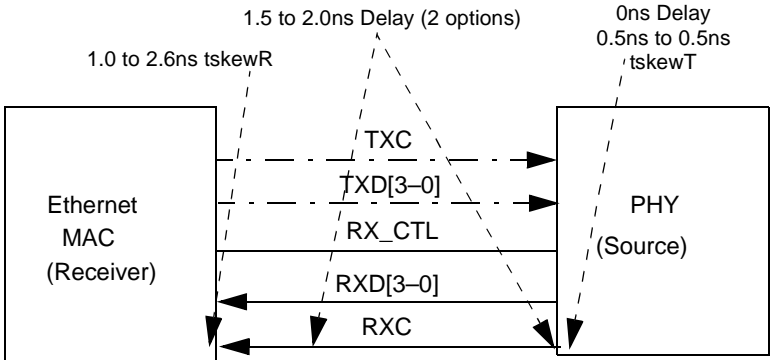


Figure 5. On-Board Delay Model

2.3 No On-Board Delay Model

The no-on-board delay model is the opposite of the on-board delay model. From the perspective of the device in question (the DSP in this case), timing does not meet the RGMII specification. This occurs if the Ethernet switch does not have internal timing registers that can be adjusted to allow it to mimic the timing seen by devices connected to a PHY. In this case, the DSP does not receive signals on RXC at 1.5–2.0 ns delay to the RX Clock, and $tskewR$ is out of specification. If the Switch MAC in Figure 6 does not provide internal skew management, this causes timing issues. In some cases (such as the MSC8144), the DSP MAC can be used to insert a skew so that $tskewR$ as seen by the Switch still meets the RGMII Specified skew as described in Figure 1.

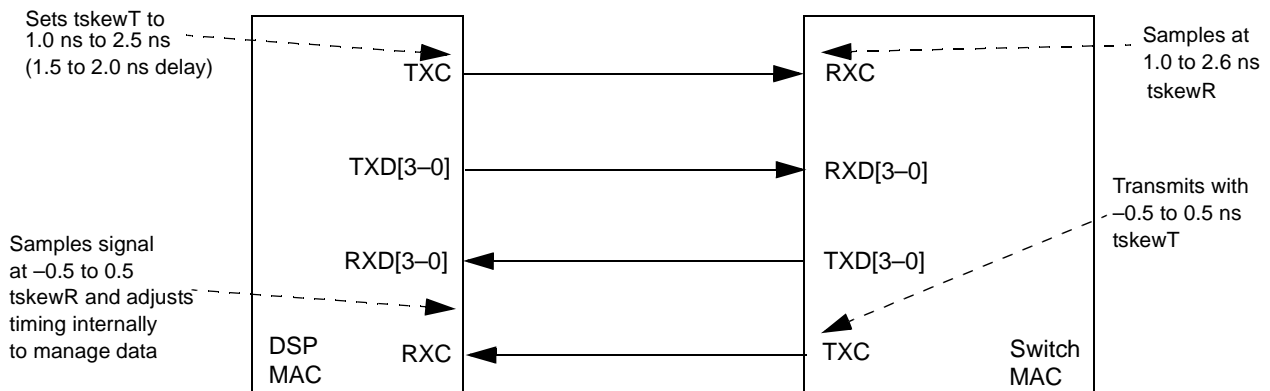


Figure 6. DSP MAC to Ethernet Switch Connection (no On-Board Delay Seen by DSP)

The MSC8144 has the ability to adjust timing using the GCR4, enabling it to connect directly to other Ethernet MACs that lack such configurability. This is discussed in detail in Section 3, *MSC8144 Ethernet MAC*.

3 MSC8144 Ethernet MAC

The MSC8144 Ethernet MAC is designed to be compliant with the various Ethernet interface standards by using the assistance of a TAP controller configured by GCR4 for fine tuning of delay and skew of the Ethernet signals. The interfaces supported by the MSC8144 include MII, RMII, SMII, RGMII, and SGMII. SGMII is connected through the SerDes port and does not require GCR4 configuration. Standard interface timing and related GCR4 settings are all listed in the AC Timings chapter of the MSC8144 Technical Data Sheet, and the related specifications are identified in Section 1, *Ethernet Timing Related Specifications* of this document.

The MSC8144 is characterized to meet RGMII Ethernet timing for two scenarios.

- The first scenario that the MSC8144 meets is described in Section 3.1, *Connecting the MSC8144 Device to an RGMII Ethernet PHY*.
- The second scenario that the MSC8144 meets is described in Section 3.2, *Connecting the MSC8144 to an MAC Device*.

3.1 Connecting the MSC8144 Device to an RGMII Ethernet PHY

The MSC8144 device is designed to meet the RGMII specification by using GCR4 to fine-tune the tskewR skews as seen by the MSC8144 Ethernet MAC. As discussed in [Section 2.2, On-Board Delay Model \(Standard Model\)](#), this is called the “On-Board Delay Model.” The two modes have their own delays:

- For transmitting data, the MSC8144 generates TXC and TXD signals with -0.5 to 0.5 ns tskewT as per the specification.

NOTE

The PHY/Switch must be able to generate internal delays to meet skew requirements or the board designer must add board trace delays.

- For receiving data, the MSC8144 expects clock and data with a 1.5 – 2.0 ns delay and 1.0 – 2.6 ns tskewR at the MSC8144 MAC. This can be done using on board trace delays (as per the RGMII standard) or by using clock/data delay configuration within the PHY.

Figure 7 shows the interconnection diagram and timing using a PHY to generate delays for the MAC8144 RXC:

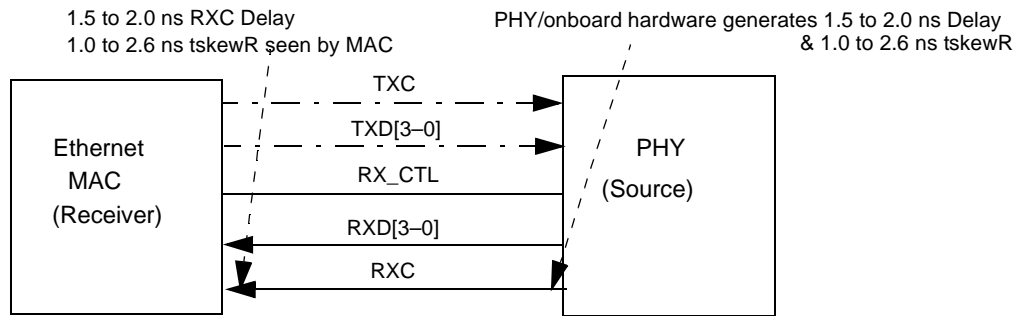


Figure 7. PHY to MSC8144 MAC Delay Diagram (Receiving Data)

Therefore, the AC timing for the MSC8144MAC to PHY connection is as shown in [Figure 8](#).

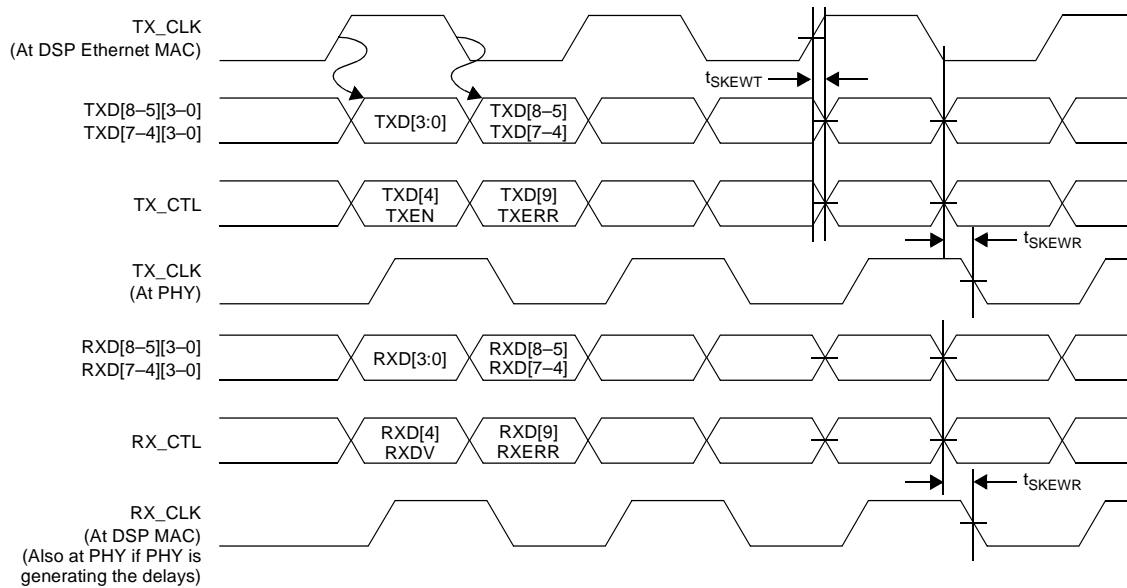


Figure 8. MSC8144 RGMII AC Timing

For the first scenario, the MSC8144 is characterized to meet the above AC timing (t_{skewR} @ 1.0–2.6 ns and t_{skewT} @ 0ns) using the following GCR4 setting:

GCR4 = 0x00001004

(As specified in the MSC8144 Technical Data Sheet).

This sets a single delay unit on the MSC8144 RX data pins for both Ethernet Controllers in order to meet 1.0 to 2.5 ns t_{skewR} .

3.2 Connecting the MSC8144 to an MAC Device

Connecting an MSC8144 MAC to an Ethernet switch (or other MAC device) may require external delay management as discussed in [Section 2.3, “No On-Board Delay Model.”](#) This is the case when connecting to a Switch that does not have sufficient AC timing tuning capabilities and expects to receive clock and data as per the RGMII Specification. This scenario is described graphically in [Figure 6](#).

For this second scenario, the MSC8144 is characterized to meet the above AC timing using the following setting for the GCR4 register:

GCR4 = 0x0004C130,

(As specified in the MSC8144 Technical Data Sheet).

By setting the GCR4 to 0x0004C130, the MSC8144 is set up to accommodate other Ethernet MAC devices by generating all RGMII required delays internally. This setup all assumes the switch (IC, and so on) sends data to the DSP with a skew between –0.5 and 0.5 ns, and the switch expects the to receive data with a skew of 1.0 to 2.6 ns. If the switch cannot meet these numbers, or the t_{skewT} and t_{skewR} must be changed, custom GCR4 tuning is required. [Section 4.2, Three-Step Process for GCR4 Fine Tuning](#) provides guidelines to achieve a custom value.

3.3 How to Determine Whether a Device Can Work with the MSC8144 Ethernet Controller

Very simply, Ethernet device specifications should include information regarding AC timing and registers that control clock skew and delay. Determine whether the switch registers can generate a clock delay to mimic an RGMII compatible PHY in the On-Board Delay case, as shown in [Figure 1](#), or operate in the No On-Board Delay timing, as described in [Figure 6](#). From this information, you can determine whether the device can be used with the GCR4 settings that are already characterized in the MSC8144 Technical Data Sheet. Additionally, you must consider the inherent board level timing and delays in your design. In the event that a specific Ethernet setup meets neither the On-Board Delay model, nor the No On-Board Delay model described in this document (and the specifications listed in the MSC8144 Technical Data Sheet), GCR4 tuning can be used to enable proper functionality.

4 GCR4 Tuning

If a MSC8144 DSP is connected on a board that fails to meet the specified timing in the MSC8144 Data Sheet (shown in either [Figure 1](#) for RGMII Standard operation, or [Figure 6](#) for non-standard operation), GCR4 requires fine tuning.

4.1 GCR4 Delay Values

GCR4 tunes TAP delays for input and output clocks, control, and data for both Ethernet controllers. Each delay unit is variable based upon device process, but falls within the limits listed in [Table 1](#):

Table 1. GCR4 Delay Unit Timing

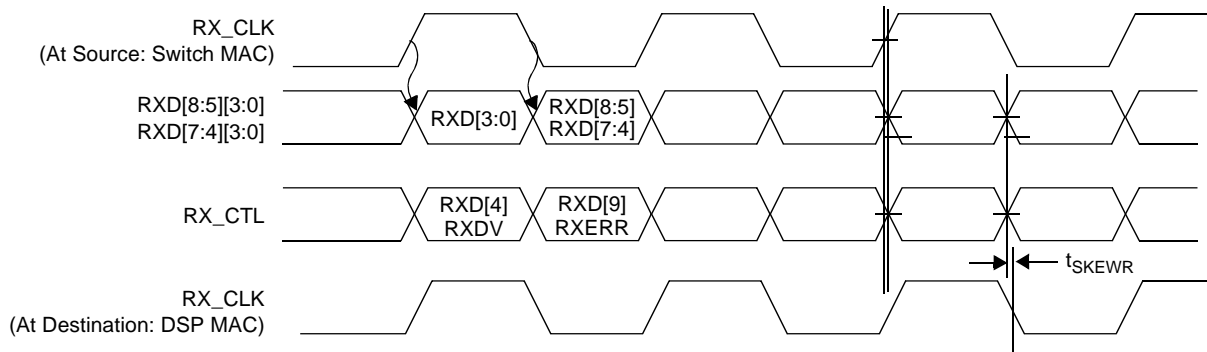
GCR4	Min	Typ	Max	Units
Delay Unit	0.5	—	1.0	ns

4.2 Three-Step Process for GCR4 Fine Tuning

We will assume the case that a specific switch setup cannot achieve the required timing shown in [Figure 6](#), and requires configuration of GCR4 to manage the timing of the MSC8144-to-Switch interface. The procedure walks through an example setup and provides timing numbers along with the final resulting GCR4 configuration.

4.2.1 Characterize the “No On-Board Delay” Timing

Characterize the interface timing by measuring the receive skew as close as possible to the pins on the MSC8144. TskewR (and TskewT) should be measured using the associated clock signal and control signals (TX_CTL or RX_CTL). Probing CTL signals (instead of data) provides the cleanest signal to determine skew. In this case, the RX_CLK to RXD&RX_CTL skew (TskewR) seen by the MSC8144 should be within -0.5 ns to 0.5 ns.



Note: Valid control is sampled on the positive edge of the clock.

Figure 9. No On-Board Delay: MSC8144 Receiving Data from Switch

The designer also needs to measure TX skew from the MSC8144 at the Switch/PHY to determine whether the timing seen by the Switch/PHY is within that device specification.

Step 1. Characterizing the Delay Timing

For the case of our example, a board designer has a setup with a new board using an MSC8144. The MSC8144 connects to a switch that does not have configurable timing settings. So the switch expects to be connected to a standard RGMII interface that provides all timing delays. Therefore, we have the scenario shown in Figure 6, for which the DSP is expected to send clock and data at 1.5-2.0ns skew so the signals at the switch meet standard tskewR (that is, the No On-board Delay case).

The designer probes the switch and finds that the timing using the Data Sheets GCR4 value leads to the following:

TX_CLK to TX_CTL max skew = 2.8 ns (this is larger than the maximum allowable 2.6ns)

4.2.2 Calculate the Required Delta from Characterized Timing Parameters

With GCR4 programmed for On-board/No On-board delay case, measure how far away timing is from the required timing shown in Figure 8 or Figure 6 of this note and shown in the Data Sheet. For the case of the example in Figure 6, which we are using as the basis for our example, the GCR4 would be programmed as

GCR4 = 0x0004C130.

From the definition of GCR4 in the Reference Manual, we know that for each Ethernet controller, this configures:

- Ethernet 2 (UCC3)
 - 1 TAP delay for RCLK
 - 3 TAP delays for output clock
- Ethernet 1 (UCC1)
 - 1 TAP delay for RCLK
 - 3 TAP delays for output clock

The above delays are based on the skew/delay measured at the switch pins.

Step 2. Adjusting GCR4

Because we measured a skew too large on the TX signals from the MSC8144, we must decrease the delay of the TX_CLK (called “Clock Out Delay” in the MSC8144 RM). Since the measured skew was 2.5 ns, decreasing by 1 delay unit (0.5–1.0 ns) brings skew to within spec.

To put the TX_CLK skew within spec for the switch

- Ethernet 2 (UCC3)
 - 1 TAP delay for RCLK
 - 2 TAP delays for output clock
 - Ethernet 1 (UCC1)
 - 1 TAP delay for RCLK
 - 2 TAP delays for output clock
-

4.2.3 Test and Verify

The final step is to repeat the measurements done in [Section 4.2.1, Characterize the “No On-Board Delay” Timing](#) to verify that the GCR4 change yields the required delay.

Step 3. Finalizing the GCR4 Settings

- If AC timing does not meet the required specifications, add or subtract additional delay units and verify until the specified timing is met.
 - If AC timing is within specification, save the GCR4 settings for this board. At this point, the MSC8144 Ethernet is ready for sending and receiving data and the user can connect the board to other Ethernet hosts.
-

5 Other Protocols

This application note uses the RGMII protocol as an example of how to adjust the Ethernet clock and delay timing using the MSC8144 DSP GCR4. For other protocols, refer to the referenced standards and use the default values for GCR4 defined in the MSC8144 Technical Data Sheet. For non-PHY interfaces, such as switches, use the timing defined by the required protocol and adjust the recommended GCR4 settings for that protocol using the general procedures defined in [Section 4, GCR4 Tuning](#) of this document.

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