

Nexus Interface Connector for the MPC567xF and MPC5676R Families

Including the Samtec ERF8 Connector Definition

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1 Introduction

The MPC567xF¹ microcontroller is the first device in the MPC5600 family that uses a 16-bit wide Message Data Output port along with multiple Nexus clients that communicate over a single IEEE-ISTO 5001™ Nexus Combined JTAG IEEE 1149.1/Auxiliary Out interface. It is also the first automotive device that supports the IEEE-ISTO 5001™-2011² revision of the Nexus standard. In addition to adding support for a high speed serial auxiliary port (currently not supported on the MPC5600 family) and minor changes to some of the trace messages, the 2011 revision of the standard defines a class of connectors that support high-speed trace (serial and parallel). The MPC5674xF supports only the parallel trace option. This application note addresses all of the connector options and recommendations for the MPC567xF and the MPC5676R³ devices. This includes the new high-speed parallel trace Samtec ERF8 connector, as well as the MICTOR-38 connector for backwards tool compatibility. A simple JTAG connector definition is included for reference as well.

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1. MPC567xF refers to both the MPC5673F (3 MB Flash and 192 KB SRAM and the MPC5674F (4 MB Flash and 256 KB SRAM).
2. Currently, the IEEE-ISTO 5001™-2011 standard is expected to be released in 2011.
3. This document also references the MPC5676R as the MPC567xR to cover possible future devices.

2 MPC5600 Nexus architectural overview

The MPC5600 devices implement a varying number of internal Nexus clients. Collectively, all of the JTAG and Nexus clients are known as the Nexus Development Interface (NDI). The typical interconnections between the different Nexus clients are shown in the following figure. Tools can communicate with each of these clients by selecting the client through the JTAG Controller (JTAGC) and the Nexus Port Controller (NPC).

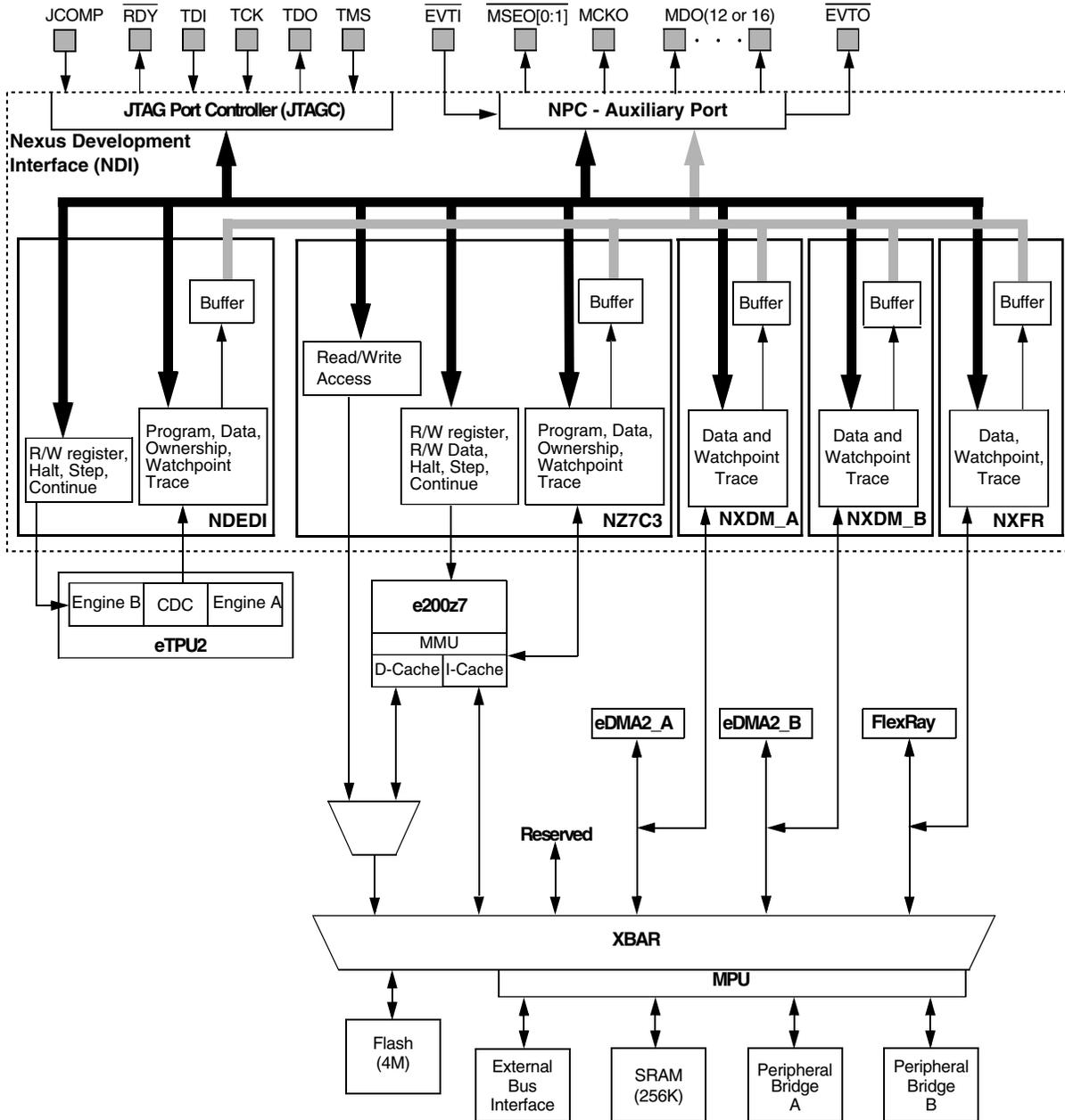


Figure 1. Typical MPC5600 Nexus development interface (MPC567xF shown)

The Nexus clients can consist of many types, but the typical clients are:

- e200x core — In the MPC5600 devices, the primary processing cores are based on Power Architecture®. Current available e200x cores are the e200z0, e200z1, e200z3, e200z4, e200z6, e200z6 with VLE, and the e200z7. Some devices implement multiple cores, some as true dual (homogeneous) cores, and some as a primary core and a secondary

core. The secondary core is a smaller core intended for off-loading the primary core. The Nexus client is usually named for the core that it supports plus the Nexus class that the client supports — for example, the Nexus client for the e200z4 that supports Class 3 functionality is called the NZ4C3.

- eTPU — The Enhanced Timing Processor (eTPU or eTPU2) is a task-specific computing engine that is designed primarily for dealing with timing functions and includes some mathematics capabilities (including multiplication and division). The eTPU Nexus client is implemented as either a dual eTPU engine (Nexus Dual eTPU Development Interface — NDEDI) or a single eTPU engine client (Nexus Single eTPU Development Interface — NSEDI). In addition to the eTPU engine interface, the NDEDI/NSEDI interfaces with a secondary Nexus client, the Coherent Data-Parameter Controller (CDC). The CDC supports the shared memory and logic between the dual eTPU engines. On NDEDI devices, the eTPU Nexus interface appears to have three sub-clients (the two eTPU engines and the CDC); on NSEDI devices there are two (one engine and the CDC).
- Bus Trace Clients — Another trace client available is a Nexus client that traces data accesses made through a crossbar bus port. Usually, these have been implemented on the master side of the crossbar switch for the eDMA module and the FlexRay communication interface. This allows master accesses made by these bus masters to peripherals or memory accessed through the crossbar switch bus (XBAR). Freescale has chosen to implement these interfaces on the master side of the crossbar for most devices, but this module can also be instantiated on the slave side of the crossbar switch on future devices, allowing trace of all accesses into a particular slave port of the crossbar switch bus. Bus trace clients are referenced by the type of interface they support. For example, the Nexus eDMA Master XBAR client is referred to as the NXDM; the FlexRay Master XBAR trace client is the NXFR.

2.1 Nexus class 1 JTAG-only operation

For Nexus class 1 (run control only) operation, the JTAG pins can be used for standard, stopped mode debug operations. In this mode, Nexus does not have to be enabled and the auxiliary port pins can be ignored by the debugger. Since there is no JTAG standard connector pinout definition, Freescale recommends that class-1-only debuggers use the same connector options as full Nexus debuggers. This allows customers to avoid having to put two separate connectors on boards, one for Nexus and one for JTAG-only debug tools. However, this document includes a definition for a 14-pin BERG style connector (2×7 , 0.1" [2.54 mm] pin centers) for extremely low-cost applications that cannot use one of the full Nexus connectors.

NOTE

The Nexus class 3 feature read/write access is accessible through a JTAG connection. Other Class 3 features are not available unless a full Nexus connector is used.

NOTE

It is recommended that all the full Nexus signals be made available (somewhere) on production boards to facilitate debugging new boards and analysis of errors in software, even on boards that have restricted space and provide a JTAG-only connection. If all of the Nexus signals are available on the production board, an adapter could be built to provide a Nexus connection on boards that do not have a complete footprint for one of the standard Nexus connectors. Likewise, the JTAG connector does not have to be populated on production boards, and could even use a smaller connector footprint. An adapter could then be used to provide standard debug connections.

3 Recommended debug connectors and connector pin out definitions

The table below shows the recommended connectors for different applications for the MPC567xF and MPC567xR.

Table 1. Recommended connectors

Connector style	Target system part number	Connector type
14-pin BERG JTAG only	3M 2514-6002UB	JTAG-only configuration
25-position (2 x 25, 50-pin) Samtec	Samtec ASP-148422-01	Full Nexus configuration
38-pin MICTOR ¹	Tyco 767054-1 ²	Full Nexus configuration

1. Recommended for backward compatibility only. Not recommended for 16-bit MDO support. The Lauterbach LA-7631 Mictor adapter has four solder pad options for connecting MDO[12:15]. Older interfaces do not support the 16-bit wide mode.
2. Other compatible part numbers are 2-5767004-2 (RoHS compliant), 2-767004-2, 767061-1, and 767044-1.

NOTE

Whichever connector is chosen, "keep-out" areas may be required by some tools. Consult the preferred tool vendor to determine any area that must remain clear around the debug connector. Some tool vendors may include an extension cable to minimize "keep-out" areas, but use of an extension will degrade the signal. In many cases, this degradation will be insignificant, but the amount of degradation depends on many factors, including clock frequency and target board layout.

3.1 MPC5600 JTAG connector

The figure below shows the pinout of the recommended JTAG connector to support the MPC5600 devices. If there is enough room allowed in the target system, a full Nexus connector is preferred over the simple 14-pin JTAG connector since it allows a higher degree of debug capability. It can be used as a minimum debug access or for BSDL board testing.

The recommended connector for the target system is the Tyco part number 2514-6002UB.

NOTE

This pinout is similar to the Freescale MCORE and DSP JTAG/OnCE connector definitions.

Table 2. Recommended JTAG connector pinout

Description	Pin	Pin	Description
TDI	1	2	GND
TDO	3	4	GND
TCK	5	6	GND
$\overline{\text{EVTI}}^1$	7	8	—
RESET	9	10	TMS
VREF	11	12	GND
$\overline{\text{RDY}}^2$	13	14	JCOMP

1. EVTI is optional and was not included in the original (very early) definitions of the JTAG-only connector.
2. The RDY signal is not available on all packages or on all devices. Check the device pinout specification. In general it is not available in packages with 208 signals or less.

NOTE

Freescale recommends that a full Nexus connector be used for all tool debug connections, regardless of whether Nexus trace information is needed. Adapters for a JTAG class 1 14-pin connector (tool side) to the full Nexus MICTOR connectors (board side) are available from P&E Microcomputer Systems (<http://www.pemicro.com>), part number PE1906, and from Lauterbach (<http://www.lauterbach.com>), order number LA-3723 (CON-JTAG14-MICTOR). Lauterbach also has an adapter that will connect a MICTOR connector (tool side) to a 14-pin JTAG connector (board side). This adapter is order number LA-3725 (CON-MIC38-J14-5500).

3.2 MPC56xx high-speed parallel trace connector

For high speed trace applications, the MICTOR-38 connector is not optimized for best signal integrity when using more than eight Message Data Out signals (MDO). Twelve MDO pins push the capability of the connector from a signal integrity standpoint. When moving to devices that support the full 16-bit MDO, a Samtec ERF8 series connector is highly recommended. The part number of the Samtec connector is shown in the following table.

Table 3. Recommended high-speed parallel trace connector part number

Connector	Part number (Samtec)	Style	Description
HP50	ASP-148422-01	Samtec ERF8 Series, 25 position by 2 row	Vertical mount for MCU module

The Samtec ERF8 series of connectors is intended for high speed applications requiring a minimum footprint size with a reliable, latching connection. The recommended connector has two rows of twenty-five contacts each with a spacing of 0.8 mm. The connector provides isolation between the high-speed trace signals and the low-speed JTAG and control signals. It also provides ample ground connections to ensure signal integrity.

The following picture is courtesy of Samtec U.S.A (<http://www.samtec.com/search/NEXUS.aspx>).

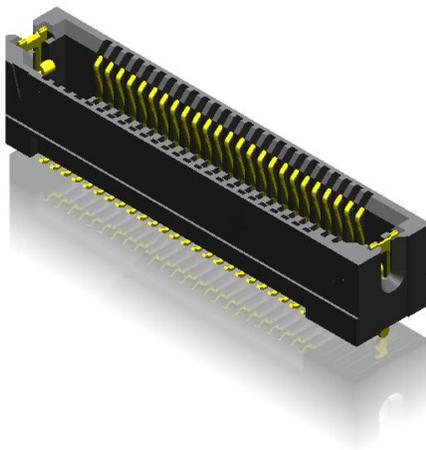


Figure 2. HP50 (ASP-148422-01) connector

recommended debug connectors and connector pin out definitions

The table below shows the recommended pinout for the Samtec connector.

Table 4. MPC56xx high-speed parallel trace connector

Position	Signal	Direction ¹	Pin number	Pin number	Direction ¹	Signal	IEEE-5001-2011 GEN_IO signal name
	GND ²					GND ²	
1	MSE00	Out	1	2	Out ³	VREF	
2	MSE01	Out	3	4	In	TCK	
3	GND		5	6	In	TMS	
4	MDO0	Out	7	8	In	TDI	
5	MDO1	Out	9	10	Out	TDO	
6	GND		11	12	In	JCOMP	
7	MDO2	Out	13	14	Out	RDY	
8	MDO3	Out	15	16	In	EVTI	
9	GND		17	18	Out	EVT0	
10	MCKO	Out	19	20	In	RESET	
11	MDO4	Out	21	22	Out	RSTOUT	GEN_IO0
12	GND		23	24		GND	
13	MDO5	Out	25	26	Out	CLKOUT	
14	MDO6	Out	27	28	In/Out	TD/WDT	GEN_IO1
15	GND		29	30		GND	
16	MDO7	Out	31	32	In/Out	DAI1	GEN_IO2
17	MDO8	Out	33	34	In/Out	DAI2	GEN_IO3
18	GND		35	36		GND	
19	MDO9	Out	37	38		ARBREQ	GEN_IO4
20	MDO10	Out	39	40		ARBGRT	GEN_IO5
21	GND		41	42		GND	
22	MDO11	Out	43	44	Out	MDO13	
23	MDO12	Out	45	46	Out	MDO14	
24	GND		47	48		GND	
25	MDO15	Out	49	50		N/C ⁴	
	GND ²					GND ²	

1. Viewed from the MCU.
2. The connector locking mechanism provides additional ground connections on each end of the connector.
3. This is an output from the connector standpoint. It may or may not be from the MCU.
4. No connection — should be left open. Reserved for MDO16 on devices with more than sixteen MDO signals (future compatibility). In some applications this may be used as an SRAM voltage detect to determine when voltage for a standby SRAM is disconnected.

3.2.1 High speed parallel trace general purpose pin definitions

The Nexus Samtec high speed parallel trace connector contains six pins that are left for definition by the MCU architecture definition. The following table lists the general I/O (GEN_IOx) signal definitions for the MPC567xF/MPC567xR.

Table 5. General IO definitions

General IO pin	Connector pin number	MPC567xF/ MPC5674R definition	Description
GEN_IO0	22	RSTOUT	Reset Out is a monitor output for tools to determine if the RSTOUT pin of the MCU has been asserted. ¹
GEN_IO1	28	TD/WDT ²	Tool detect and watchdog disable — The watchdog disable input is an input signal to the target system MCU that can be used to disable any system watchdog timer (not located in the target system primary MCU). For normal operation (no tool attached), this pin should have a pulldown resistor installed in the system. Tools can drive the pin high to disable the external watchdog. This signal is optional from the MCU standpoint and is defined for standardization of systems that require this additional functionality. In addition, this signal can be used in multi-tool environments to indicate to tools attached downstream that a tool is attached.
GEN_IO2	32	DAI1 ²	Data acquisition trigger pin — optional signal that can be used as a signal to the external tool. This pin may be attached to a general purpose IO pin of the MCU. The complete definition of this pin is left for the system designer and the tool vendor.
GEN_IO3	34	DAI2 ²	Data acquisition trigger pin — optional signal that can be used as a signal to the external tool. This pin may be attached to a general purpose IO pin of the MCU. The complete definition of this pin is left for the system designer and the tool vendor.
GEN_IO4	38	ARBREQ ²	Tool arbitration request — This signal has no defined purpose for or connection to the MCU. It is reserved for use in situations that require multiple tools to arbitrate for the MCU Nexus interface. This is the tool request for access.
GEN_IO5	40	ARBGR ²	Tool arbitration grant — This signal has no defined purpose for or connection to the MCU. It is reserved for use in situations that require multiple tools to arbitrate for the MCU Nexus interface. This is the tool grant signal.

1. The MPC56xx family allows the RSTOUT pin to be asserted without resetting the MCU itself. Tools may need to know if user software allows this functionality. Otherwise, RSTOUT is asserted only when the MCU responds to an internal reset or the RESET input assertion.
2. These functions are defined for use by some tools and may not be required in all cases. Contact your tool vendor for exact signal requirements.

3.3 MICTOR connector definition for the MPC567xF/MPC567xR family

The following table shows the complete signal usage for the MPC567xF/MPC567xR full-port mode MICTOR connector that supports the 16-bit MDO option. This uses the Vendor_IO pins 1–4 as MDO[11:8] and the reserved pins of the connector for the MDO[15:12]. This connector may also be used for reduced-port mode (which only uses MDO[11:0]). While only one

recommended debug connectors and connector pin out definitions

MICTOR is recommended, some tools may not support this configuration. For maximum tool compatibility, a second MICTOR may need to be added for the upper eight MDO signals (MDO[15:8]). If the second connector is used, the layout of the two connectors should conform to the dimensions in the figure following the tables.

Attention

Using the MICTOR-38 is recommended only when backwards compatibility to previous devices and existing tools is required. It is highly recommended that the Samtec high speed parallel connector option be used instead.

Table 6. MPC567xF/MPC567xR family MICTOR connector M38C

MPC5600 signal	Combined M38C or M38-2C	Direction	Pin number		Pin number	Direction	Combined M38C or M38-2C	MPC5600 signal
MDO12	Reserved	Out	1	Ground	2	Out	Reserved	MDO13
MDO14	Reserved	Out	3		4	Out	Reserved	MDO15
MDO9	VEN_IO0	Out	5		6	Out	CLOCKOUT	CLKOUT
BOOTCFG1	VEN_IO2	In	7		8	Out	VEN_IO3	MDO8
RESET	/RESET	In	9		10	In	/EVTI	EVTI
TDO	TDO	Out	11		12	—	VREF	VDDE2
MDO10	VEN_IO4	Out	13		14	Out	/RDY	RDY
TCK	TCK	In	15		16	Out	MDO7	MDO7
TMS	TMS	In	17	Ground	18	Out	MDO6	MDO6
TDI	TDI	In	19		20	Out	MDO5	MDO5
JCOMP	/TRST	In	21		22	Out	MDO4	MDO4
MDO11	VEN_IO1	Out	23	Ground	24	Out	MDO3	MDO3
RSTOUT	TOOL_IO3	Out	25		26	Out	MDO2	MDO2
TD/WDT	TOOL_IO2	—	27		28	Out	MDO1	MDO1
ARBGR1	TOOL_IO1	—	29		30	Out	MDO0	MDO0
12 V	UBATT	—	31		32	Out	/EVT0	EVT0
12 V	UBATT	—	33		34	Out	MCKO	MCKO
ARBREQ	TOOL_IO0	—	35		36	Out	/MSE01	MSE01
VSTBY	VALTREF	—	37	38	Out	/MSE00	MSE00	

Table 7. MPC5600 Family MICTOR Connector M38-2C (if necessary)

MPC5600 signal	Combined M38-2C	Direction	Pin number		Pin number	Direction	Combined M38-2C	MPC5600 signal
—	Reserved	—	1	Ground	2	—	Reserved	—
—	Reserved	—	3		4	—	Reserved	—
—	VEN_IO5	In/Out	5		6	—	—	—
—	VEN_IO6	In/Out	7		8	In/Out	PORT15	—
—	VEN_IO7	In/Out	9		10	In/Out	PORT14	—
—	VEN_IO8	In/Out	11		12	In/Out	PORT13	—
—	VEN_IO9	In/Out	13		14	In/Out	PORT12	—
—	TOOL_IO7	In/Out	15		16	In/Out	PORT11	—
—	TOOL_IO6	In/Out	17	Ground	18	In/Out	PORT10	—
—	TOOL_IO5	In/Out	19		20	In/Out	PORT9	—
—	TOOL_IO4	In/Out	21		22	In/Out	PORT8	—
MDO15	MDO15	Out	23	Ground	24	In/Out	PORT7	—
MDO14	MDO14	Out	25		26	In/Out	PORT6	—
MDO13	MDO13	Out	27		28	In/Out	PORT5	—
MDO12	MDO12	Out	29		30	In/Out	PORT4	—
MDO11 ¹	MDO11	Out	31		32	In/Out	PORT3	—
MDO10 ²	MDO10	Out	33		34	In/Out	PORT2	—
MDO9 ³	MDO9	Out	35		36	In/Out	PORT1	—
MDO8 ⁴	MDO8	Out	37	38	In/Out	PORT0 ⁵	—	

1. This pin duplicates the signal available on pin 23 of the first MICTOR connector.
2. This pin duplicates the signal available on pin 13 of the first MICTOR connector.
3. This pin duplicates the signal available on pin 8 of the first MICTOR connector.
4. This pin duplicates the signal available on pin 7 of the first MICTOR connector.
5. The MPC5600 family does not support port replacement.

The following figure shows the recommended layout for the M38-2C connectors.

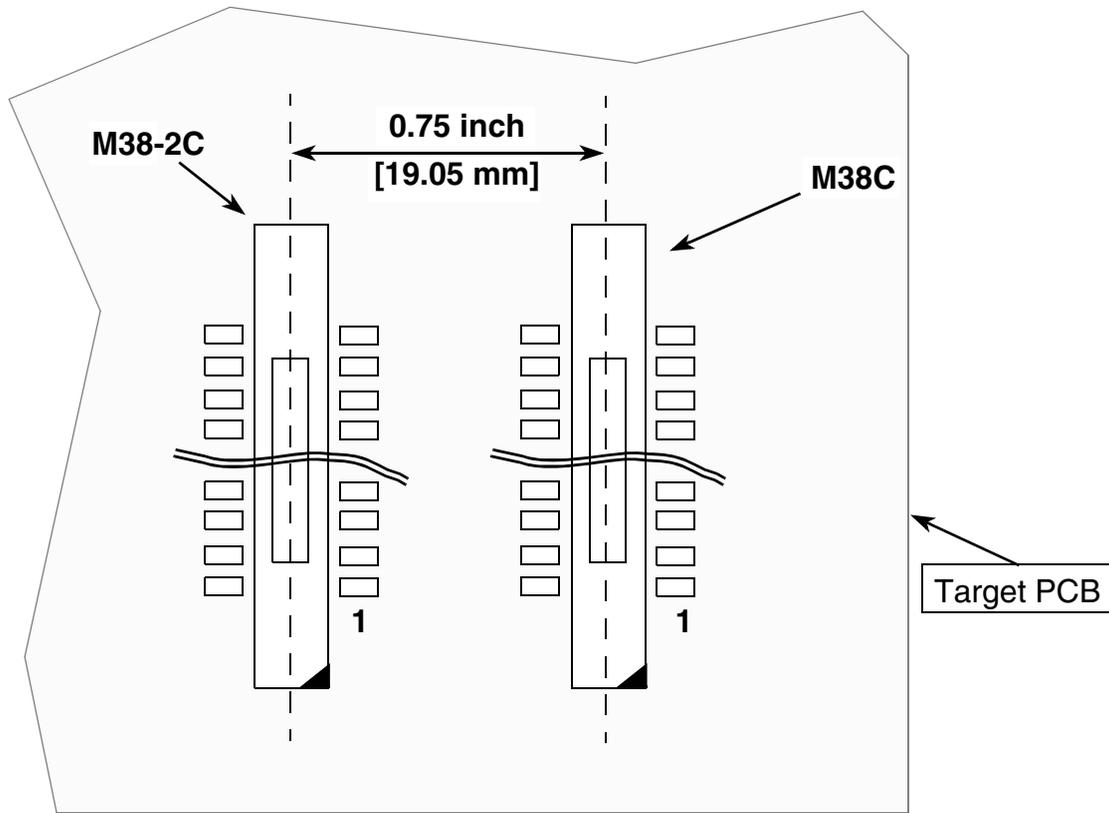
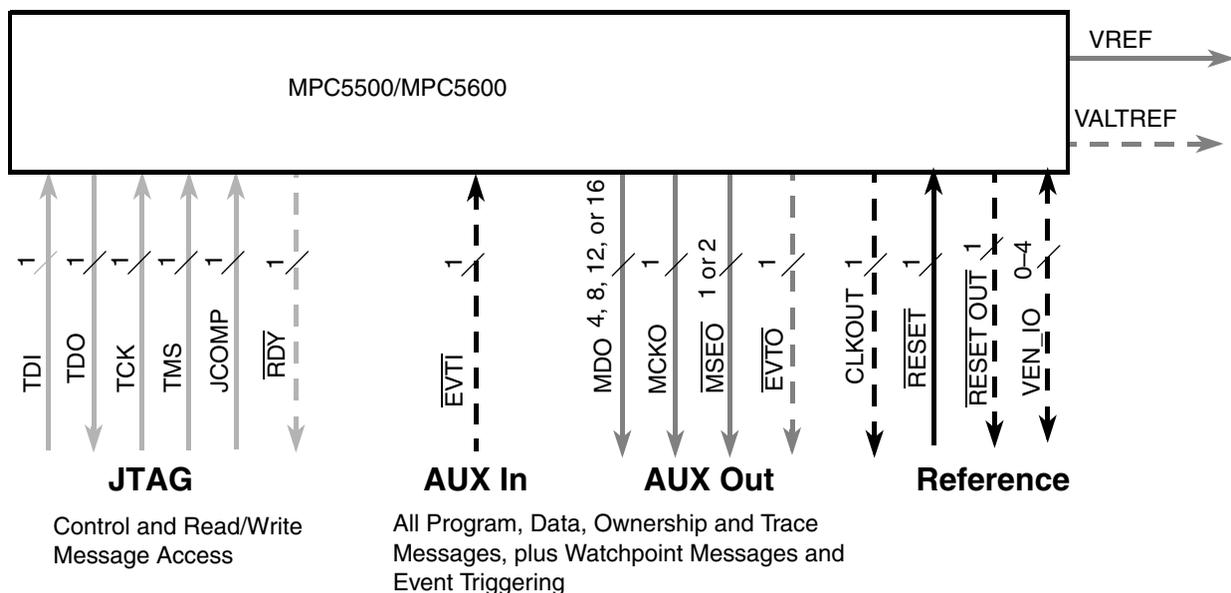


Figure 3. Nexus M38-2C connector layout

4 Nexus signals for the MPC5600 family

The figure below shows a block diagram of the MPC5600 family Nexus signals. The pins are divided between the JTAG/OnCE port, the auxiliary input port, the auxiliary output port, and reference signals. The $\overline{\text{RDY}}$ pin is grouped with the JTAG pins, but it is used for Nexus block transfers done through the JTAG port (read/write messaging).



Note: Dashed signals are optional in the Nexus standard. Tool_IO pins do not have any connectivity to the MCU.

Figure 4. Pin interface for an MPC5600 Nexus combined JTAG/AUX port

The auxiliary output port can be implemented with twelve or sixteen Message Data Output signals (MDO) and either one or two Message Start/End Output signals (MSEO).

Some of the auxiliary output port functions on the MPC5600 family are shared with other pin functions. The following sections show the JTAG and Nexus auxiliary port signals versus the MPC5600 pins and signal descriptions.

4.1 MPC5600 JTAG signals

The following table shows the JTAG signals for the MPC5500 and MPC5600 families.

Table 8. JTAG connector signal descriptions

JTAG signal	Description
TDO	JTAG Test Data Output (TDO) TDO provides the serial test data output for the on-chip test logic.
TDI	JTAG Test Data Input (TDI) TDI provides the serial test instruction and data input for the on-chip test logic.
TCK	JTAG Test Clock Input (TCK) TCK is the clock input to the JTAG TAP controller and should be a maximum of one-fourth of the system clock frequency.
TMS	JTAG Test Mode Select Input (TMS) $\overline{\text{TMS}}$ controls test mode operations for the on-chip test logic for boundary scan and debug access.

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Table 8. JTAG connector signal descriptions (continued)

JTAG signal	Description
EVTI	<p>Nexus Event In ($\overline{\text{EVTI}}$)</p> <p>After reset, the $\overline{\text{EVTI}}$ pin is used to initiate program and data trace synchronization messages or generate a breakpoint. If asserted during reset, upon negation of $\overline{\text{RESET}}$, the device will enter debug mode and not begin code execution.</p>
RDY	<p>Nexus Ready Output ($\overline{\text{RDY}}$)</p> <p>$\overline{\text{RDY}}$ is an output that indicates to the development tools that the data is ready to be read from or written to the Nexus read/write access registers.</p>
RESET	<p>Reset ($\overline{\text{RESET}}$)</p> <p>This is the reset input to the microcontroller. It should be driven by tools to reset the microcontroller. It should be driven by an open drain device. The tool should also monitor this pin to determine if other devices have forced a reset to the microcontroller. It does not reset the JTAG state machine.</p>
JCOMP	<p>JTAG TAP Controller Enable/ JTAG Compliancy ($\overline{\text{JCOMP}}$)</p> <p>JCOMP is used to enable the TAP controller for communication to the JTAG state machine for boundary scan and for debug access. A high on this pin enables the TAP controller.¹</p>
VREF	<p>Nexus VREF ($\overline{\text{VREF}}$)</p> <p>Provides a reference for the signal levels of the Nexus device. All input high and low voltages should be referenced to this pin. The Nexus specification defines the input voltages as $V_{IL} = 0.3 \times V_{REF}$ and $V_{IH} = 0.7 \times V_{REF}$.</p> <p>NOTE: This is a reference for the signal level and may not be the actual power supply for the debug pins. See the device definition for the debug pins in the device reference manual.</p>
GND	<p>Ground</p> <p>This is the negative reference (return) for the interface.</p>

1. The IEEE 1149.1 specifies a Test Reset ($\overline{\text{TRST}}$) pin; however, the standard defines that by default the pin should be high (enabled) on the device. Since normal operation of the device does not require the JTAG port to be enabled, Freescale uses the JTAG compliancy pin ($\overline{\text{JCOMP}}$), which performs the same basic function, but is asserted (low) by default to disable the JTAG boundary scan/debug port (for normal operation).

The recommended voltage of the JTAG connector is a nominal 3.3 V for the MPC5500 family devices. For the MPC5600 family and the MPC5510 family, see the definition in each device's reference manual for the recommended voltage. Some devices recommend a nominal 3.3 V and some devices are 5.0 V.

4.2 Nexus auxiliary port signals

The Nexus auxiliary port provides trace and event signalling information out of the device, as well as an optional input that can be used to signal the MCU. Some of the auxiliary output port functions on the MPC5600 family are shared with other pin functions; however, many are dedicated debug signals on the MCU. [Table 9](#) shows the Nexus auxiliary port signals.

Table 9. Nexus auxiliary port signal descriptions

Signal Type	Nexus Signal	MPC5600 Signal	Full Signal Name	Description
Auxiliary Output Port	/EVTO	EVTO	Nexus Event Out	EVTO is an output that provides timing to a development tool for a single watchpoint or breakpoint occurrence.
	/MSEO[1:0]	MSEO[1:0]	Nexus Message Start/End Output	The MSEO[1:0] signals indicate when an MDO packet has started and when an MDO packet has ended.
	MCKO	MCKO	Nexus Message Clock Out	MCKO provides timing for the MDO and MSEO[0:1] signals.
	MDO[15:0]	MDO15_GPIO234 MDO14_GPIO233 MDO13_GPIO232 MDO12_GPIO231 MDO11_GPIO82 MDO10_GPIO81 MDO9_GPIO80 MDO8_GPIO70 MDO7_GPIO78 MDO6_GPIO77 MDO5_GPIO76 MDO4_GPIO75 MDO3_GPIO223 MDO2_GPIO222 MDO1_GPIO221 MDO0_GPIO220	Nexus Message Data Output	MDO[11:0] provide the message data out of the auxiliary output port in the reduced-port configuration. The full-port configuration uses MDO[15:0].
Auxiliary Input Port	/EVTI	EVTI	Nexus Event Input	After reset, the EVTI pin is used to initiate program and data trace synchronization messages or generate a breakpoint. If asserted during reset, upon negation of RESET, the device will enter debug mode and not begin code execution.

4.3 Other Nexus connector signals

In addition to the JTAG and Nexus auxiliary port signals, there are additional signals included on the connector for reference and for use by tools or other purposes. The following table shows the definition of these signals.

Table 10. Other Nexus connector signal descriptions

Signal Type	Nexus Signal ¹	MPC5600 Signal	Full Signal Name	Description
GEN_IO	GEN_IO6	BOOTCFG1_IRQ3_GPIO212	General IO 6	Nexus General IO6 (GEN_IO6). The MPC567xF signal BOOTCFG1_IRQ3_GPIO212 gives the Nexus tool access to IRQ3. This signal can either generate an interrupt to the interrupt controller or can be used to initiate a DMA transfer via DMA channel 3. This allows the Nexus port to request a DMA transfer. It can also invoke the DMA gather data feature. The BOOTCFG1 function can be used during reset to change the default boot mode of the device.
	GEN_IO4 ²	—	General IO 4	Nexus General IO4 (ARBREQ) on the Mictor connector is reserved for use as a bus request signal for arbitration between different tools on the Nexus bus. It has no connection to the MPC5600 device. NOTE: Tool arbitration is an informal extension of the Nexus IEEE-ISTO 5001-2003 specification and has not been approved by the Nexus Consortium.
	GEN_IO5 ²	—	General IO 5	Nexus General IO5 (ARBGR) on the Mictor connector is reserved for use as a bus grant signal for arbitration between different tools on the Nexus bus. It has no connection to the MPC567xF device. NOTE: Tool arbitration is an informal extension of the Nexus IEEE-ISTO 5001-2003 specification and has not been approved by the Nexus Consortium.
	GEN_IO2 ²	—	General IO 2	Nexus General IO2 on the Mictor connector is defined as the Tool Detect and watchdog disable. The watchdog disable input is an input signal to the target system MCU that can be used to disable any system watchdog timer (not located in the target system primary MCU). For normal operation (no tool attached), this pin should have a pulldown resistor installed in the system. Tools can drive the pin high to disable the external watchdog. This signal is optional from the MCU standpoint and is defined for standardization of systems that require this additional functionality. In addition, this signal can be used in multi-tool environments to indicate to tools attached downstream that a tool is attached.

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Table 10. Other Nexus connector signal descriptions (continued)

Signal Type	Nexus Signal ¹	MPC5600 Signal	Full Signal Name	Description
GEN_IO	GEN_IO0	—	General IO 0	Nexus General IO0 ($\overline{\text{RSTOUT}}$) on the Mictor connector is defined on the MICTOR 38 pin connector as $\overline{\text{RSTOUT}}$ of the MPC5600. This allows a tool to monitor when the MCU has caused an internal reset, however, all tools may not monitor $\overline{\text{RSTOUT}}$. NOTE: The MCU can drive $\overline{\text{RSTOUT}}$ low via software to reset external devices, but not cause a reset of the MCU.
Reference Signals	/RESET	RESET	/Reset	Reset (/RESET). This is the reset input to the MPC567xF microcontroller and should be driven by tools to reset the microcontroller. It should be driven by an open drain device. The tool should also monitor this pin to determine if other devices have forced a reset to the microcontroller. It does not reset the JTAG state machine.
	CLOCKOUT	CLKOUT	System Clock Output	Clock Out (CLKOUT). Clock out provides a reference clock for determining the system clock frequency. This signal is optional and may not be available on all packages and the user can disable this signal.
	VREF	VDDE2	Signal Power Reference	Nexus VREF (VREF). Provides a reference for the signal levels of the Nexus device. All input high and low voltages should be referenced to this pin. The Nexus specification defines the input voltages as $V_{IL} = 0.3 \times V_{REF}$ and $V_{IH} = 0.7 \times V_{REF}$.
	VALTREF	VSTBY	Alternate Reference	Nexus VALTREF (VSTBY). Provides a monitor for the backup power supply for the MPC567xF internal SRAM. This pin is monitored by the Nexus tool to determine if power is lost to the standby supply of the system. This pin should be grounded if standby operation is not allowed in a particular system.
	GND	GND	Ground Reference	Ground. This is the return (ground) reference point for the Nexus connectors. Many ground signals are included to provide shielding for the high-speed Nexus signals. In the MICTOR connector, the center pins should be grounded.
	UBATT ³	12 V	Unregulated Battery Voltage	Battery/unregulated module voltage. This is a supply voltage output from the target system and should have reverse-bias protection. This allows tools to have circuitry powered by the target system. The IEEE-ISTO 5001-2003 defines this as a 5–20 V supply of up to 300 mA of current.

1. The General IO signals on the Mictor-38 connector are defined differently than the SAMTEC high speed connector for legacy reasons.
2. These functions are defined for use by some tools and may not be required in all cases. Contact your tool vendor for exact signal requirements.

3. Not available on the high speed parallel connector.

5 Nexus connector voltages

All of the Nexus and JTAG pins on the MPC567xF and MPC567xR are supplied by VDDE2. VDDE2 can be used with any voltage from 1.62 V to 3.6 V. The user determines the voltage level of the Nexus pins. See the following table for the common voltages that could be used. Most commonly, this should be set to 3.3 V, which is also the most common bus voltage used on the MPC5600 family.

Table 11. Nexus port voltages options

System bus voltage	Recommended Nexus voltage
1.8 V	1.8 V
2.5 V	2.5 V
3.3 V	3.3 V ¹

1. A 3.3 V supply is the preferred option. 1.8 V and 2.5 V are not recommended, but they are allowed by the specifications.

On the MPC5600 devices, the $\overline{\text{RESET}}$ input should be driven by devices with an open drain. The target system is required to have a pullup device to the device power supply; this can be up to 5 V for the MPC5600. Care must be taken to insure that all circuitry connected to the $\overline{\text{RESET}}$ signal is 5-V tolerant. Tools need to be able to drive $\overline{\text{RESET}}$, but they also need to sense $\overline{\text{RESET}}$ to determine if another device in the target system has requested that the MCU be reset.

NOTE

$\overline{\text{RESET}}$ and $\overline{\text{RSTOUT}}$ are powered by VDDEH1. VDDEH1 can have a nominal voltage of 3.3 V or 5.0 V. Other than the UBATT pins, the IEEE-ISTO 5001-2003 standard does not allow voltages greater than VREF. If VDDEH1 is connected to 5.0 V, then the tool must have protection for the $\overline{\text{RESET}}$ and $\overline{\text{RSTOUT}}$ signals.

NOTE

Consult the hardware specifications of the debug interface to insure that the voltages are all compatible with the module design.

6 Minimum external circuitry

In general, other than the connector, no additional circuitry is required for the Nexus/JTAG debug circuitry. The MPC5600 devices include internal pull devices that ensure the pins remain in a safe state; however, if there is additional circuitry connected to the Nexus/JTAG pins, or long traces that could be affected by other signals (due to crosstalk from high-current or high-speed signals), a minimum number of external pull resistors can be added to insure proper operation under all conditions.

Table 12. Optional minimum debug port external resistors

Nexus/JTAG signal	Resistor direction and value	Description
JCOMP	10 k Ω pulldown	Holds debug port in reset and prevents any debug commands from interfering with the normal operation of the MCU.
RESET	4.7 k Ω pullup	The $\overline{\text{RESET}}$ input should be driven from an open collector output; therefore, it requires a pullup resistor for the MCU.

Table continues on the next page...

Table 12. Optional minimum debug port external resistors (continued)

Nexus/JTAG signal	Resistor direction and value	Description
TD/WDT ¹	10 kΩ pulldown	With no tool attached, this signal should be held low and may or may not be connected to a pin of the MCU, depending on the system definition.
EVTI	10 kΩ pullup	A pullup resistor prevents debug mode from being forced after reset if debug mode is enabled (JCOMP = high). It also prevents breakpoints from being forced if debug mode is enabled. NOTE: In almost all situations, a resistor is not required on this signal.

1. This is an optional signal and is not actually required for the MCU.

In addition to the pullup and pulldown resistors, some systems may want to use buffers between the Nexus/JTAG connector inputs and the MCU. This will prevent over-voltage conditions from causing damage to the MCU signals. Normal systems should not require this circuitry, but it is helpful in systems that can be exposed to improper connections that provide voltages that are outside the operating conditions of the MCU. A common circuit to use is the Texas Instruments SN74CBTLV3861⁴. This device is a bus switch that implements a bidirectional interface between two terminals with less than 5 Ω of resistance. It should be powered by the same supply that powers the debug port. The device enable should be connected to ground for the interface to be enabled whenever the debug port on the MCU is powered. This circuit provides a high impedance to the tool when the debug port is powered off.

NOTE

It is recommended that at least the reduced port configuration Nexus signals be made available (somewhere) on production boards. This facilitates debugging of new boards and analysis of errors in software, even on boards that have restricted space and normally provide a JTAG-only connection. If the Nexus signals are available on the production board, an adapter could be built to provide a Nexus connection on boards that do not have a complete footprint for one of the standard Nexus connectors. Likewise, the JTAG connector does not have to be populated on production boards and could even utilize a smaller connector footprint that could be used with an adapter to the standard debug connections.

7 Nexus port configuration register

The Nexus Port Controller Port Configuration Register (NPC_PCR) controls the operation and configuration of the Nexus debug interface for the entire device. This register overrides any control settings (MCKO_DIV, FPM, and MCKO_EN) that may be available in individual Nexus client (NDEDI/NSEDI, NZ6C3/NZ3C3, NXDM, and NXFR) Debug Control (DC) or Port Configuration Registers (PCR).

During $\overline{\text{RESET}}$, the MPC5600 will assert (high) MDO0 until the PLL is locked or until there is a stable clock (depending on the device) after the initial internal power-on reset. Once MDO0 is negated (low), access to the JTAG controller is enabled and registers can be written by tools. The Nexus port should be enabled in the NPC_PCR while the processor is in reset. After the port has been configured, the NPC will transmit a device identification (DID) message through the Nexus auxiliary output port.

The bit fields are described in the next four subsections.

4. SN74CBTLV3861-Q1 is automotive qualified if required.

NOTE

The numbering of the bits in the NPC_PCR are set per the IEEE-ISTO 5001 standard, as this register is accessed only by tools and the CPU cannot write to any of the bits in the register. All bits are controlled by the external tool.

Table 13. NPC Port Configuration Register (NPC_PCR)

NPC Register Index 127		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	R	FPM	MCKO_GT	MCKO_EN	MCKO_DIV			EVT_E N ¹	DDR_EN 2	NEXCF G ³	0	0	0	0	0	0	0	
	W																	
	Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	R	LP_DBG 4							LP2_SYN ⁴	LP1_SYN ⁴								
	W																	
	Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSTAT_EN 5

1. This bit is not implemented on all devices. It is not implemented on the MPC567xF.
2. The Double Data Rate feature does not conform to the Nexus 5001 standard and is not supported on all devices. This bit is not supported on the MPC567xF or MPC5676R.
3. This bit is not implemented on all devices. This use of this bit is determined by the MCU definition. This bit is not supported on the MPC567xF or MPC5676R.
4. This bit is not supported on devices that do not support true low-power modes (where some power supplies can be removed from the MCU). This bit is not supported on the MPC567xF or MPC5676R.
5. PSTAT is an internal Freescale monitor mechanism and its use is not supported. This bit should always be set to 0.

7.1 Nexus port size (NPC_PCR[FPM])

The configuration of the full-port mode or reduced-port mode is selected via the JTAG port by setting of the Full Port Mode (FPM) bit in the Nexus Development Interface port configuration register (NPC_PCR). Setting NPC_PCR[FPM] selects full-port mode. Clearing NPC_PCR[FPM] selects reduced-port mode. In RPM, MDO[12:15] are defined to the GPIO function; FPM automatically disables the GPIO function.

Table 14. MPC567x family Nexus port sizes across packages

Device	Package	Reduced port size	Full port size
MPC567xF/MPC567xR	416 PBGA	12	16
	516 PBGA	12	16
MPC567xR	416 PBGA	12	16
	516 PBGA	12	16

7.2 Nexus clock speed (NPC_PCR[MCKO_DIV])

The Nexus auxiliary clock prescaler should be programmed in the NPC_PCR. For systems with a maximum operating frequency of over 80 MHz, the auxiliary clock prescaler should be set to divide by two or more. MCKO_DIV should not be changed after the auxiliary output port is enabled (NPC_PCR[MCKO_EN]). The ability to run the MCKO at the same frequency as the system frequency is available on some devices if the system frequency is 80 MHz or less. In all cases, see the device electrical specification to determine if the signals have any other speed limitations.

Table 15. Nexus MCKO clock divider options

MCKO_DIV	MCKO frequency
0b000	System frequency ¹
0b001	System frequency ÷ 2
0b010	Reserved
0b011	System frequency ÷ 4
0b100	Reserved
0b101	Reserved
0b110	Reserved
0b111	System frequency ÷ 8

1. The 1× clock mode is not supported on all devices. In addition, MCKO is limited to 80 MHz maximum on all devices.

The speed of the Nexus port limits the amount of trace information that will be available to tools. Enabling too much trace will cause overflows of the trace buffers included on the device. In general, trace of the core program execution will not cause overflows with the MCKO frequency set to divide by two. A divide of four may also support full instruction trace if branch history mode is used. Enabling data trace may cause overruns if too much information is requested. Care should be taken when enabling data trace to limit the information that should be traced. Watchpoints can be used to enable trace upon an event occurrence and then disabled by a second event to limit the data trace bandwidth requirements.

7.3 Nexus clock gating (NPC_PCR[MCKO_GT])

The Nexus auxiliary output clock (MCKO) can be gated off when the MCU is not transmitting trace information. Setting NPC_PCR[MCKO_GT] gates the auxiliary clock off when auxiliary messages are not being transmitted. If this bit is cleared, then the Nexus auxiliary clock is always present when the Nexus auxiliary port is enabled.

NOTE

Tools may require that the MCKO not be gated. Check with your tool vendor to determine if the tool can work with a gated MCKO.

7.4 Unsupported bits in the NPC_PCR

Low power modes are not supported on all devices. Therefore the Low Power Debug Enable (LP_DBG) and the Low Power Mode Synchronization (LP2_SYN and LP1_SYN) bits in the NPC_PCR are not supported.

The Dual Data Rate (DDR) enables a non-standard signal format that clocks two bits per clock cycle. The MDO bits are valid on both edges of MCKO. This convention is not covered by the IEEE-ISTO5001 standard and is not expected to be supported by the standard. This feature is not supported on this device.

The Nexus Configuration (NEXCFG) bit is not supported on all devices. If NEXCFG is not supported, the bit in the register may be writable, but writes will not have any affect.

The Processor Status Enable (PSTAT_EN) is for internal Freescale use only and should always be set to 0b0.

Appendix A MPC5600 available debug adapters

A number of adapters are available to ease the task of having full debug capabilities available with a minimum board footprint impact to the target system. The following table lists adapters that are available from Freescale and third-party manufacturers.

Table A-1. Available debug connector adapters

Part number	Description	Manufacturer
PE1906	14-pin JTAG debug tool to MICTOR 38-pin target board connector adapter	P&E Microcomputer Systems
LA-3723 CON-JTAG14-MICTOR	14-pin JTAG debug tool to MICTOR 38-pin target board connector adapter	Lauterbach GmbH
LA-3725 CON-MIC38-J14-5500	38-pin MICTOR debug trace tool to 14-pin JTAG target board connector adapter	Lauterbach GmbH
LA-7631	<p>MICTOR 76 (T32 internal connector on LA-7630) to MICTOR-38 adapter</p> <p>This adapter supports 12 MDO signals, and can optionally support 16 MDO signals by adding four 0 Ω resistors.</p>	Lauterbach GmbH
LA-7636	MICTOR 76 (T32 internal connector on LA-7630) to SAMTEC-50 adapter	Lauterbach GmbH
LA-7638	MICTOR-38 to SAMTEC-50 adapter	Lauterbach GmbH
LFVDBJR	<p>VertiCal debug board with JTAG / MICTOR connector interface, rigid PCB (lead-free)</p> <p>VertiCal Lead Free Debug Interface board which consists of a VertiCal Male interface on the secondary side and a VertiCal Female interface on the primary side, allowing the user to connect to any VertiCal-based development tool. Debug tool interface is facilitated by both a 2x7 pin JTAG header and MICTOR connector interface on the primary side. The LFVDBJR is implemented with a rigid PCB.¹</p>	Freescale Semiconductor
LFVDBJF	<p>VertiCal debug board with JTAG / MICTOR interface, flexible PCB (lead-free)</p> <p>VertiCal lead-free debug interface board which consists of a VertiCal male interface on the secondary side and a VertiCal female interface on the primary side, allowing the user to connect to any VertiCal-based development tool. Debug tool interface is facilitated by both a 2x7 pin JTAG header and MICTOR connector interface on the primary side. The LFVDBJF is implemented with a flexible PCB.¹</p>	Freescale Semiconductor

Table continues on the next page...

Table A-1. Available debug connector adapters (continued)

Part number	Description	Manufacturer
LFVDBGR ²	VertiCal debug board with Robust Nexus 51-pin connector interface, rigid PCB (lead-free) VertiCal lead-free debug interface board which consists of a VertiCal male interface on the secondary side and a VertiCal female interface on the primary side, allowing the user to connect to any VertiCal-based development tool. Debug tool interface is facilitated by a Robust Nexus connector interface on the primary side. The LFVDBGR is implemented with a rigid PCB. ¹	Freescale Semiconductor
LFVDBGF ²	VertiCal debug board with Robust Nexus 51-pin connector interface, flexible PCB (lead-free) VertiCal lead-free debug interface board which consists of a VertiCal male interface on the secondary side and a VertiCal female interface on the primary side, allowing the user to connect to any VertiCal-based development tool. Debug tool interface is facilitated by a Robust Nexus 51-pin connector interface on the secondary side. The LFVDBGF is implemented with a Flexible PCB. ¹	Freescale Semiconductor

1. Works with LFVCALSRAM or any tool with a male VertiCal interface.
2. This adapter only supports a maximum of twelve MDO signals.

Additional information is available at the sources shown in [Table A-2](#).

Table A-2. Adapter manufacturer contact information

Company	Web Link
Freescale Semiconductor	http://www.freescale.com
Lauterbach GmbH	http://www.lauterbach.com
P&E Microcomputer Systems	http://www.pemicro.com

Appendix B Core memory access versus Nexus read/write access

There seems to be much confusion about accessing memory via either the e200zx core or via Nexus read/write access. The Nexus read/write access feature is sometimes referred to as the DMA access. This itself causes confusion because the e200zx devices implement an eDMA module, and on the high-end devices any transfers via the eDMA module can also be traced using the Nexus data trace features of the device.

Core access (by a debugger) is performed by forcing instructions into the e200zx core. Accesses to memory, therefore, are through the cache and the Memory Management Unit (MMU). Memory accesses use the virtual address, which are translated by the MMU to the physical address.

Nexus read/write accesses do not access memory through the core; Nexus read/write accesses bypass both the cache and the MMU. All accesses utilize physical addresses. A Nexus read/write access can be performed while the core is running. This allows a debugger to perform real-time access of variables without stopping the core.

NOTE

On devices with cache, Nexus read/write access will not see changes made by the core to variables or data in the cache, until the cache contents are flushed to memory. Conversely, changes to memory by Nexus read/write access may not be seen by the core, if that area of memory is cached by the CPU.

Nexus read/write access provides a much faster and much more streamlined transfer of blocks of data. A tool initializes read/write start address (RWA), the word transfer size (RWCS[*SZ*]), and the number of transfers (RWCS[*CNT*]) to be performed. The two different paths from the debugger to memory are shown in the following figure. The MCU architecture shown in this figure is based on the MPC5567.

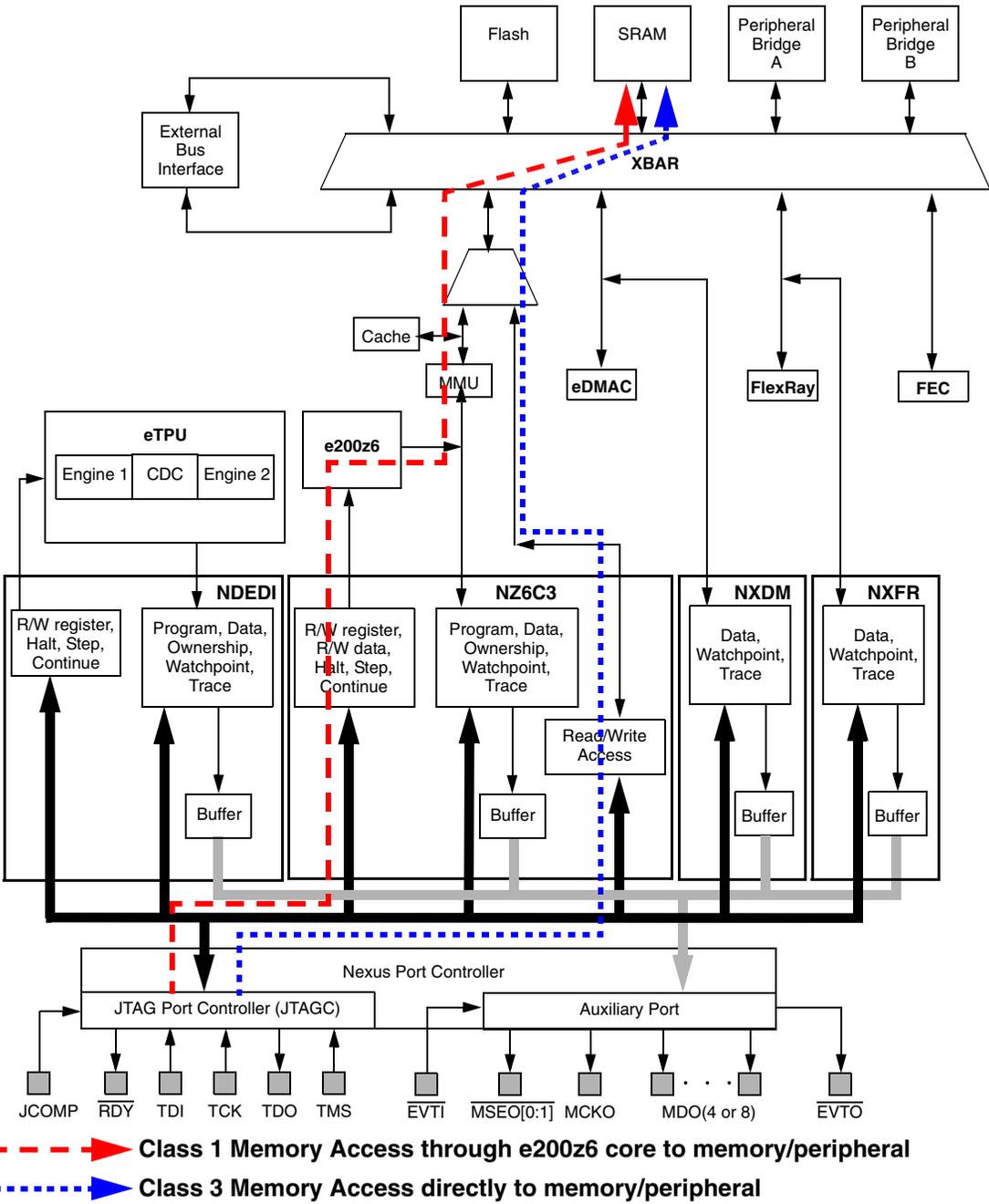


Figure B-1. Core (class 1) versus Nexus class 3 memory access

The sequence for performing a Nexus read/write access is as follows.

1. Enable access to e200zx Nexus.
2. Write address to Nexus Read/Write Access Address register.
3. Write data to Nexus Read/Write Access Data register.
4. Write to Nexus Read/Write Control/Status register to set the size and length of the transfer.

5. Poll the $\overline{\text{RDY}}$ pin (if available) to determine if a single access (when performing a block read or write operation) is complete. If the $\overline{\text{RDY}}$ pin is not available, the Read/Write Access Control register should be polled for the status of the operation.

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