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**Application Note** 

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# MC9S12XHY-Family Demonstration Lab Training

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## 1 Introduction

This publication serves to document demonstration lab software examples. The examples show how to configure and use the modules to users getting started with the MC9S12XHY family of MCUs.

The examples included here illustrate a basic configuration of the modules that allow users to quickly start developing applications.

The complete code is available for all examples. This can be downloaded onto an MC9S12XHY256 target such as the DEMO9S12XHY256 demo board, which this demonstration lab is based on.

Each module of the MC9S12XHY family has its own stand alone software and is discussed within its own section of this document.

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# 2 Setup

### 2.1 Tools setup

#### NOTE

Before starting any of the module examples in this document, it is important to install CodeWarrior<sup>TM</sup> Development Studio and CodeWarrior for Micro-controllers as described in the *DEMO9S12XHY256 Quick Start Guide* which accompanies the demonstration board.

### 2.2 Board setup

The steps listed below provide a basic configuration for each of the module examples in this document. Any deviation from this basic configuration or any specific requirements for a module will be outlined in the relevant module chapter.

- 1. The DEMO9S12XHY256 board must be configured with the default jumper settings as shown in the *DEMO9S12XHY256 Quick Start Guide* that accompanies the demonstration board.
- 2. Connect an A/B USB cable to an open USB port on the host PC and the USB connector on the DEMO9S12XHY256 demonstration board. Follow the on-screen instructions to install the necessary USB drivers if required.
- 3. Move the ON/OFF switch (SW5) to the ON position.
- 4. The green +5 V LED above the ON/OFF switch will illuminate.

# 3 Demonstration Lab Examples

### 3.1 Clocks and reset generator

This lab example shows how to produce PLL based bus clocks using the CRG module in its different modes of operation. The example software initializes the PLL to run in RUN Mode at 4 MHz bus, Run Mode 40 MHz bus, Pseudo Stop 8 MHz bus, and Stop Mode 16 MHz bus clock. The changes in the bus clock can be observed via the pulse rate of LED1 and the frequency can be measured by monitoring the ECLK signal (bus clock) on an oscilloscope.

### 3.1.1 Setup

The following steps must be followed before running the lab example.

- 1. Start CodeWarrior by selecting it in the Windows Start menu.
- 2. From the CodeWarrior main menu, choose File > Open and choose the S12XHY\_CRG\_Demo.mcp file.
- 3. Click Open. The project window then opens.
- 4. C code of this demonstration is contained within the main.c file. Double click on the file to open it.



- 5. From the main menu choose Project > Debug. This compiles the source code, generates an executable file, and downloads it to the demo board.
- 6. A new debugger environment opens. After the download process is finished, close the debugger environment.
- 7. The PLL configuration is sent through the serial communications port on the DEMO9S12XHY256 board (baud rate = 9600, data bits = 8, parity = N, stop bits = 1, flow control = none). Open a terminal window on the PC with this configuration.
- 8. The bus clock speed is represented on pin 59 PH2/ECLK (to accomplish this demonstration code clear the ECLKCTL register and see the MCU reference manual for further information). The ECLK signal is equivalent to the MCU bus speed and can be monitored by attaching an oscilloscope probe to pin 23 of the DS1 header. This signal is not available in J1 header because it is part of the LCD bus.

#### 3.1.2 Instructions

Follow these instructions to run the lab example.

#### Run 4 MHz test

- 1. Press RESET, the MCU is now in run mode with a bus clock frequency of 4 MHz.
- 2. Monitor the ECLK signal on the oscilloscope. The ECLK matches the bus clock frequency, observe the LED pulse rate, and examine the PLL configuration on the terminal window.

#### Run 40 MHz test

- 3. Press RESET while pressing down SW1, make sure to release the RESET switch first. The MCU is now in run mode with a bus clock frequency of 40 MHz.
- 4. Monitor the ECLK signal on the oscilloscope. The ECLK will match the bus clock frequency, observe the LED pulse rate, and examine the PLL configuration on the terminal window.

#### Pseudo stop mode test

- 5. Press RESET while pressing down SW2, make sure to release the RESET switch first. The MCU is now running in Pseudo Stop with a bus clock frequency of 8MHz.
- 6. Monitor the ECLK signal on the oscilloscope. The ECLK will match the bus clock frequency, observe the LED pulse rate, and examine the PLL configuration on the terminal window.
- 7. Press the SW4 button, clock pulses will disappear, and the MCU will restart after WD expires with its default clock configuration (4 MHz bus clock).

#### Stop mode test

- 8. Press RESET while pressing down SW3, make sure to release RESET switch first. The MCU is now running and prepared for stop mode with a bus clock frequency of 16 MHz.
- 9. Monitor the ECLK signal on the oscilloscope. ECLK will match the bus clock frequency. Observe the LED pulse rate and examine the PLL configuration on the terminal window.
- 10. Press the SW4 button, the clock pulses disappear, the MCU enters STOP mode, the bus clock will stop, and the MCU will stay in STOP mode until the RESET switch is pressed.

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### 3.1.3 Summary

The CRG PLL has four operation modes, self-clock mode (which is a fail soft action when the MCU looses the main CLK, see the MCU manual for further information regarding this mode), run mode, pseudo stop, and full stop mode.

For further information on the CRG module, refer to the following documentation available at www.freescale.com.

### 3.2 Flash programming example

The flash technology module contains program flash (P-flash) and data flash (D-flash). P-Flash is intended primarily for non-volatile code storage. D-Flash is used as basic flash memory for non-volatile data storage or non-volatile storage to support emulated EEPROM or a combination of both. The user interfaces with this module via the following steps.

- 1. Set the flash clock divider (FCLKDIV)
- 2. Check the status of the Flash status register (FSTAT)
- 3. Make sure the command complete interrupt flag is set (CCIF=1)
- 4. Launch the appropriate flash commands (program, erase, verify, and so on) via FCCOBIX and FCCOB registers.
- 5. Check flash status register and the CCIF=1.

A flow chart of these steps is shown below Figure 3-1.



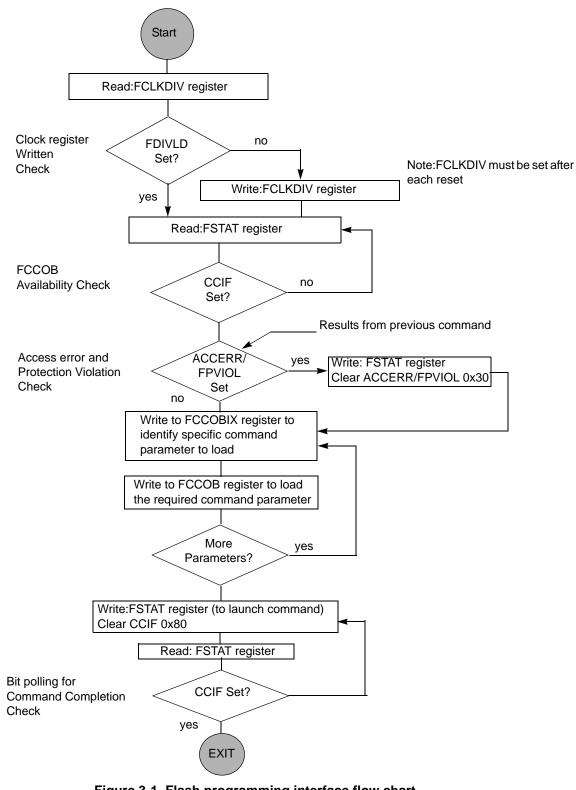


Figure 3-1. Flash programming interface flow chart



#### 3.2.1 Setup

- 1. Start CodeWarrior by selecting it in the Windows Start menu.
- 2. From the CodeWarrior main menu, choose File > Open and choose the S12XHY\_Flash\_Demo.mcp file.
- 3. Click Open. The project window opens.
- 4. The C code of this demonstration is contained within the main.c file. Double click on the file to open it.
- 5. From the main menu choose Project > Debug. This compiles the source code, generates an executable file, and downloads it to the demo board.
- 6. A new debugger environment will open.

#### 3.2.2 Instructions

Notice that this program is compiled and runs from RAM because sections of the flash will be erased in this example. The security information (0x7F\_FF0F) in the flash configuration field is not erased.

#### NOTE

If this is accidently erased the part will be secured and cannot be re-programmed until it is unsecured. For more information on how to unsecure go to the P&E Micro website.

The file of interest is main.c. The purpose of this demonstration is to:

- Launch a flash command
- Demonstrate programming and erasing of flash

This example has been written with a series of user software breakpoint. Therefore, the only thing that has to be done is to press the Run button .

On start-up, the debugger should begin the program in main.

#### 3.2.2.1 Breakpoint 1— Launch flash command—filling P-flash

The importance at this breakpoint is the LaunchFlashCommand function. This function is responsible for exercising the flash block depending upon the flash command given. The flash commands are briefly described in the flash.h header file and within the *S12XHY Reference Manual*.

Stepping through will take the user to the function below Figure 3-2.



/*************************************
Function Name : LaunchFlashCommand
Engineer : b06320 Date : 08/06/09
Arguments :
Return : Notes : This function does not check if the Flash is erased.
This function does not explicitly verify that the data has been
sucessfully programmed
This function must be located in RAM or a flash block not being programmed.
***************************************
tU08 LaunchFlashCommand(char params, tU08 command, tU08 ccob0, tU16 ccob1, tU16 ccob2, tU16 ccob3, tU16 ccob4, tU16 ccob5)
if(FSTAT_CCIF == 1) {
/* Clear any error flags*/ FSTAT = (FPVIOL_MASK   ACCERR_MASK);
/* Write the command id / ccob0 */ FCCOBIX = 0; FCCOBII = command;
FCCOBLO = ccob0;
if(++FCCOBIX != params) {     FCCOB = ccob1:
if(++FCCOBIX != params) {
FCCOB = ccob2; /* Write next data word to CCOB buffer. */ if(++FCCOBIX != params) {
FCCOB = ccob3; /* Write next data word to CCOB buffer. */
if(++FCCOBIX != params) { FCCOB = ccob4: /* Write next data word to CCOB buffer. */
if(++FCCOBIX != params)
FCCOB = ccob5; /* Write next data word to CCOB buffer. */
}
FCCOBIX = parame-1:
/* Clear command buffer empty flag by writing a 1 to it $*/$
/* Liear command buffer empty flag by Writing a 1 to 1t */ FSTAT = CCLF_MASK;
<pre>while (!FSTAT_CCIF) {</pre>
<pre>} return(FSTAT); /* command completed */ }</pre>
<pre>return(FLASH_BUSY); /* state machine busy */ }</pre>

Figure 3-2. (Code Snippet) Launch flash command function

#### 3.2.2.2 Breakpoint 2 — Launched program commands — known data

On entry of the second breakpoint, the memory maps have been set up to show the P-flash being erased (0xFFFF state) then programmed with known parameters (0xAAAA). P-Flash pages from F0 to FB have been filled with 0XAAAA. Consider that the store process, particularly in sectors as big as the P-Flash, may take ~20s to be completed Figure 3-3.

D-flash	P-flash
📟 Memory: 1	Memory: 2
Auto Logical	Auto Logical
000800'L FF FF FF FF FF FF FF FF	008000'L AA AA AA AA AA AA AA AA AA
000808'L FF FF FF FF FF FF FF FF	008008'L AA AA AA AA AA AA AA AA AA
000818'L FF FF FF FF FF FF FF FF	008010'L AA AA AA AA AA AA AA AA AA
000820'L FF FF FF FF FF FF FF FF	008020'L AA AA AA AA AA AA AA AA AA
000828'L FF FF FF FF FF FF FF	008028'L AA AA AA AA AA AA AA AA AA
000830'L FF FF FF FF FF FF FF FF	008030'L AA AA AA AA AA AA AA AA
000838'L FF FF FF FF FF FF FF FF	008038'L AA AA AA AA AA AA AA AA AA
000840'L FF FF FF FF FF FF FF FF	008040'L AA AA AA AA AA AA AA AA AA
000848'L FF FF FF FF FF FF FF FF	008048'L AA AA AA AA AA AA AA AA
000850'L FF FF FF FF FF FF FF FF	008050'L AA AA AA AA AA AA AA AA AA
000858'L FF FF FF FF FF FF FF FF	008058'L AA AA AA AA AA AA AA AA
000860'L FF FF FF FF FF FF FF FF	008060'L AA AA AA AA AA AA AA AA
000868'L FF FF FF FF FF FF FF FF	008068'L AA AA AA AA AA AA AA AA AA
000870'L FF FF FF FF FF FF FF FF	008070'L AA AA AA AA AA AA AA AA AA
000878'L FF FF FF FF FF FF FF FF	008078'L AA AA AA AA AA AA AA AA AA
000880'L FF FF FF FF FF FF FF FF	008080'L AA AA AA AA AA AA AA AA AA
000888'L FF FF FF FF FF FF FF FF	008088'L AA AA AA AA AA AA AA AA AA
000898'L FF FF FF FF FF FF FF FF	008090'L AA AA AA AA AA AA AA AA AA
0008A0'L FF FF FF FF FF FF FF FF	0080A0'L AA AA AA AA AA AA AA AA AA
0008A8'L FF FF FF FF FF FF FF FF	0080A8'L AA AA AA AA AA AA AA AA AA
0008B0'L FF FF FF FF FF FF FF FF	0080BO'L AA AA AA AA AA AA AA AA AA
0008B8'L FF FF FF FF FF FF FF	0080B8'L AA AA AA AA AA AA AA AA
0008C0'L FF FF FF FF FF FF FF	0080CO'L AA AA AA AA AA AA AA AA
0008C8'L FF FF FF FF FF FF FF FF	0080C8'L AA AA AA AA AA AA AA AA AA
0008D0'L FF FF FF FF FF FF FF FF	0080DO'L AA AA AA AA AA AA AA AA
0008D8'L FF FF FF FF FF FF FF FF	0080D8'L AA AA AA AA AA AA AA AA
0008E0'L FF FF FF FF FF FF FF FF	0080EO'L AA AA AA AA AA AA AA AA
지지 지지 지지 지지 지지 지지 지지 NR NNNN	א גע גע גע גע גע גע די איז א און אין 🗹
📰 Register	
HC12	Auto
D O A O B	0
	1.0
IP 3115 PC 3115 PPA(	
	SXHINZVC
EPAGE   0 GPAGE   F DIRI	ECT   0 RPAGE   FD
	na and meansmine. D Flack filled with 0x44444 usi

Figure 3-3. The memory maps real time erasing and programming, P-Flash filled with 0xAAAA values

The P-flash window (0x8000 to 0xBFFF) shows 16 K of the P-Flash content, to navigate through all programmed pages change the PPAGE index. Programmed pages in this example are F0 to FB.

The D-flash window (0x0800 to 0x0BFF) shows 1 K of the D-Flash, navigation through the D-Flash's 8 K space is possible by changing EPAGE index from 0 to 7 (8 1K pages) (Figure 3-4).



🔳 Register		
HC12		Auto
D 0	A 0	в 0
IX CO	IY 2	
IP 3312	PC 3312	PPAGE FO
SP 20FB	IPL 0	CCR SXHINZVC
EPAGE 0	GPAGE F	DIRECT O RPAGE FD

Figure 3-4. Changing P and D flash page indexes

### 3.2.2.3 Breakpoint 3 — Launched program commands — address data

The store procedure is the same as in previous step, except the data being written to the P-flash is different. The data written is the actual addresses of the P-flash (Figure 3-5).

D-flash			P-fla	ash		
Memory: 1		Memory: 2			-	
Auto	Logical				Auto Lo	gical
000800'L FF FF FF FF FF FF FF FF	🔺	008000'L 00	00 00 02 00	04 00 06		~
000808'L FF FF FF FF FF FF FF FF		1. No. 2. 2. 2. 2. 2. 2. 2. 2. 2. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1.				
000810'L FF FF FF FF FF FF FF FF		008010'L 00	10 00 12 00	14 00 16		
000818'L FF FF FF FF FF FF FF FF		008018'L 00	18 <mark>00</mark> 1A 00	1C <mark>00</mark> 1E		
000820'L FF FF FF FF FF FF FF FF		008020'L <mark>00</mark>	20 00 22 00	24 00 26	".\$.&	
000828'L FF FF FF FF FF FF FF FF					. (.*.,	
000830'L FF FF FF FF FF FF FF FF			30 00 32 00		.0.2.4.6	
000838'L FF FF FF FF FF FF FF FF		7.57.787.787.87			.8.:.<.>	
000840'L FF FF FF FF FF FF FF FF		C. M. C. S. C. Starting and Street	40 00 42 00		.@.B.D.F	
000848'L FF FF FF FF FF FF FF FF			48 00 4A 00		.H.J.L.N	
000850'L FF FF FF FF FF FF FF FF			50 00 52 00		.P.R.T.V	
000858'L FF FF FF FF FF FF FF FF		A CONTRACTOR OF A CONTRACTOR OF A CONTRACTOR OF A CONTRACTOR OF A CONTRACTOR A CONTRACTOR A CONTRACTOR A CONTRA	58 00 5A 00		.X.Z.\.^	
000860'L FF FF FF FF FF FF FF FF			60 00 62 00		. b.d.f	
000868'L FF FF FF FF FF FF FF FF			68 00 6A 00		.h.j.l.n	
000870'L FF FF FF FF FF FF FF FF				74 00 76	.p.r.t.v	
000878'L FF FF FF FF FF FF FF FF			78 00 7A 00 80 00 82 00		.x.z. .~	
000880'L FF FF FF FF FF FF FF FF 000888'L FF FF FF FF FF FF FF FF		1. No. 2. State (1996) ***********************************	88 00 8A 00		*******	
000880°L FF FF FF FF FF FF FF FF FF		Contraction of the second second	90 00 92 00			
000898'L FF FF FF FF FF FF FF FF		Contraction of the state of the state	98 00 92 00 98 00 9A 00			
0008A0'L FF FF FF FF FF FF FF FF		A CONTRACTOR OF A CONTRACTOR A CONTRA	A0 00 A2 00			
0008A8'L FF FF FF FF FF FF FF FF		Constant and an an an an an	A8 00 AA 00			
0008B0'L FF FF FF FF FF FF FF FF			B0 00 B2 00			
0008B8'L FF FF FF FF FF FF FF		[14] 20 19 20 20 20 20 20 20 20 20 20 20 20 20 20	B8 00 BA 00			
0008CO'L FF FF FF FF FF FF FF FF		12.13.24.26.25.26.26.7 State	CO 00 C2 00			
0008C8'L FF FF FF FF FF FF FF FF		1 1 1 1 2 2 2 2 2 2 1 2 2 2 2 2 2 2 2 2	C8 00 CA 00			
0008D0'L FF FF FF FF FF FF FF FF		0080D0'L 00	DO 00 D2 00	D4 <mark>00</mark> D6		
0008D8'L FF FF FF FF FF FF FF FF		0080D8'L 00	D8 00 DA 00	DC <mark>OO</mark> DE		
0008E0'L FF FF FF FF FF FF FF FF		0080E0'L 00	E0 00 E2 00	E4 <mark>00</mark> E6		
वन वन वन वन वन वन वन ता 18780000	<u> </u>	ດດຂດສຸຊານ. ດດ	F8 00 FA 00	नन <mark>00</mark> 1न		×
I Re	gister					
HC12	2			Auto		
		D P	0	, ion o		
D	0 A	0 B	U U			
IX	CO IY	2				
	3312 PC :	3312 PPAGE	FO			
SP	20FB IPL	0 CCR S	SXHINZVC			
EPAG	E O GPAGE	F DIRECT	T O RPAGE	FD		
	111	1//		9-24		

Figure 3-5. Address values stored in P-flash



### 3.2.2.4 Breakpoint 4 — D-flash — launched program commands

The same functions are used but now they perform activity on the D-flash. The only differences to the flash command function are the memory addresses issued and flash commands, that is D-flash instead of P-flash.

The end of the demonstration is indicated by the LEDs on the evaluation board (EVB) being toggled.

This example does not re-program the device to default, this happens on the next re-load of a program by allowing NVM erasing.

#### 3.2.3 Summary

The demonstration software has shown how to initialize the flash command to perform programming, erasing, and erase verify on both the P-flash and D-flash. It is vital that the flow diagram is followed for correct operation. Deviation from this could cause errors when working with the P/D-flash. Although this demonstration did not include it, it is good practice to verify that the correct data has been programmed to the flash.

### 3.3 Emulated EEPROM driver

The electrically erasable programmable read only memory (EEPROM), which can be byte or word programmed and erased is often used in automotive electronic control units. This flexibility for program and erase operations make it suitable for data storage of application variables that must be maintained when power is removed, and needs to be updated individually during run-time. For the devices without EEPROM memory, the page-erasable flash memory can be used to emulate for EEPROM through EEPROM emulation software.

The EEPROM emulation driver for the S12XHY implements the fixed-length data record scheme emulation on a split gate flash. The emulated EEPROM functionalities are organizing data records, initializing and de-initializing EEPROM, and reporting EEPROM status reading and writing data records.

Four or more sectors will be involved in emulation with a round robin scheduling scheme.

#### 3.3.1 Setup

- 1. Start CodeWarrior by selecting it in the Windows Start menu.
- 2. From the CodeWarrior main menu, choose File > Open and choose the S12XHY\_EEE\_Demo.mcp file.
- 3. Click Open. The project window opens.
- 4. The C code of this demonstration is contained within the NormalDemo.c file. Double click on the file to open it.
- 5. From the main menu choose Project > Debug. This compiles the source code, generates an executable file, and downloads it to the demo board.
- 6. A new debugger environment opens.



### 3.3.2 Instructions

The file of interest is NormalDemo.c where the main function resides. The purpose of this demonstration is to show how:

- The D-flash is initialized for EEE
- The active and alternative sectors are assigned
- The active sector is filled and swapped (and erased) with an alternative sector

In an application, only the last point above is of relevance — the D-flash is continually read and written to, sectors would be copied, and swapped and erased. This example has been written with a series of user software breakpoint, therefore the only thing that has to be done is to press the Run button .

On start-up, the debugger should begin the program in main as shown in Figure 3-6.

```
void main(void)
{
    UINT16 returnCode;
    UINT16 readAddr;
    UINT16 erasingCycles;
    UINT16 temp[EED_DATA_VALUE_SIZE/EED_MIN_PROG_SIZE] = { > 0,0,0 < };
    UINT18 i,j;</pre>
```

#### Figure 3-6. Main function

#### 3.3.2.1 Breakpoint 1 — Erase the D-flash

```
/* This erases the D-Flash sectors used for EED. The entire emulated EEPROM
from EED_FLASH_START_ADDRESS to EED_FLASH_END_ADDRESS is erased. */
asm_BGND;
/* User breakpoint1 - the function below will erase the D-flash */
returnCode = FSL_DeinitEeprom();
if (EED_OK != returnCode)
{
[...]
/* Wait until DeinitEeprom is done */
while(BUSY_== EE_Status)
...]
```

#### Figure 3-7. Breakpoint 1

When selecting the run button, the first software breakpoint is reached. Breakpoint 1 stops at the function responsible for initializing the D-flash. This function erases and assigns the physical D-flash which is used for EEE. Notice that the selected D-flash (0x800, 0x900, 0xA00, 0xB00) is in the erased state.



# NP

#### 3.3.2.2 Breakpoint 2 — Initialize the active and alternative sectors

```
returnCode = FSL_InitEeprom();  /* initilise EEPROM */
/* Hit run to the next software breakpoint, where first record will be written */
if (EED_OK != returnCode)
{
    ErrorTrap();
    FrorTrap();
    while (BUSY == EE_Status)
    {
    FSL_Main();
    FSL_Main();
}
```

#### Figure 3-8. Breakpoint 2

The D-flash has now been erased and has to be arranged as active and alternative sectors. This software driver requires that at least 2 alternative sectors be available. This deals with any brownout or dead sector situations. The FSL\_InitEeprom function initializes the two sectors at location 0x100000 and 0x100100 to *active* and the remaining sectors 0x100200, 0x100300, and 0x100400 to *alternative*. On completion, the active sectors are defined by 0xFACF0000 and the alternative sectors are defined by 0xFFFF0000.

The active sectors are displayed on the memory windows as follows (Table 3-1).

Window	EPAGE	Local Map	Global Address
Memory:1	0	0x800	0x100000
Memory:2	0	0x900	0x100100
Memory:3	0	0xA00	0x100200
Memory:4	0	0xB00	0x100300
Memory:1	1	0x800	0x100400

#### Table 3-1. Active sectors on memory windows

#### NOTE

For being able to see the content of the 0x100400 alternative record change the EPAGE register on the Register window as indicated on Figure 3-9.



Memory:1	Memory:2		Memory:3	<u>_   ×</u>	Memory:4	
Auto		Auto Lo		Auto		Auto
000800'L FA CF 00 00	000900'L FA CF 00 00	<b>_</b>	000A00'L FF FF 00 00	<b></b>	000B00'L FF FF 00 00	
000804'L FF FF FF FF	000904'L FF FF FF FF		000A04'L FF FF FF FF		000B04'L FF FF FF FF	
000808'L FF FF FF FF	000908'L FF FF FF FF		000A08'L FF FF FF FF		000B08'L FF FF FF FF	
00080C'L FF FF FF FF	00090C'L FF FF FF FF		000A0C'L FF FF FF FF		000B0C'L FF FF FF FF	.
000810'L FF FF FF FF	000910'L FF FF FF FF		000A10'L FF FF FF FF		000B10'L FF FF FF FF	
000814'L FF FF FF FF	000914'L FF FF FF FF		000A14'L FF FF FF FF		000B14'L FF FF FF FF	·
000818'L FF FF FF FF	000918'L FF FF FF FF		000A18'L FF FF FF FF		000B18'L FF FF FF FF	·
00081C'L FF FF FF FF	00091C'L FF FF FF FF		000A1C'L FF FF FF FF		000B1C'L FF FF FF FF	·
000820'L FF FF FF FF	000920'L FF FF FF FF		000A20'L FF FF FF FF		000B20'L FF FF FF FF	
000824'L FF FF FF FF	000924'L FF FF FF FF		000A24'L FF FF FF FF		000B24'L FF FF FF FF	-
000828'L FF FF FF FF 00082C'L FF FF FF FF	000928'L FF FF FF FF		000A28'L FF FF FF FF 000A2C'L FF FF FF FF		000B28'L FF FF FF FF 000B2C'L FF FF FF FF	
	00092C'L FF FF FF FF		000A2C'L FF FF FF FF			
000830'L FF FF FF FF	000934'L FF FF FF FF		000A30 L FF FF FF FF		000B30'L FF FF FF FF	
000838'L FF FF FF FF	000938'L FF FF FF FF		000A38'L FF FF FF FF		000B38'L FF FF FF FF	
00083C'L FF FF FF FF	00093C'L FF FF FF FF		000A3C'L FF FF FF FF		000B3C'L FF FF FF FF	· · ·
000840'L FF FF FF FF	000940'L FF FF FF FF		000A40'L FF FF FF FF		000B40'L FF FF FF FF	
000844'L FF FF FF FF	000944'L FF FF FF FF		000A44'L FR FF FF FF		000B44'L FF FF FF FF J	
000848'L FF FF FF FF	000948'L/FF FF FF FF		000A48'L FF FF FF FF		000B48'L FF FF FF FF	
00084C'L FF FF FF FF	00094C'\$ FF FF FF FF		000A4C'L FF FF FF FF		000B4C'L FF FF FF FF	
000850'L FF FF FF FF	000950 /L FF FF FF FF		000A50'L FF FF FF FF		000B50'L FF FF FF FF	
000854'L FF FF FF FF \	000954/L FF FF FF FF		000A54'L FF FF KF FF		000B54'L FF FF FF FF	·
000858'L FF FF FF FF \	000958'L FF FF FF FF		000A58'L FF FF FF FF		000B58'L FF FF FF FF	·
00085C'L FF FF FF FF	0009\$C'L FF FF FF FF		000A5C'L FF FF FF FF		000B5C'L FF FF FF FF	·
000860'L FF FF FF FF	000960'L FF FF FF FF	_	000A60'L FF FF FF FF		000B60'L FF FF FF FF	·
000864'L FF FF FF FF	000964'L FF FF FF FF	<u> </u>	000A64'L FF FF FF FF	-	000B64'L AF FF FF FF	·



Alternative sectors

📰 Register		
HC12		Auto
D 3	A 0	B 3
IX 20F2	IY 20F6	
IP FE80D7	PC 80D7	PPAGE FE
SP 20EF	IPL 0	CCR SXHINZVC
EPAGE 0	GPAGE F	DIRECT 0 RPAGE FD

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Memory:1	Memory:2	Memory:3	Memory:4
Auto	Auto Lo	Auto	Auto
000800'L FF FF 00 00	000900'L FF FF FF FF	000A00'L FF FF FF FF	OOOBOO'L FF FF FF FF
000804'L FF FF FF FF	000904'L FF FF FF FF	000A04'L FF FF FF FF	000B04'L FF FF FF FF
000808'L FF FF FF FF	000908'L FF FF FF FF	000A08'L FF FF FF FF	1000B08'L FF FF FF FF
00080C'L FF FF FF FF	00090C'L FF FF FF FF	OOOAOC'L FF FF FF FF	000B0C'L FF FF FF FF
000810'L FF FF FF FF	000910'L FF FF FF FF	000A10'L FF FF FF FF	000B10'L FF FF FF FF
000814'L FF FF FF FF	000914'L FF FF FF FF	000A14'L FF FF FF FF	000B14'L FF FF FF FF
000818'L FF FF FF FF	000918'L FF FF FF FF	000A18'L FF FF FF FF	000B18'L FF FF FF FF
00081C'L FF FF FF FF	00091C'L FF FF FF FF	OOOA1C'L FF FF FF FF	000B1C'L FF FF FF FF
000820'L FF FF FF FF	000920'L FF FF FF FF	000A20'L FF FF FF FF	000B20'L FF FF FF FF
000824'L FF FF FF FF		000A24'L FF FF FF FF	000B24'L FF FF FF FF
000828'L FF FF FF FF	II	000A28'L FF FF FF FF	000B28'L FF FF FF FF
00082C'L FF FF FF FF	II	000A2C'L FF FF FF FF	000B2C'L FF FF FF FF
000830'L FF FF FF FF		000A30'L FF FF FF FF	000B30'L FF FF FF FF
000834'L FF FF FF FF		000A34'L FF FF FF FF	000B34'L FF FF FF FF
000838'L FF FF FF FF	II	000A38'L FF FF FF FF	000B38'L FF FF FF FF
00083C'L FF FF FF FF	II	OOOA3C'L FF FF FF FF	000B3C'L FF FF FF FF
000840'L FF FF FF FF		000A40'L FF FF FF FF	000B40'L FF FF FF FF
000844'L FF FF FF FF		000A44'L FF FF FF FF	000B44'L FF FF FF FF
000848'L FF FF FF FF		000A48'L FF FF FF FF	000B48'L FF FF FF FF
00084C'L FF FF FF FF		000A4C'L FF FF FF FF	000B4C'L FF FF FF FF
000850'L FF FF FF FF		000A50'L FF FF FF FF	000B50'L FF FF FF FF
000854'L FF FF FF FF		000A54'L FF FF FF FF	000B54'L FF FF FF FF
000858'L FF FF FF FF		000A58'L FF FF FF FF	000B58'L FF FF FF FF
00085C'L FF FF FF	II	OOOA5C'L FF FF FF FF	000B5C'L FF FF FF FF
000860'L FF FF FF FF		000A60'L FF FF FF FF	000B60'L FF FF FF FF
000864'L FF FF FF FF	000964'L FF FF FF FF	000A64'L FF FF FF FF	000B64'L FF FF FF FF

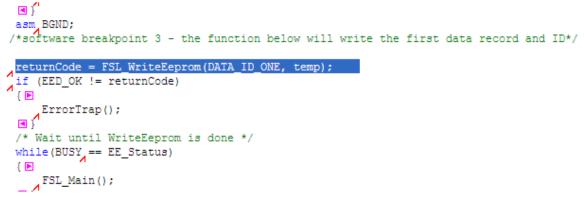
Alternative sector

🚟 Register		
HC12		Auto
D 3	A 0	В 3
IX 20F2	IY 20F6	
IP FE80D7	PC 80D7	PPAGE FE
SP 20EF	IPL 0	CCR SXHINZVC
EPAGE 1	GPAGE F	DIRECT O RPAGE FD

Figure 3-9. EPAGE register change



#### 3.3.2.3 Breakpoint 3 — Write first data and ID record



#### Figure 3-10. Breakpoint 3

The data to be written is defined within a header file (Figure 3-11) – 0x10. This function when executed writes the data 0x10 and assigns this with a record ID of 0x01. The ID size is 2 bytes and the data size has been configured to 6 bytes. The specific EEE User Guide explains how to set the data size.

	C Memory	y:1					
						Auto	1
	000800'L	FA CF	00	00			1
Data Record	000804'5						1
	000808'L				<u> </u>		ID Record
	000800'L			FF			1
	000810'L			FF			1
		FF FF		FF			1
	000818'L	FF FF	FF	FF			1
	00081C'L	FF FF	FF	FF			1
	000820'L	FF FF	FF	FF			1
	000824'L	FF FF	FF	FF			1
	000828'L	FF FF	FF	FF			1
	00082C'L	FF FF	FF	FF			1
	000830'L	FF FF	FF	FF			1
	000834'L	FF FF	FF	FF			1
	000838'L	FF FF	FF	FF			1
	00083C'L	FF FF	FF	FF			1
	000840'L	FF FF	FF	FF			1
	000844'L	FF FF	FF	FF			1
	000848'L	FF FF	FF	FF			1
	00084C'L	FF FF	FF	FF			1
	000850'L	FF FF	FF	FF			1
	000854'L	FF FF	FF	FF			1
	000858'L	FF FF	FF	FF			1
	00085C'L			FF			1
	000860'L			FF			1
	000864'L	FF FF	FF	FF		<u> </u>	

Figure 3-11. Header file content



#### 3.3.2.4 Breakpoint 4 — Completely write the active sectors

```
asm_BGND;
/* software breakpoint 4 - the first record has been written and the function below will write t
/* It will loop here until all the active sectors are filled*/
for (i = DATA_ID_ONE_; i <= EED_MAX_RECORD_NUMBER; i++)
{ [b]
for (j = 0; j < (EED_DATA_VALUE_SIZE/EED_MIN_PROG_SIZE) ; j++)
{ [b]
temp[j] = i + DATA_VALUE;
]
returnCode = FSL_WriteEeprom(i, temp);
if (EED_OK != returnCode)
{ [b]
```

#### Figure 3-12. Breakpoint 4

This writes data records so that the active block is completely filled. The next write after the loop causes a swap. The active sectors at 0x800 and 0x900 have been filled because the code executes a loop until it reaches the end of the second active sector.



Figure 3-13. Sector filling

### 3.3.2.5 Breakpoint 5 — Sector swap

Now that the active sectors have been completely filled, the next record write only occurs after a new active sector has been created. This is a two-stage process. First, all the records from the first active sector are copied to the first available alternative sector, in this case, data and ID records from 0x800-0x899 are



copied to 0xA00. Second, the sector at 0x800 is erased and becomes a new alternative sector. Notice that on the new alternative sector it begins with 0xFFFF0001.

E Memory:1	- 🗆 🗵	Memory:2	_O×	Memory:3	- 🗆 🗵	E Memory:4	
	Auto		Auto Le		Auto		Auto
000800'L FF FF 00 01		000900'L FA CF 00 00		0000A00'L FA CF 00 00		000B00'L FF FF 00 00	
000804'L FF FF FF FF		000904'L 00 2F 00 2F ././		000A04'L 00 11 00 11		000B04'L FF FF FF FF	
000808'L FF FF FF FF		000908'L 00 2F 00 1F ./		000A08'L 00 11 00 01		000B08'L FF FF FF FF	
00080C'L FF FF FF FF		00090C'L 00 30 00 30 .0.0		000A0C'L 00 12 00 12		OOOBOC'L FF FF FF FF	
000810'L FF FF FF FF		000910'L 00 30 00 20 .0.		000A10'L 00 12 00 02		000B10'L FF FF FF FF	
000814'L FF FF FF FF		000914'L 00 31 00 31 .1.1		000A14'L 00 13 00 13		000B14'L FF FF FF FF	
000818'L FF FF FF FF		000918'L 00 31 00 21 .1.!		000A18'L 00 13 00 03		000B18'L FF FF FF FF	
00081C'L FF FF FF FF		00091C'L 00 32 00 32 .2.2		000A1C'L 00 14 00 14		000B1C'L FF FF FF FF	
000820'L FF FF FF FF		000920'L 00 32 00 22 .2."		000A20'L 00 14 00 04		000B20'L FF FF FF FF	
000824'L FF FF FF FF		000924'L 00 33 00 33 .3.3		000A24'L 00 15 00 15		000B24'L FF FF FF FF	
000828'L FF FF FF FF		000928'L 00 33 00 23 .3.#		000A28'L 00 15 00 05\		000B28'L FF FF FF FF	
00082C'L FF FF FF FF		00092C'L 00 34 00 34 .4.4		000A2C'L 00 16 00 16		000B2C'L FF FF FF FF	
000830'L FF FF FF FF		000930'L 00 34 00 24 .4.\$		000A30'L 00 16 00 06 \		000B30'L FF FF FF FF	
000834'L FF FF FF FF		000934'L 00 35 00 35 .5.5		000A34'L 00 17 00 17 \		000B34'L FF FF FF FF	
000838'L FF FF FF FF		000938'L 00 35 00 25 .5.%		000A38'L 00 17 00 07 \		000B38'L FF FF FF FF	
00083C'L FF FF FF FF		00093C'L 00 36 00 36 .6.6		000A3C'L 00 18 00 18		000B3C'L FF FF FF FF	
000840'L FF FF FF FF		000940'L 00 36 00 26 .6.«		000A40'L 00 18 00 08		000B40'L FF FF FF FF	
000844'L FF FF FF FF		000944'L 00 37 00 37 .7.7		000A44'L 00 19 00 19		000B44'L FF FF FF FF	
000848'L FF FF FF FF		000948'L 00 37 00 27 .7.'		000A48'L 00 19 00 09		000B48'L FF FF FF FF	
00084C'L FF FF FF FF		00094C'L 00 38 00 38 .8.8		000A4C'L 00 1A 00 1A		000B4C'L FF FF FF FF	
000850'L FF FF FF FF		000950'L 00 38 00 28 .8.(		000A50'L 00 1A 00 0A		000B50'L FF FF FF FF	
000854'L FF FF FF FF		000954'L 00 39 00 39 .9.9		000A54'L 00 1B 00 1B		000B54'L FF FF FF FF	
000858'L FF FF FF FF		000958'L 00 39 00 29 .9.)		000A58'L 00 1B 00 0B		000B58'L FF FF FF FF	
00085C'L FF FF FF FF		00095C'L 00 3A 00 3A		000A5C'L 00 1C 00 1C \		000B5C'L FF FF FF FF	
000860'L FF FF FF FF		000960'L 00 3A 00 2A .:.*		000A60'L 00 1C 00 0C \		000B60'L FF FF FF FF	
000864'L FF FF FF FF	-	000964'L 00 3B 00 3B .;.;	-	000A64'L 00 1D 00 1D		000B64'L FF FF FF FF	· ·

Old active sector now becomes alternative

**Records** copied

#### Figure 3-14. Sector SWAP

The process described where the sectors are being filled, copied, and erased will continue through an application, for example such as an odometer. When power to the application is lost, the data is stored in the D-flash and is easily read.

#### 3.3.2.6 Breakpoint 6 — Reading EEE and erase

```
asm_BGND;
/* software breakpoint 6 - Active sector swapped. The code below will read and then re-program the
/* This reads the data with Data ID 0x01. The record is read from the cache table if EED_CACHETABLE
returnCode=FSL_ReadEeprom(DATA_ID_ONE, &readAddr);
if (EED_OK != returnCode)
{
ErrorTrap();
}
else
{
ErrorTrap();
}
For(_i = 0;i < EED_DATA_VALUE_SIZE ;_i+=EED_MIN_PROG_SIZE)
{
Error3-15 Breakpoint 6
```

#### Figure 3-15. Breakpoint 6

Functions after breakpoint 6 read a specific EEE address from the stored data tables.

This demonstration program completes by erasing the D-flash sectors and ends while in the loop.



Memory:1	. D × D	Memory:2		Memory:3		Memory:4	
Aul	ito 🗌		Auto Le		Auto		Auto
000800'L FF FF FF FF		000900'L FF FF FF FF		000A00'L FF FF FF FF		000B00'L FF FF FF FF	
000804'L FF FF FF FF		000904'L FF FF FF FF		000A04'L FF FF FF FF		000B04'L FF FF FF FF	
000808'L FF FF FF FF		000908'L FF FF FF FF		000A08'L FF FF FF FF		000B08'L FF FF FF FF	
00080C'L FF FF FF FF		00090C'L FF FF FF FF		OOOAOC'L FF FF FF FF		OOOBOC'L FF FF FF FF	
000810'L FF FF FF FF		000910'L FF FF FF FF		000A10'L FF FF FF FF		000B10'L FF FF FF FF	
000814'L FF FF FF FF		000914'L FF FF FF FF		000A14'L FF FF FF FF		000B14'L FF FF FF FF	
000818'L FF FF FF FF		000918'L FF FF FF FF		000A18'L FF FF FF FF		000B18'L FF FF FF FF	
00081C'L FF FF FF FF		00091C'L FF FF FF FF		OOOA1C'L FF FF FF FF		000B1C'L FF FF FF FF	
000820'L FF FF FF FF		000920'L FF FF FF FF		000A20'L FF FF FF FF		000B20'L FF FF FF FF	
000824'L FF FF FF FF		000924'L FF FF FF FF		000A24'L FF FF FF FF		000B24'L FF FF FF FF	
000828'L FF FF FF FF		000928'L FF FF FF FF		000A28'L FF FF FF FF		000B28'L FF FF FF FF	
00082C'L FF FF FF FF		00092C'L FF FF FF FF		000A2C'L FF FF FF FF		000B2C'L FF FF FF FF	
000830'L FF FF FF FF		000930'L FF FF FF FF		000A30'L FF FF FF FF		000B30'L FF FF FF FF	
000834'L FF FF FF FF		000934'L FF FF FF FF		000A34'L FF FF FF FF		000B34'L FF FF FF FF	
000838'L FF FF FF FF		000938'L FF FF FF FF		000A38'L FF FF FF FF		000B38'L FF FF FF FF	
00083C'L FF FF FF FF		00093C'L FF FF FF FF		OOOA3C'L FF FF FF FF		000B3C'L FF FF FF FF	
000840'L FF FF FF FF		000940'L FF FF FF FF		000A40'L FF FF FF FF		000B40'L FF FF FF FF	
000844'L FF FF FF FF		000944'L FF FF FF FF		000A44'L FF FF FF FF		000B44'L FF FF FF FF	
000848'L FF FF FF FF		000948'L FF FF FF FF		000A48'L FF FF FF FF		000B48'L FF FF FF FF	
00084C'L FF FF FF FF		00094C'L FF FF FF FF		000A4C'L FF FF FF FF		000B4C'L FF FF FF FF	
000850'L FF FF FF FF		000950'L FF FF FF FF		000A50'L FF FF FF FF		000B50'L FF FF FF FF	
000854'L FF FF FF FF		000954'L FF FF FF FF		000A54'L FF FF FF FF		000B54'L FF FF FF FF	
000858'L FF FF FF FF		000958'L FF FF FF FF		000A58'L FF FF FF FF		000B58'L FF FF FF FF	
00085C'L FF FF FF FF		00095C'L FF FF FF FF		OOOA5C'L FF FF FF FF		000B5C'L FF FF FF FF	
000860'L FF FF FF FF		000960'L FF FF FF FF		000A60'L FF FF FF FF		000B60'L FF FF FF FF	
000864'L FF FF FF FF		000964'L FF FF FF FF	-	000A64'L FF FF FF FF	•	000B64'L FF FF FF FF	•

Figure 3-16. EEE data read

### 3.3.3 Summary

The demonstration software has shown how to initialize the D-flash for EEE operation by producing active and alternative sectors via the FSL\_InitEeprom function. The functions for writing FSL\_WriteEeprom and reading FSL\_ReadEeprom are required to write/read the appropriate data and accompanying ID records and hence emulate EEPROM. In an application it is the two latter functions that are relied upon. Moreover, the software is capable of dealing with brownout events as well as dead sectors. For developing applications with this code read the *EEE Driver User's Guide* included in this pack.

### 3.4 MSCAN Module

This lab example uses the MSCAN module in loopback mode to transmit and receive a byte of data using standard length identifiers and four 16-bit filters. The status of the four switches, SW1 to SW4, is read and transmitted by the MSCAN module. When the MSCAN module receives its own transmission, the data in the message is read and displayed on the four LEDs.

When the MSCAN module is operated in loopback mode no CAN signals are transmitted externally. Both the Tx and Rx pins are held high.

#### 3.4.1 Setup

The following steps must be followed before running the lab example.

- 1. Start CodeWarrior by selecting it in the Windows Start menu.
- 2. From the CodeWarrior main menu, choose File > Open and choose the S12XHY\_MSCAN\_Demo.mcp file.
- 3. Click Open. The project window opens.



- 4. The C code of this demonstration is contained within the main.c file. Double click on the file to open it.
- 5. From the main menu choose Project > Debug. This compiles the source code, generates an executable file, and downloads it to the demo board.
- 6. A new debugger environment will open. After the download to the demo board is complete, close the debugger environment.

#### 3.4.2 Instructions

Follow these instructions to run the lab example.

- 1. Press RESET. The MSCAN demo software begins execution.
- 2. Press various combinations of the SW1, SW2, SW3, and SW4 switches. The LEDs must match their configuration.

#### 3.4.3 Summary

The MSCAN module is a serial data bus communication controller implementing the CAN 2.0A/B protocol as defined in the Bosch specification dated September 1991. It is not limited to automotive applications and is suited to a wide variety of uses that require reliable communications.

### 3.5 PWM module

This lab provides an example of how to setup and use the pulse width modulation (PWM) module to create a 50% duty cycle output with different polarity and alignment settings. This behavior is best illustrated if all of the PWM signals can be displayed simultaneously on a four channel oscilloscope.

#### 3.5.1 Setup

The following steps must be completed before running the lab example.

- 1. Start CodeWarrior by selecting it in the Windows Start menu.
- 2. From the CodeWarrior main menu, choose File > Open and choose the S12XHY\_PWM\_Demo.mcp file.
- 3. Click Open. The project window will open.
- 4. The C code of this demonstration is contained within the main.c file. Double click on the file to open it.
- 5. From the main menu choose Project > Debug. This compiles the source code, generates an executable file, and downloads it to the demo board.
- 6. A new debugger environment will open. After the download to the demo board is complete, close the debugger environment.



#### 3.5.2 Instructions

To give access to PWM signals on the J1 header, the software re-routes PWM[3:0] from PP[3:0] to PS[7:4].

Follow these instructions to run the lab example

- 1. Press RESET. The code must run and re-route the PWM channels. The PWM module must output 50% duty cycle signals on ports PS7 PS4.
- 2. Try probing all four signals simultaneously if possible. This allows the difference in settings such as center alignment and polarity to be more apparent.

#### 3.5.3 Summary

The PWM is a common module on many microcontrollers. It often finds use in applications that have a need to vary frequency or intensity, such as lighting.

#### 3.6 Low Power Modes

In addition to the default run mode, the MC9S12XHY has three low power modes, wait, pseudo stop and stop.

Wait mode is similar to run mode except that the CPU execution is halted and it is possible to selectively disable some modules so that only necessary modules are clocked.

Self clock mode is used for safety purposes. It provides a reduced functionality in case a loss of clock is causing severe system conditions.

For lower power consumption, pseudo stop mode halts the bus clock, but the external oscillator continues to run.

Stop mode disables the external oscillator for the lowest power consumption.

This lab example shows how to enter each mode and the differences between them.

The table below summarizes the signals present in each mode.

Mode	Bus Clock	External Oscillator
Run	Y	Y
Wait	Y	Y
Self Clock	Y	Y
Pseudo Stop	N	Y
Stop	N	Ν

Table 3-2. Power modes

The changes in the MCU operating mode can be observed via the LEDs and by monitoring the ECLK signal (Bus clock) and EXTAL signal (Crystal) on an oscilloscope.

Care must be taken to probe the ECLK and EXTAL separately to avoid adding extra noise to the signals.

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### 3.6.1 Setup

The steps below must be followed before running the lab example.

- 1. Start CodeWarrior by selecting it in the Windows Start menu.
- 2. From the CodeWarrior main menu, choose File > Open and choose the S12XHY\_Low\_Power\_Modes.mcp file.
- 3. Click Open. The project window will open.
- 4. The C code of this demonstration is contained within the main.c file. Double click on the file to open it.
- 5. From the main menu choose Project > Debug. This compiles the source code, generates an executable file, and downloads it to the demo board.
- 6. A new debugger environment will open. After the download to the demo board is complete, close the debugger environment.
- 7. The bus clock speed is represented on pin 59 PH2/ECLK. The ECLK signal is equivalent to the MCU bus speed and can be monitored by attaching an oscilloscope probe to pin 23 of the DS1, this signal is not available in the J1 header because it is part of the LCD bus.
- 8. The oscillator can be monitored by attaching a scope probe to the EXTAL side of the Y1 crystal.

#### NOTE

If the CLK is monitored in the XTAL, additional noise is input to the device and may cause the MCU not to run properly.

### 3.6.2 Instructions

Follow these instructions to run the lab example:

#### Run mode test

- 1. Press RESET. The MCU is now operating in run mode. The LEDs flash indefinitely indicating the MCU is in run mode.
- 2. Monitor the ECLK signal on the oscilloscope. ECLK represents the bus clock. A 40 MHz signal should be observed.
- 3. Monitor the EXTAL signal on the oscilloscope. The EXTAL indicates that the crystal oscillator is running. An 8 MHz sine wave is observed.

#### Wait mode test

- 1. Press RESET while pressing down SW1 and first release RESET then SW1. LED1 flashes twenty times indicating run mode and then the MCU enters wait mode. Pressing SW4 causes the MCU to exit wait mode and go back into run mode. LED1 flashes twenty times before the MCU returns to wait mode.
- 2. Monitor the ECLK signal on the oscilloscope. The 40 MHz clock signal representing the bus clock is present in both run and wait modes.
- 3. Monitor the EXTAL signal on the oscilloscope. In both run and wait modes, an 8 MHz sine wave is observed indicating that the external oscillator continues to operate in wait mode.



#### Pseudo stop mode test

- 1. Press RESET while pressing down SW2 and first release RESET then SW2. LED1 flashes twenty times indicating run mode and then the MCU enters into pseudo stop mode. Pressing SW4 causes the MCU to exit pseudo stop mode and back into run mode. LED1 flashes twenty times before the MCU returns to pseudo stop mode.
- 2. Monitor the ECLK signal on the oscilloscope. The 40 MHz clock signal representing the bus clock is present in run mode. In pseudo stop mode, the bus clock is stopped to save power.
- 3. Monitor the EXTAL signal on the oscilloscope. In both run and pseudo stop modes, an 8 MHz sine wave is observed indicating that the external oscillator continues to operate in pseudo stop mode.

#### Stop mode test

- 1. Press RESET while pressing down SW3 and first release RESET then SW3. LED1 flashes twenty times indicating run mode and then the MCU enters into stop mode. Pressing SW4 causes the MCU to exit stop mode and back into run mode. LED1 flashes twenty times before the MCU enters and returns into stop mode.
- 2. Monitor the ECLK signal on the oscilloscope. The 40 MHz clock signal representing the bus clock is only present in run mode. In stop mode, the bus clock is stopped to save power.
- 3. Monitor the EXTAL signal on the oscilloscope. The 8 MHz sine wave is only present in run mode. In stop mode, the external oscillator is stopped to save power.

#### 3.6.3 Summary

The MC9S12XHY Family can be configured in a variety of ways to achieve low power consumption. The three low power modes offer different solutions for user applications.

### 3.7 MMC program flash paging window

The MC9S12XHY256 has a flash memory of 256 KB. Because the 256 KB of memory cannot be addressed by the 16-bit MC9S12XHY256 MCU, there is insufficient local addressing space to accommodate all of the flash memory, the RAM memory, and the register space. Instead, a paging system is used which maps 16 KB flash memory blocks, 4 KB RAM memory blocks, and 1 KB Emulated EEPROM memory blocks. The paging system maps the blocks into the local memory map as shown in the next table.

Memory	Local Memory Map Address
EEPROM	0x800 to 0xBFF
RAM	0x1000 to 1FFF
FLASH	0x8000 to 0xBFFF

The MC9S12XHY256 supports Global addressing access. Global addresses are 23 bit addresses that cover an 8 MB address space, ranging from addresses 0x000000 to 0x7FFFFF. In this linear global address space all memory resources are grouped and the GPAGE register can be used to access all RAM, EEPROM, and



FLASH locations, as well as external memory space. See the memory map included in the MC9S12XHY256 Reference Manual.

This lab example shows how to use the paging capability of the MMC module to access global memory addresses within the local memory map. As well as how to use the Global Addressing Access for the different memory resources.

### 3.7.1 Setup

The following steps must be followed before running the lab example

- 1. Start CodeWarrior by selecting it in the Windows Start menu.
- 2. From the CodeWarrior main menu, choose File > Open and choose the S12XHY\_MMC\_Demo.mcp file.
- 3. Click Open. The project window will open.
- 4. The C code of this demonstration is contained within the main.c file. Double click on the file to open it.
- 5. From the main menu choose Project > Debug. This compiles the source code, generates an executable file, and downloads it to the demo board.
- 6. A new debugger environment will open. Do not close the debugger environment.

#### 3.7.2 Instructions

Follow these instructions to run the lab example

1. The Memory:1 window in the debugger environment is configured to show the first few locations of the P-Flash Window at address 0x8000. Note that the P-Flash Memory mapping on this example does not map the pages FF nor FD. This is made intentional due to that the memory locations are non banked. Even though these non banked locations are still accessible by the paging system.

📖 Men	nor	/								
										Auto
08000	00	00	00	00	00	00	00	00		<u> </u>
80080	00	00	00	00	43	00	00	00	c	
08010	00	00	00	00	00	00	00	00		_
08018	00	00	1A	80	80	00	00	00		
08020	00	00	00	00	00	00	09	00		
08028	00	00	00	00	00	00	00	00		
08030	00	00	00	00	5F	OF	03	78	x	
08038	00	80	00	00	00	00	00	00		
08040	00	00	00	00	00	00	00	00		
08048	00	00	00	00	00	00	00	00		-

Figure 3-17. P-Flash window

2. The Register window in the debugger environment shows the setting of the program page index register (PPAGE).



📰 Re	gister		
HC12	2		Auto
D	FE	A 0	B FE
IX	C16C	IY 3030	
IP	C061	PC CO61	PPAGE FE
SP	FFCO	IPL 0	CCR SXHINZVC
EPA6	E 0	GPAGE F	DIRECT 0 RPAGE FD

Figure 3-18. PPAGE register

- 3. Start the software by clicking on the Run button
- 4. When the software reaches the first software breakpoint, examine the contents of the Memory and Register windows. The PPAGE register is set to FE and the P-Flash Window shown in the Memory window displays the contents of PPAGE FE.

📰 Registe	:r												
HC12													Auto
D	FE	A		Γ	0	в			FE				
IX CI	.6C	I	Y	303	30								
IP CO	)61	Р	с	CO	51	PF	AGE	: 1	FE				
SP FF	7C0	I	PL		0	СС	R	SXH	INZVC				
EPAGE	0	G	PAG	E	F	DI	REC	т 🗌	0 RPAGE FD				
🛄 Memor	y:1												
											Auto		Logical
008000'L	46	45	20	50	50	41	47	45	FE PPAGE				
1'800800	20	46	45	20	50	50	41	47	FE PPAG				
008010'L	45	20	46	45	20	50	50	41	E FE PPA				
008018'L	47	45	20	46	45	20	50	50	GE FE PP				
008020'L	41	47	45	20	46	45	20	50	AGE FE P				
008028'L	50	41	47	45	20	46	45	20	PAGE FE				
008030'L	50	50	41	47	45	20	46	45	PPAGE FE				-
	Figure 3-19 PPAGE EE contents												

Figure 3-19. PPAGE FE contents

- 5. Press the Run button and observe the Memory and Register windows at the next breakpoint.
- 6. Now the PPAGE register is set to FC and the P-Flash Window shown in the Memory window displays the contents of PPAGE FC.



📰 Register		_ <b>_ _ _ _ _</b>									
HC12		Auto									
D FC A O	B FC										
IX C16C IY 3030											
IP CO65 PC CO65	PPAGE FC										
SP FFCO IPL 0	CCR SXHINZVC										
EPAGE 0 GPAGE F	DIRECT O RPAGE FD										
Memory:1		_ 🗆 🗵									
		Auto Logical									
008000'L 46 43 20 50 50	41 47 45 FC PPAGE	<b>_</b>									
008008'L 20 46 43 20 50	50 41 47 FC PPAG										
008010'L 45 20 46 43 20	50 50 41 E FC PPA										
008018'L 47 45 20 46 43	20 50 50 GE FC PP										
008020'L 41 47 45 20 46	43 20 50 AGE FC P										
008028'L 50 41 47 45 20	46 43 20 PAGE FC										
008030'L 50 50 41 47 45 20 46 43 PPAGE FC											

- 7. Press the Run button as many times as necessary to reach the PPAGE F0 and observe that every time that you reach a breakpoint the Memory and Register windows are updated accordingly.
- 8. Now, after the PPAGE register is set to F0 and the P-Flash Window shown in the Memory window displays the contents of PPAGE F0.
- 9. The Memory:2 window in the debugger environment is configured to show the first few locations of the RAM Window at address 0x1000. Notice that the RAM Memory mapping in this example maps the pages from FF to FD. The sections that correspond to the pages FF and FE are non banked. Even though these non banked locations are still accessible by the paging system.
- 10. Press the Run button to start running the RPAGE section after reaching the first breakpoint, observe that register RPAGE is set to FF and the contents in Memory:2 are unknown data, this is because this page was not set with information. This page is non banked memory, but it is still accessible through the RAM paging system.

N			

🚟 Register									<u> </u>
HC12									Auto
D FFI	70 A	. [	FF	в	F	0			
IX C17	74 I	Y 30	30						
IP COS	A P	c CO	9A	PPAGE	E F	0			
SP FF0	CO I	PL	0	CCR [	SXHI	ENZVC			
EPAGE	0 G	PAGE	F	DIREC	ст 🗌	0 RPAGE FF			
📖 Memory:									
Memnev:									
	۷								
	2							Auto	
		ad fa	2F 2	7 3D	ЗE	//'=>		Auto	
	2F FB	AD FA BA DB	2F 2 CA 7		3E FA	//'=> n{		Auto	
) 001000'L : 001008'L ;	2F FB	BA DB	CA 7	B 5F				Auto	
) 001000'L : 001008'L ;	2F FB 5E 7F 3C DA	BA DB 8A 7B	CA 7 5D 7	B 5F	FA FF	n{		Auto	
001000'L : 001008'L : 001010'L : 001018'L : 001018'L : 001020'L :	2F FB 5E 7F 3C DA FC F5 01 24	BA DB 8A 7B FF 6F	CA 7 5D 7	B 5F 7 1B 6 9D	FA FF 7F	n{ {]w	1	Auto	
001000'L : 001008'L : 001010'L : 001018'L : 001020'L : 001028'L :	2F FB 5E 7F 3C DA FC F5 01 24 09 20	BA DB 8A 7B FF 6F 00 14 10 84	CA 7 5D 7 67 3 60 3 A0 A	B 5F 7 1B 6 9D 6 10 .6 50	FA FF 7F C2 1B	n{ {]w og6 .\$`6 P.	<u> </u>	Auto	
001000'L : 001008'L ( 001010'L : 001018'L : 001020'L ( 001028'L )	2F FB 5E 7F 3C DA FC F5 01 24 09 20 31 06	BA DB 8A 7B FF 6F 00 14 10 84 22 08	CA 7 5D 7 67 3 60 3 A0 A 09 C	B 5F 7 1B 6 9D 6 10 .6 50 6 44	FA FF 7F C2 1B 0F	n{ {]w og6 .\$`6	<u> </u>	Auto	

Figure 3-21. RPAGE FF Contents

- 11. Press the Run button as many times as necessary to reach the RPAGE FD and observe that every time a breakpoint is reached the Memory and Register windows are updated accordingly.
- 12. Now the RPAGE register is set to FD and the Window shown in the Memory:2 window, displays the contents of RPAGE FD.

🚟 Register	
HC12	Auto
D FDFO A FD B FO	
IX C174 IY 3030	
IP COA2 PC COA2 PPAGE FO	
SP FFCO IPL O CCR SXHINZVC	
EPAGE O GPAGE F DIRECT O RPAGE FD	
	- <b>- ×</b>
	Auto Logical
001000'L 46 44 20 52 50 41 47 45 FD RPAGE	
001000'L 46 44 20 52 50 41 47 45 FD RPAGE	
001000'L 46 44 20 52 50 41 47 45 FD RPAGE 001008'L 20 46 44 20 52 50 41 47 FD RPAG 001010'L 45 20 46 44 20 52 50 41 E FD RPA 001018'L 47 45 20 46 44 20 52 50 GE FD RP	
001000'L 46 44 20 52 50 41 47 45 FD RPAGE 001008'L 20 46 44 20 52 50 41 47 FD RPAG 001010'L 45 20 46 44 20 52 50 41 E FD RPA 001018'L 47 45 20 46 44 20 52 50 GE FD RP 001020'L 41 47 45 20 46 44 20 52 AGE FD R	
001000'L 46 44 20 52 50 41 47 45 FD RPAGE 001008'L 20 46 44 20 52 50 41 47 FD RPAG 001010'L 45 20 46 44 20 52 50 41 E FD RPA 001018'L 47 45 20 46 44 20 52 50 GE FD RP 001020'L 41 47 45 20 46 44 20 52 AGE FD R 001028'L 50 41 47 45 20 46 44 20 PAGE FD	
001000'L 46 44 20 52 50 41 47 45 FD RPAGE 001008'L 20 46 44 20 52 50 41 47 FD RPAG 001010'L 45 20 46 44 20 52 50 41 E FD RPA 001018'L 47 45 20 46 44 20 52 50 GE FD RP 001020'L 41 47 45 20 46 44 20 52 AGE FD R	

Figure 3-22. RPAGE FD contents

13. After the RPAGE register is set to FD and the RAM window, the Memory window displays the contents of RPAGE FD.



- 14. The Memory:3 window in the debugger environment is configured to show the first few locations of the Emulated EEPROM window at address 0x1000. Notice that the Emulated EEPROM Memory mapping in this example maps the pages from 00 to 0F. The sections that correspond to the pages 00 and 0F are banked.
- 15. Press the Run button to start running the EPAGE section after reaching the first breakpoint. Observe, that the EPAGE register is set to 7 and the contents in Memory:3 are EPAGE 07 data.

📟 Register		
HC12		Auto
D FD07 A FD B 7		
IX C174 IY 3030		
IP COA7 PC COA7 PPAGE FO		
SP FFCO IPL O CCR SXHINZVC		
EPAGE 7 GPAGE F DIRECT O RPAGE FD		
Memory:3		- D X
	Auto	Logical
000800'L 30 37 20 45 50 41 47 45 07 EPAGE		
000808'L 20 30 37 20 45 50 41 47   07 EPAG		
000810'L 45 20 30 37 20 45 50 41 E 07 EPA		
000818'L 47 45 20 30 37 20 45 50 GE 07 EP		
000820'L 41 47 45 20 30 37 20 45 AGE 07 E		
000828'L 50 41 47 45 20 30 37 20 PAGE 07		
000830'L 45 50 41 47 45 20 30 37 EPAGE 07		-

Figure 3-23. EPAGE 7 contents

- 16. Press the Run button as many times as necessary to reach the EPAGE 00 and notice that every time the breakpoint is reached the Memory and Register windows are updated accordingly.
- 17. The EPAGE register is now set to 00 in the window shown. The Memory:3 window displays the contents of EPAGE 00.

🚟 Register						
HC12						Auto
D FDO	1 A	FD	в	1		
IX C17	4 IY	D038				
IP COC	3 PC	COC3	PPAGE D	FO		
SP 210	0 IPL	0	CCR SXH	INZVC		
	 0 GPAG	<u> </u>	DIRECT	0 RPAGE FD		
		- , - ,				
🛄 Memory:	3					
					Auto	Logical
1						
, 000800'L 3	30 30 20	45 50	41 47 45	00 EPAGE		<b>_</b>
	30 30 20 20 30 30		41 47 45 50 41 47	00 EPAGE 00 EPAG		▲ _
000808'L 2		20 45				<u>•</u>
000808'L 2 000810'L 4	20 30 30	20 45 30 20	50 41 47	OO EPAG		<b>_</b>
000808'L 2 000810'L 4 000818'L 4 000820'L 4	20 30 30 15 20 30 17 45 20 11 47 45	20 45 30 20 30 30 20 30	50 41 47 45 50 41 20 45 50 30 20 45	OO EPAG E OO EPA GE OO EP AGE OO E		
000808'L 2 000810'L 4 000818'L 4 000820'L 4 000828'L 5	20 30 30 15 20 30 17 45 20	20 45 30 20 30 30	50 41 47 45 50 41 20 45 50	OO EPAG E OO EPA GE OO EP		

Figure 3-24. EPAGE 0 contents

- 18. After the EPAGE register is set to 00 and the EEPROM Window shown. The Memory window displays the contents of EPAGE 00.
- 19. Press the Run button to start running the GPAGE section after reaching the first breakpoint, notice that the GPAGE register is set to 7 and the contents in the Memory:4 window are PPAGE F0 data. The data of window Memory:4 was read from the P-Flash PPAGE F0. This data was accessed using Global addressing.

📰 Register					
HC12					Auto
D F	'F A	0 B	FF		
IX C17	4 IY -	4630			
IP COE	2 PC 1	COE2 PPA	AGE FO		
SP FFC	0 IPL	0 CCR	R SXHINZVC	_	
EPAGE	0 GPAGE	F DIR	ECT 0 RPAGE FD	)	
🛄 Memory:-	4				
Memory:	4			Auto	Logical
	4 46 30 20 -	50 50 41 4	47 45 FO PPAGE	Auto	
	46 30 20 -		47 45 FO PPAGE 41 47 FO PPAG	Auto	
003FC0'L 4 003FC8'L 2 003FD0'L 4	46 30 20 20 46 30 3 45 20 46 3	20 50 50 4 30 20 50 5	41 47 FO PPAG 50 41 E FO PPA	Auto	
003FC0'L 4 003FC8'L 2 003FD0'L 4 003FD8'L 4	46 30 20 20 46 30 3 45 20 46 3 47 45 20 4	20 50 50 4 30 20 50 5 46 30 20 5	41 47 FO PPAG 50 41 E FO PPA 50 50 GE FO PP	Auto	
003FC0'L 4 003FC8'L 2 003FD0'L 4 003FD8'L 4 003FD8'L 4 003FE0'L 4	46 30 20 20 46 30 3 45 20 46 3 47 45 20 4 41 47 45 3	20 50 50 4 30 20 50 5 46 30 20 5 20 46 30 2	41 47 FO PPAG 50 41 E FO PPA	Auto	

Figure 3-25. Global memory addressing access to P-FLASH



20. Press the Run button and the second breakpoint is reached, observe that the GPAGE register is set to 7 and the contents in the Memory:4 window are RPAGE FD data. The data of window Memory:4 was read from the RAM RPAGE FD. This data was accessed using Global addressing.

📰 Register	•					
HC12						Auto
D 1	FF A	0	В	FF		
IX C1	74 IY	4644				
IP C1	01 PC	C101	PPAGE	FO		
SP FF	CO IPL	0	CCR SX	HINZVC		
EPAGE	O GPAG	E F	DIRECT	0 RPAGE FD		
🛄 Memory	:4					
Memory	:4				Auto	
Memory		52 50	41 47 45	FD RPAGE	Auto	
003FCO'L			41 47 45 50 41 47		Auto	
003FC0'L 003FC8'L 003FD0'L	46 44 20 20 46 44 45 20 46	20 52 44 20	50 41 47 52 50 41	FD RPAG E FD RPA	Auto	
003FC0'L 003FC8'L 003FD0'L 003FD8'L	46 44 20 20 46 44 45 20 46 47 45 20	20 52 44 20 46 44	50 41 47 52 50 41 20 52 50	FD RPAG E FD RPA GE FD RP	Auto	
003FC0'L 003FC8'L 003FD0'L 003FD8'L 003FE0'L	46 44 20 20 46 44 45 20 46	20 52 44 20 46 44 20 46	50 41 47 52 50 41	FD RPAG E FD RPA GE FD RP AGE FD R	Auto	

Figure 3-26. Global memory addressing access to RAM

21. Press the Run button and the third breakpoint is reached. Notice that the GPAGE register is set to 7 and the contents in Memory:4 window are EPAGE 00 data.

📰 Register		
HC12		Auto
D FF	A O B	FF
IX C174	IY 3030	
IP C120	PC C120 PPAGE	FO
SP FFCO	IPL 0 CCR SX	HINZVC
EPAGE 0	GPAGE F DIRECT	0 RPAGE FD
🛄 Memory:4		
Memory:4		X Auto Logical
	30 20 45 50 41 47 45	Auto Logical
		Auto Logical
003FC0'L 30 003FC8'L 20 003FD0'L 45	30 30 20 45 50 41 47 20 30 30 20 45 50 41	Auto Logical OO EPAGE E OO EPA
003FC0'L 30 003FC8'L 20 003FD0'L 45 003FD8'L 47	30 30 20 45 50 41 47 20 30 30 20 45 50 41 45 20 30 30 20 45 50	Auto Logical OO EPAGE OO EPA GE OO EPA GE OO EP
003FC0'L 30 003FC8'L 20 003FD0'L 45	30       30       20       45       50       41       47         20       30       30       20       45       50       41         45       20       30       20       45       50       41         45       20       30       30       20       45       50         47       45       20       30       30       20       45	Auto Logical OO EPAGE OO EPAG E OO EPA GE OO EP AGE OO E

Figure 3-27. Global memory addressing access to Emulated EEPROM

### 3.7.3 Summary

The MMC module can be used to expand the accessible amount of memory of the MC9S12XHY256 MCU by paging the expanded global memory into a window in the local memory.

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### 3.8 ADC module

This lab example shows how to use the ADC module to perform single conversions, continuous conversions, and automatic compare. The ADC conversion results are output on a terminal window via the RS-232 port.

#### 3.8.1 Setup

The following steps must be followed before running the lab example.

- 1. Start CodeWarrior by selecting it in the Windows Start menu.
- 2. From the CodeWarrior main menu, choose File > Open and choose the S12XHY\_ADC\_Demo.mcp file.
- 3. Click Open. The project window will open.
- 4. The C code of this demonstration is contained within the main.c file. Double click on the file to open it.
- 5. From the main menu choose Project > Debug. This compiles the source code, generates an executable file, and downloads it to the demo board.
- 6. A new debugger environment will open. After the download to the demo board is complete, close the debugger environment.
- 7. The ADC conversion result is sent to the RS-232 port (baud rate = 9600, data bits = 8, parity = N, stop bits = 1, Flow control = none). Open a terminal window on the PC with this configuration.

#### 3.8.2 Instructions

Follow these instructions to run the lab example.

- 1. Press RESET. The ADC will perform a single 12-bit conversion on PAD00. To perform another conversion press SW4.
- 2. Vary the conversion result by turning the potentiometer RV1 on PAD00 and observe the changes in the terminal window.
- 3. Press RESET while pressing down SW1 and release the switches, following the next sequence RESET then SW1. The ADC will perform continuous 8-bit conversions on PAD00.
- 4. Vary the conversion result by turning potentiometer RV1 on PAD00 and observe the changes in the terminal window.
- 5. Press RESET while pressing down SW2 and release the switches, following the next sequence RESET then SW2. The ADC will perform continuous 12-bit conversions on PAD00 and compare the result to see if it is higher than 0x07FF. While the comparison is true, LED1 on the demo board flashes.
- 6. Vary the conversion result by turning potentiometer RV1 on PAD00 and observe the result in the terminal window. Notice how LED1 only flashes when the result is greater than 0x07FF.



### 3.8.3 Summary

The ADC module is highly autonomous with an array of flexible conversion sequences and resolution. It can be configured to select which analogue source to start conversion on, how many conversions to perform, and whether these must be on the same or multiple input channels. An automatic compare can be used to compare the conversion result against a programmable value for higher than, less than, or equal to matching. Any conversion sequence can be repeated continuously without additional MCU overhead.

For further information on the ADC module please refer to the following documentation which is available at www.freescale.com.

### 3.9 Timer module

This lab example shows how to use the Timer module to perform output compare and input capture. In case an oscilloscope is unavailable, the LEDs associated with port R on the DEMO9S12XHY256 board are used to indicate port toggles due to an output compare match, or a successful input capture.

### 3.9.1 Setup

The following steps must be completed before running the lab example

- 1. Ensure that the LED4 and POT jumpers on the JP14 have been removed.
- 2. Connect the potentiometer output (pin 18 on JP14) to port R3 (pin 7 on JP14). This allows the potentiometer RV1 to provide a stimulus to the input capture function on IOC1\_7.
- 3. Start CodeWarrior by selecting it in the Windows Start menu.
- 4. From the CodeWarrior main menu, choose File > Open and choose the S12XHY\_Timer\_Demo.mcp file.
- 5. Click Open. The project window will open.
- 6. The C code of this demonstration is contained within the main.c file. Double click on the file to open it.
- 7. From the main menu choose Project > Debug. This compiles the source code, generates an executable file, and downloads it to the demo board.
- 8. A new debugger environment will open. After the download to the demo board is complete, close the debugger environment.

#### 3.9.2 Instructions

To drive LEDs directly from timer output channels the software re-routes the timer 0 channels IOC0\_7 and IOC0\_6 from port T7:6 to port R1:0. In addition, to allow a connection to an input capture channel, the software also re-routes timer 1 channel IOC1\_7 from port T3 to port R3. The re-routing also gives the user access to the signals on the J1 header.

Follow these instructions to run the lab example

1. Press RESET. The code runs and re-routes the timer channels.



- Timer 0 performs output compares on channels IOC0\_7 (port R1 re-routed from port T7) and IOC0\_6 (port R0 re-routed from port T6). When a compare match occurs on IOC0\_7, port R1 (LED2) will toggle. When a match compare occurs on IOC0\_6, port R0 will toggle.
- 3. Timer 1 performs input capture on both rising and falling edges on channel IOC1\_7 (port R3 re-routed from port T3).
- 4. Use an oscilloscope to view the toggling timer 0 channels IOC0\_7 and IOC0\_6 on port pins R1 and R0 (J1 header pins 11 and 9). In case an oscilloscope is not available, the LEDs associated with port R1 (LED2) and port R0 (LED1) toggle in sync with the timer channels.
- 5. Use the potentiometer RV1 to create rail to rail rising and falling edges on timer 1 channel IOC1\_7.
- 6. To ensure the input capture is detecting edge transitions, notice LED3 toggles with each rising or falling edge.

### 3.9.3 Summary

The timer is a useful module. It provides a trigger for events to occur at a specific time, or captures when events have occurred. It is important in the scheduling of repetitive actions and contains a variety of special functions, such as pulse accumulation.

### 3.10 SCI communications

This lab example shows how to configure the SCI module to transmit and receive data using different baud rates.

### 3.10.1 Setup

The following steps must be followed before running the lab example.

- 1. Ensure that both the BCOM\_EN jumpers on JP11 have been removed.
- 2. Start CodeWarrior by selecting it in the Windows Start menu.
- 3. From the CodeWarrior main menu, choose File > Open and choose the S12XHY\_SCI\_Demo.mcp file.
- 4. Click Open. The project window will open.

### 3.10.2 Instructions

Follow these instructions to run the lab example

- 1. The C code of this demonstration is contained within the main.c file. Double click on the file to open it.
- 2. Configure the variable Baud\_Rate to 9600 and make sure all other options are disabled.



```
void main(void) {
    char RegisterCase;
    unsigned int BaudRatePrescaler, x,y;
    unsigned long Baud_Rate = 9600;
// unsigned long Baud_Rate = 19200;
// unsigned long Baud_Rate = 38400;
// unsigned long Baud_Rate = 57600;
```

Figure 3-28. Baud rate configuration section

- 3. From the main menu choose Project > Debug. This compiles the source code, generates an executable file, and downloads it to the demo board.
- 4. A new debugger environment will open.
- 5. The software uses the RS-232 port to interact with the user. Open a terminal window (baud rate = 9600, data bits = 8, parity = N, stop bits = 1, Flow control = None) to see the RS-232 port data.
- 6. Press Run. The code begins execution and configuring the SCI to the selected baud rate. Its status can be confirmed on the terminal window.
- 7. The SCI register configurations can be confirmed by selecting an option displayed on the terminal window. Choose some options and observe the SCI register configurations.
- 8. Repeat steps 2 to 9 for baud rates of 19200, 38400, and 57600. Alternatively modify the definition of the variable Baud\_Rate for a user configured baud rate.

#### 3.10.3 Summary

The SCI module can be used to communicate with peripheral devices or other MCUs.

### 3.11 SPI Communications

This lab example shows how to set up and use the SPI module in master mode to transmit and increment bytes of data.

As there is only one SPI module available on the DEMO9S12XHY256 board this example is limited to transmitting data only. When an SPI master transmits data to an SPI slave, data is usually received simultaneously and synchronized by a serial clock.

### 3.11.1 Setup

An oscilloscope and three scope probes are required for this demo. The following steps must be followed before running the lab example.

- 1. Start CodeWarrior by selecting it in the Windows Start menu.
- 2. From the CodeWarrior main menu, choose File > Open and choose the S12XHY\_SPI\_Demo.mcp file.
- 3. Click Open. The project window will open.
- 4. The C code of this demonstration is contained within the main.c file. Double click on the file to open it.



- 5. From the main menu choose Project > Debug. This compiles the source code, generates an executable file, and downloads it to the demo board.
- 6. A new debugger environment will open. After the download to the demo board is complete, close the debugger environment.
- 7. Attach scope probes to signals PS5, PS6, and PS7 on header J1.
- 8. Configure the oscilloscope to trigger on the falling edge of PS7.

#### 3.11.2 Instructions

Follow these instructions to run the lab example.

- 1. Press RESET. The code begins execution, configuring the SPI to transmit an incrementing byte of data at a baud rate of 15.625 kbits/s.
- 2. Monitor the SPI transmission on the oscilloscope to see the relationship between Slave Select (PS7), data transmitted on MOSI (PS5), and the Serial Clock (PS6) signals.

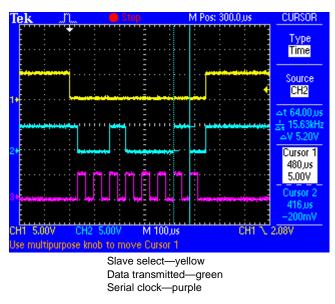


Figure 3-29. SPI protocol signals

### 3.11.3 Summary

The SPI module can be used to allow duplex synchronous serial communication between peripheral devices and the MCU.

### 3.12 Motor Control Module

This demonstration code has been constructed to explain how to set up the motor control module and operate an external stepper motor. To operate this demo, connecting an external motor to PTU0-3 is required.



### 3.12.1 Set-up

- 1. Connect a stepper motor to motor 0 pins, PTU0-3 –J3 on the demo board.
- 2. Start CodeWarrior by selecting it in the Windows Start menu.
- 3. From the CodeWarrior main menu, choose File > Open and choose the S12XHY\_MC\_DEMO.mcp file.
- 4. Click Open. The project window will open.
- 5. The C code of this demonstration is contained within the main.c file. Double click on the file to open.
- 6. From the main menu choose Project > Debug. This compiles the source code, generates an executable file, and downloads it to the demo board.

The motor control module is set-up via the MC\_init function where the motor control registers are configured. The module can be set to operate in various modes. In this case it is operated in dual full H-bridge, which is ideal for controlling stepper motors. The physical set-up of the motor requires four connections (Figure 3-30), where each PWM channels has two connections. Refer to the section *Motor Controller* in the *MC9S12XHY256 Reference Manual*.

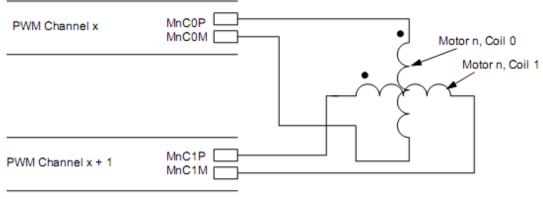


Figure 3-30. —Dual full H-bridge configuration

### 3.12.2 Instructions

This is a self-contained example, which requires no intervention. On running the program, the motor initializes by returning to zero (RTZ) position. The motor is controlled by adjusting the potentiometer RV1 on the board.

#### 3.12.3 Summary

This demonstration has shown that it is possible to control the movement of a stepper motor and this basic example can be applied to many types of applications.



### 3.13 LCD module

The demonstration code incorporates an example of an odometer display and trip meters, that increments in real time. There are also other common items displayed and updated on the LCD to emulate a dashboard unit display. This document describes the software and explains the operation of the LCD module.

#### 3.13.1 Set-up

- 1. Start CodeWarrior by selecting it in the Windows Start menu.
- 2. From the CodeWarrior main menu, choose File > Open and choose the S12XHY\_LCD\_DEMO.mcp file.
- 3. Click Open. The project window will open.
- 4. The C code of this demonstration is contained within the main.c file. Double click on the file to open it.
- 5. From the main menu choose Project > Debug. This compiles the source code, generates an executable file, and downloads it to the demo board.

To begin using the LCD, the pins that operate the front-planes and backplanes must be configured. This is made easy for the user because when the LCD module is enabled, performed in the LCD\_Init function, the 44 pins output an LCD driver waveform based on the DUTY and BIAS settings in LCDCR0.

```
void LCD_init()
{
   CONFIG_CLKSOURCE();
   SET_LCDCR1_REG();
   SET_LCD_FRAME_FREQU();
   SET_DUTY();
   SET_BIAS();
   ENABLE_FP();
   ENABLE_LCD(ON);
  }
}
```

//Configure clock source //Configure operation in stop/wait //Configure frame frequncy //Enable Frontplanes //Enable LCD

#### Figure 3-31. LCD initialization functions

The frequency at which the LCD glass must be operated is determined by the glass manufacturer and in the case of this demo it is 61 Hz. This is obtained by setting the frame frequency via the LCD clock prescaler bits. Refer to the section *Liquid Crystal Display* in the *MC9S12XHY256 Reference Manual* which provides information on the LCD clock vs. the frame frequency.

The LCD module has a dedicated 20 bytes of RAM at 0x208 which contains data that is displayed on the 160 segment LCD. This LCD RAM interfaces with the internal address and data buses of the MCU. During any type of power cycle, the contents of the RAM can be indeterminate, therefore it is recommended to set the 20 bytes of RAM to a known state prior to exercising.

#### 3.13.2 Instructions

This is a self-contained example and requires no intervention. On program start-up, the LCD displays S12XHY and will proceed into a never-ending loop which is responsible for the updating and animation of the LCD display.



A port interrupt has also been used on analogue ports which are connected to the switches. On pressing SW1 on the hardware, this allows the user to switch the LCD numerical display between ODO, TRIPA and TRIPB.

### 3.13.3 Summary

This demonstration has shown that controlling the LCD is a matter of updating the dedicated RAM and manipulating the backplane and frontplane pins. This demonstration does not save the information during power down, notice then that the odometer and trip information have been reset. A further exercise to this example is to use the emulated EEPROM driver, to enable recovery of this information, by continuously reading and writing the data to the device's D-flash, available for free on the Freescale website.

### 3.14 Stepper stall detect module

This demonstration code has been constructed to demonstrate SSD module capabilities using a back EMF signal to determine stall detection on a stepper motor. This module consists of an internal hardware block included in the S12XHY microcontroller family. This hardware module shares the same pins with the motor control module (MCM), thus no additional wiring is required to use SSD and MCM for stepper motor control.

To operate this demo, it is required to connect an external stepper motor to MOTOR0 pins on the DEMO9S12XHY256 board.

#### 3.14.1 Set-up

- 6. Connect a stepper motor to MOTOR0 pins, PTV0–3 –J3 on the demo board.
- 7. Start CodeWarrior by selecting it in the Windows Start menu.
- 8. From the CodeWarrior main menu, choose File > Open and choose the S12XHY\_SSD\_DEMO.mcp file.
- 9. Click Open. The project window will open.
- 10. The C code of this demonstration is contained within the main.c file. Double click on the file to open it.
- 11. From the main menu choose Project > Debug. This compiles the source code, generates an executable file, and downloads it to the demo board.

The stepper stall detection module is set-up via the SSD0\_Step function. The SSD configuration registers are modified in sequence depending on the SSD stage, see Figure 3-32 for more details. The module can be used to calibrate a stepper motor, use the visualization tool included in this software package to modify stall detection values on the run, and find the adequate stall value to fit your HW set up, a full CodeWarrior license is required to use this feature. The physical set-up of the motor requires four connections, use the Motor Control Diagram connection (shown in the section *Motor Controller* in the *MC9S12XHY256 Reference Manual*) as a guide.

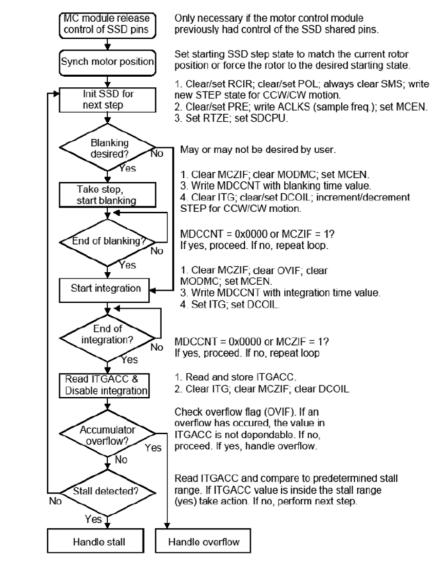


Figure 3-32. SSD software flow chart

#### NOTE

Be aware that parameters calibration may be required to successfully run this application code, the calibration values depend on the stepper motor type. Use Motor\_Calibarion.vtl (Figure 3-33) to help in finding the correct values that meet your Motor parameters and be able to determine stall state.



Conclusion

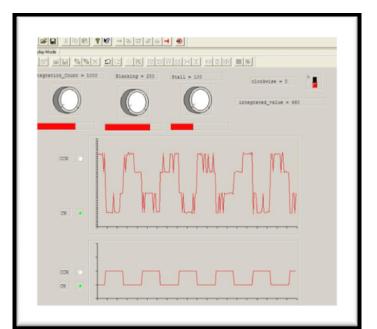


Figure 3-33. Visualization tool application (available, a full CodeWarrior license is required)

### 3.14.2 Instructions

This project is written to work with a small stepper motor connected to the SSD0 module pins on the DEMO9S12XHY256. It is assumed the stepper motor has a pointer attached to the shaft coming out of the motor. When the project is working, the user will see the pointer rotate in one direction until it bumps into an object (stall detected). When the pointer bumps into an object, the SSD accumulator yields an integration result with a lower magnitude value that is between the stall magnitude and zero. The code may interpret this as a stall, and reverse the rotational direction. The process repeats by beginning another sequence of steps until another stall is detected and the rotational direction is again reversed.

### 3.14.3 Summary

This demonstration has shown that it is possible to determine stall state using the SSD hardware module of a stepper motor and this basic example can be applied to many types of applications.

# 4 Conclusion

The S12XHY family of microcontrollers (MCUs) offers the enhanced features of 16-bit performance at a value of 8-bit MCUs. The S12XHY is an extension of the S12HY featuring higher performance and additional modules.

The S12XHY family is ideal for a wide range of central body control applications, such as low-end instrument clusters.

A zip file, AN4236SW.zip, containing the complete CodeWarrior projects for the lab examples accompanies this application note. The file can be downloaded from <u>www.freescale.com</u>.

#### **Useful Reference Material**



## 5 Useful Reference Material

The following material is available at <u>www.freescale.com</u>.

Software development tools

• CodeWarrior 5.1 for HCS12(X) Microcontrollers

Application notes

- AN3330 Introduction to the Stepper Stall Detector Module
- AN3219 XGATE Library: TN/STN LCD Driver
- AN3622 Comparison of the S12XS CRG Module with S12P CPMU Module
- AN3034 Using MSCAN on the HCS12 Family
- AN2612 PWM Generation Using HCS12 Timer Channels
- AN2428 An Overview of the HCS12 ATD Module
- AN2883 Serial Communication Interface as UART on HCS12 MCUs
- AN2461 Low Power Management using HCS12 and SBC devices
- AN4201 *Migrating Applications from S12HY to S12XHY*
- AN4024 High Speed Stall Detection on S12HY and S12XHY

Reference manual

- MC9S12XHY256 Reference Manual
- S12XHY256ACDUG Automotive Cluster Demo Guide

Useful links

- LCD\_TIPS
- S12HXY256\_Cluster\_DEMO\_VIDEO
- EEPROM\_Software\_Driver



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