

MPC5674F PMC Trimming of Internal Regulators and Low Voltage Detection

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1 Introduction

This application note covers power management controller trimming of internal regulators and low voltage detection on the MPC5674F.

1.1 Overview

This application note describes the trimming used on internal regulators and Low Voltage Detection (LVD) on the MPC5674F microcontroller (MCU). It details the different trimmings performed, and explains how and when to use the trimming functionality.

The application note specifically covers the trimming of internal regulators and LVDs, but does not cover all functionalities of the internal regulators or LVDs. It is assumed that the reader has a basic understanding of the Power Management Controller (PMC) on the MPC5674F.

NOTE

Specifications used in this application note are taken from the latest MPC5674F Microcontroller Data Sheet as of the time of publication. You must consult the latest MPC5674F Microcontroller Data Sheet to ensure the

Contents

1	Introduction.....	1
1.1	Overview.....	1
1.2	MPC5674F PMC.....	2
2	Bandgap.....	2
3	Monitoring the PMC via the eQADC.....	2
4	Trimming of Internal Regulators.....	3
4.1	Untrimmed internal regulator.....	4
4.2	Bandgap trimmed internal regulator.....	5
4.3	User trimming of internal regulators.....	5
5	Potential Hazards with Trimming.....	9
6	Implementing a PMC Monitoring Strategy.....	9
7	Trimming of LVD circuits.....	10
8	User Trimming — Use Cases.....	10
9	Summary.....	11

latest specifications are used if applying any methods used within this application note.

1.2 MPC5674F PMC

The PMC on the MPC5674F generates internal supplies and LVD circuits. The PMC implements an internal 3.3 V regulator and has the ability to generate a 1.2 V supply from either an internal linear regulator or internal switched mode power supply (SMPS). It also implements LVD circuits for a selection of supplies, including the internal regulators and I/O supplies, that can be used to gate, reset, or interrupt events.

The internal regulators use a common PMC bandgap as a reference to achieve the desired supply level (that is, 1.2 V or 3.3 V). This bandgap is also used by the LVD circuits as a reference for the LVD thresholds.

During power-up, while the MCU is in reset, the PMC bandgap is untrimmed and therefore has a wide variation, this has an impact on the variations of the internal regulators and LVD thresholds. As the device comes out of reset, the PMC trims this bandgap to a tighter tolerance to reduce the variation. This has the effect of tightening the tolerance on the internal regulators and LVD thresholds, however other factors, such as increased loading on the internal regulators also affect this tolerance.

The user has the ability to trim the levels of both the internal regulators and LVD thresholds via software. The trimmable supplies and LVDs can all be monitored via the enhanced Queued Analogue to Digital Converter (eQADC), allowing the user to read the current level and trim it accordingly. This provides flexibility for certain conditions, however the user must have a good understanding of trimming. It is possible to exceed MCU specifications if supplies are trimmed incorrectly.

2 Bandgap

The bandgap is used by the PMC as an absolute reference point for all the internal regulators and LVD thresholds. The nominal value of the PMC bandgap is 0.62 V.

During power-up, while the MCU is in reset the PMC bandgap is untrimmed and will vary by +/- 5%.

On the release of reset, the PMC trims the bandgap to a variation of +/- 3% to tighten the tolerances of the internal regulators and LVD thresholds. The PMC performs this trimming by fetching trim values located in the shadow flash, which have been programmed by Freescale during testing of the production devices. The user is not able to trim the bandgap reference at any point.

After the PMC has trimmed the bandgap it remains with the variation of +/- 3% until the next power cycle. The user can monitor the bandgap voltage by reading it via the eQADC, this is detailed in Chapter 4. "[Monitoring the PMC via the eQADC](#)"

3 Monitoring the PMC via the eQADC

The eQADC can be used to internally monitor the voltage of the internal regulators and the LVD thresholds. Configure an eQADC command to sample a specified channel, listed in [Table 1](#), relevant to the supply or LVD to monitor.

Table 1. ADC channels for monitoring PMC signals

eQADC_A channel number	Signal propagated to ADC	Signal propagated to ADC
ADC0 CH145	Band gap 0.62 V	0.62 V (trimmed)
ADC0 CH146	Analog supply 1.2 V	1.22 V
ADC0 CH147	VDD12OUT	Equal to VDD12OUT / 2.045
ADC0 CH180	LVD 1.2 V	Equal to VLVD12 / 1.774
ADC0 CH181	VDD33OUT	Equal to VDD33OUT / 5.460
ADC0 CH182	LVD 3.3 V	Equal to VLVD33 / 4.758

eQADC_A channel number	Signal propagated to ADC	Signal propagated to ADC
ADC0 CH183	LVD 5.0 V	Equal to VLVDREG / 4.758 in LDO mode; (VLVDREG / 7.032 in SMPS mode)
ADC1 CH196	LVD VDDA	Equal to VDDA LVD / 3.8934

4 Trimming of Internal Regulators

The PMCs internal regulators use the bandgap voltage as a reference point to achieve a desired output. Figure 1 illustrates how the reference voltage for the internal 3.3 V regulators is created from the bandgap.

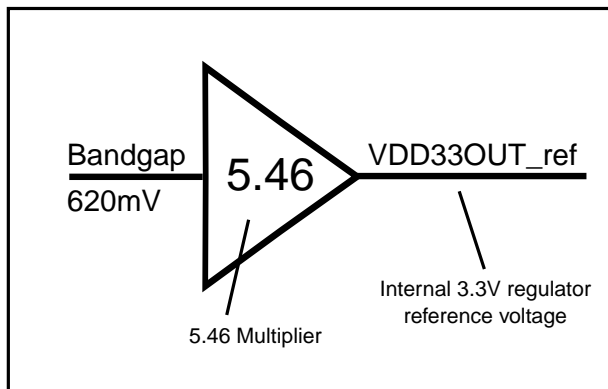


Figure 1. Bandgap reference for internal 3.3 V regulator

The bandgap is multiplied by a factor of 5.46 to achieve a reference voltage for the internal 3.3 V regulator.

The bandgap is used as the reference for the internal regulators therefore the trimming of the bandgap has an effect on the variation of the internal regulators.

There are three stages to consider regarding the trimming of the internal regulators:

- Untrimmed — During start-up, while the MCU is in reset Bandgap
- Trimmed — Occurs on the de-assertion of reset
- User Trimming — When the user trims the internal regulators via software

NOTE

In the following sections, the internal 3.3 V regulator is used to explain trimming. The same methods described can be applied to the internal 1.2 V regulator.

A summary of the three stages is shown in Figure 2, the details of this are covered in the following sections.

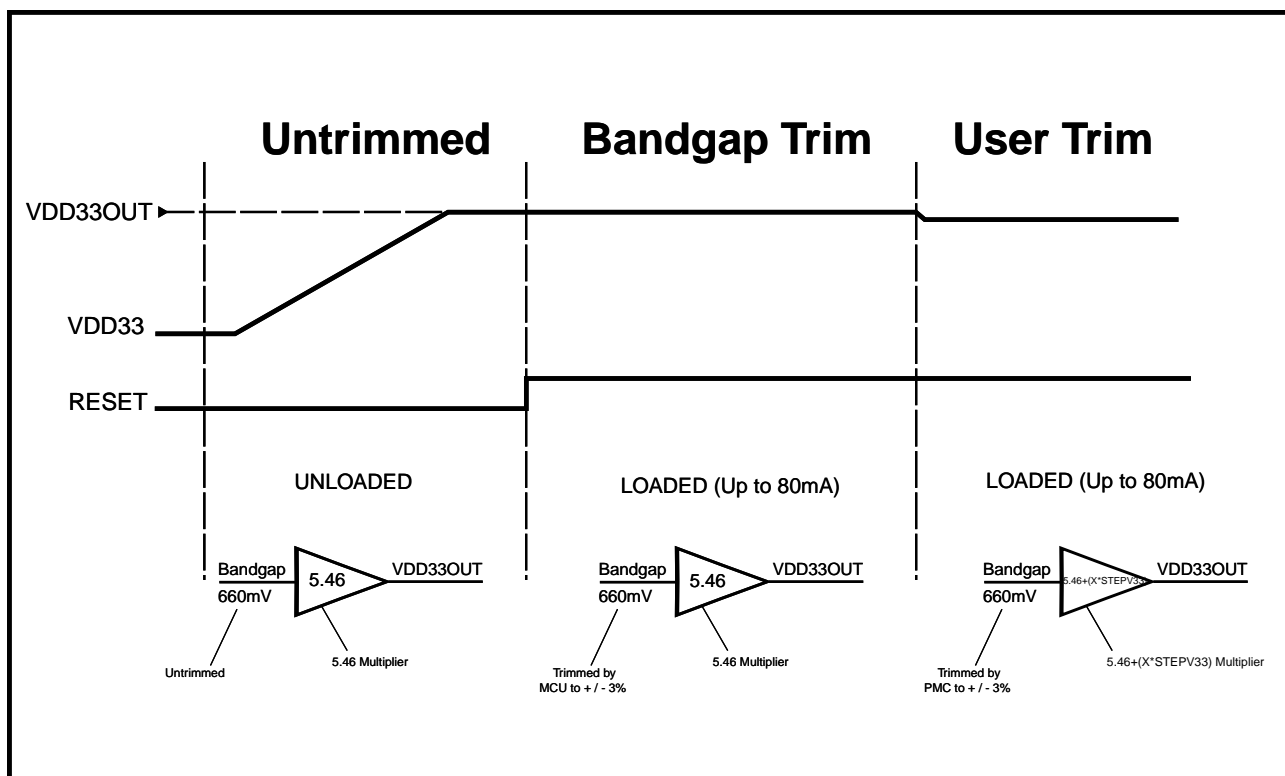


Figure 2. The different stages of trimming

4.1 Untrimmed internal regulator

During power-up, while the MCU is in reset, the bandgap is in an untrimmed state. At this point the internal 3.3 V regulator is also unloaded. This means that the variation on the output of the internal regulator is mainly related to the variation of the untrimmed bandgap.

During power-up, the internal 3.3 V regulator attempts to regulate to the output level specified by the VDD33OUT specification, however the output of the regulator can vary by the VDD33OUT-6% or VDD33OUT+10% ("Untrimmed VREG 3.3 V output variation before band gap trim" spec). The potential variation of the output of the internal 3.3 V regulator is shown in Figure 3.

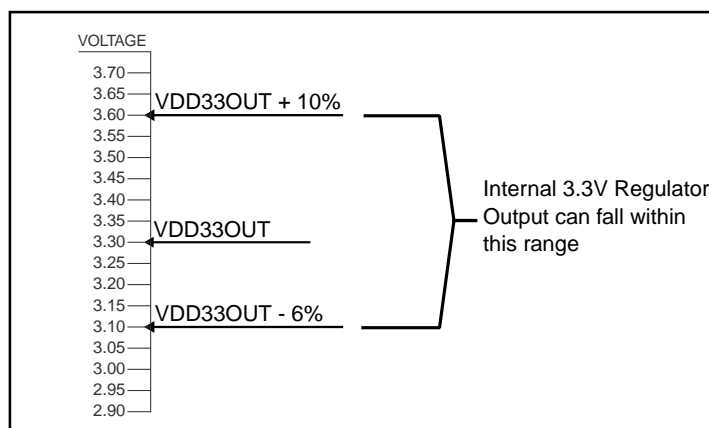


Figure 3. Range of internal 3.3 V regulator while in untrimmed state

4.2 Bandgap trimmed internal regulator

Upon the release of reset, the PMC trims the bandgap to $\pm 3\%$. This, therefore, trims the reference voltage for the internal 3.3 V regulator. You may expect that the internal regulator would now be trimmed to $\pm 3\%$, however due to loading on the regulator this is not the case.

During the untrimmed state, with the MCU in reset, the internal 3.3 V regulator is largely unloaded. This means loading on the regulator has minimal impact on its variation.

When the MCU de-asserts reset, and trims the bandgap, the internal 3.3 V regulator has increased loading from internal flash usage and internal pad circuits. The internal 3.3 V regulator can also be used externally with a combined loading (internal and external) of up to 80 mA. This increased loading, impacts the variation of the internal regulator, this means the internal regulator has a larger variation than the $\pm 3\%$ of the trimmed bandgap.

The variation of the internal 3.3 V regulator after bandgap trimming is specified in the MPC5674F Microcontroller Data Sheet (“Trimmed VREG 3.3 V output variation after band gap trim” spec). See [Figure 4](#).

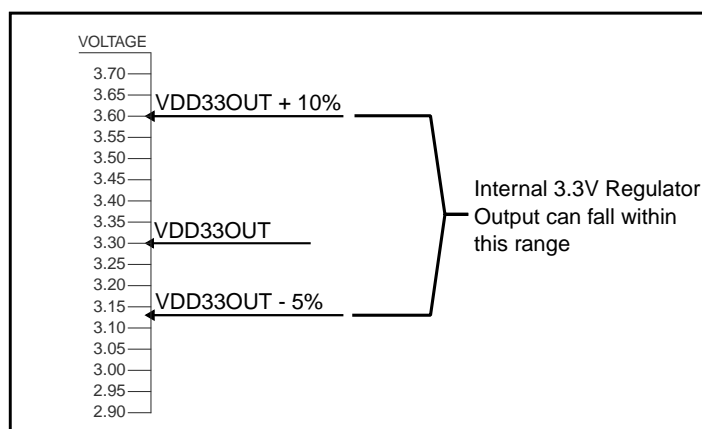


Figure 4. Range of internal 3.3 V regulator after bandgap trimming

4.3 User trimming of internal regulators

After the MCU has come out of reset, and the PMC has trimmed the bandgap, the user can sample the internal regulator supply using the eQADC and adjust this value up or down by a number of voltage steps.

Before the user trimming is performed, it is essential to understand exactly what a voltage reading of the eQADC relates to and by how much it could vary. This avoids conditions where trimming the internal regulators puts the MCU out of spec.

[Figure 5](#) shows two potential scenarios that can occur after bandgap trimming.

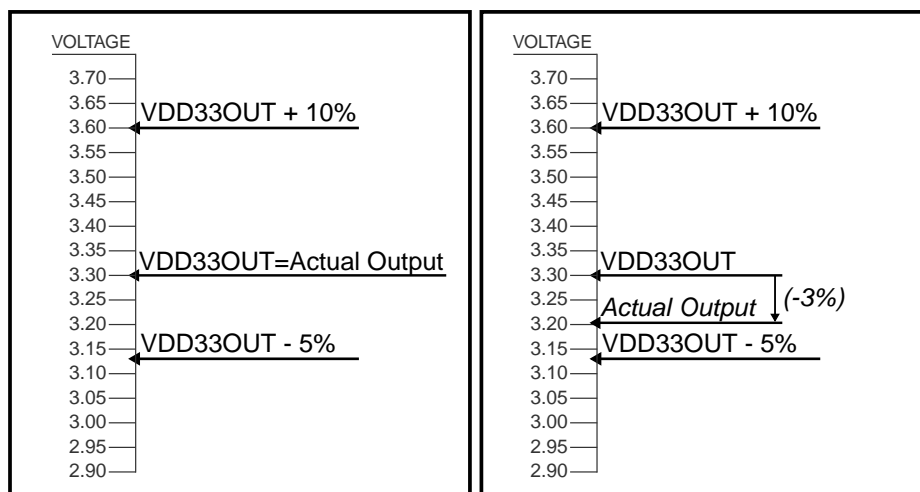


Figure 5. Output of internal 3.3 V regulator after bandgap trimming

In [Figure 5](#), VDD33OUT is the specification in the MPC5674F Microcontroller Data Sheet for the targeted (that is, ideal) output of the internal 3.3 V regulator. The actual output of the internal 3.3 V regulator may not match the VDD33OUT specification, due to variations of the internal regulator (explained in the previous chapters). The actual outputs can vary between the upper and lower limits (+10% to -5%) which are also specified in the MPC5674F Microcontroller Data Sheet and have been determined by characterization of the internal 3.3 V regulator.

- The box on the left shows a scenario where the actual output of the internal 3.3 V regulator is equal to VDD33OUT specification. This means there is zero variation between the ideal output and the actual output of the regulator. In this case the actual output of the internal regulator can vary by +10% to -5% of the VDD33OUT specification.
- The box on the right shows a scenario where the actual output of the internal 3.3 V regulator is not equal to the VDD33OUT specification. In this example, the actual output is 3% less than the ideal output, due to the variation of the regulator (for example, related to load or temperature). In this case the actual output of the internal regulator still varies by +10% to -5% of the VDD33OUT specification (that is, 3.3 V), not by +10% to -5% of the actual value (that is, 3.2 V).

When the user performs an eQADC conversion on the internal 3.3 V regulator, the value sampled will be the “actual value”. Using the above example, this would be 3.3 V for the box on the left, and 3.2 V for the box on the right.

The user has the option to fine tune the level of the internal regulator via the PMC Trimming Register (PMC_TRIMR). In this register the user can modify the VDD33TRIM field to adjust the internal 3.3 V regulator by a number of voltage steps. These steps are described in [Table 2](#).

Table 2. PMC_TRIMR[VDD33TRIM] description

Field	Description
VDD33TRIM	<p>Description:</p> <p>This field is used to fine tune VDD33 the output voltage of the 3.3 V regulator, the VDDSYN (VRC33) supply. See the MPC5674F Microcontroller Data Sheet for details.</p> <p>Bit values:</p> <p>0111 — VDD33–8 * STEPV33</p> <p>0110 — VDD33–7 * STEPV33</p> <p>0101 — VDD33–6* STEPV33</p> <p>0100 — VDD33–5* STEPV33</p> <p>0011 — VDD33–4* STEPV33</p> <p>0010 — VDD33–3* STEPV33</p> <p>0001 — VDD33–2* STEPV33</p> <p>0000 — VDD33–1* STEPV33</p> <p>1111 — Nominal, start-up and default value VDD33</p> <p>1110 — VDD33+1* STEPV33</p> <p>1101 — VDD33+2* STEPV33</p> <p>1100 — VDD33+3* STEPV33</p> <p>1011 — VDD33+4* STEPV33</p> <p>1010 — VDD33+5* STEPV33</p> <p>1001 — VDD33+6* STEPV33</p> <p>1000 — VDD33+7* STEPV33</p>

This register is used to modify the multiplication factor for the internal regulators reference voltage. This results in the regulator attempting to regulate to a modified reference voltage. This is illustrated in [Figure 6](#).

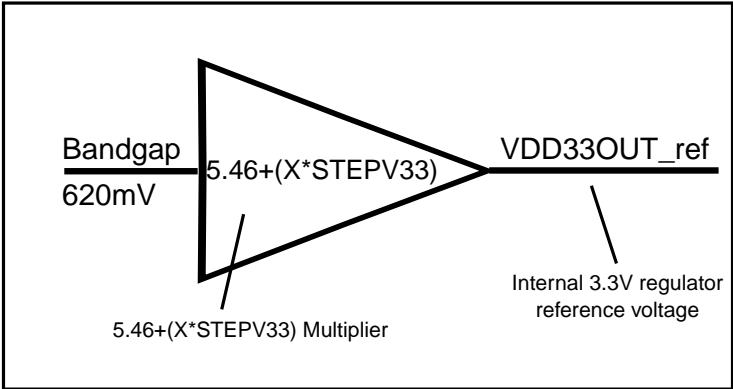


Figure 6. User trimming of internal 3.3 V regulator

The user trimming modifies the multiplication factor for generating the internal reference for the 3.3 V regulator. This however, does not impact the variation of the output voltage. The variation remains the same as a percentage, however the levels are shifted by the corresponding offset set by the VDD33TRIM value.

The VDD33TRIM register is used to trim the output of the internal regulator. The default value of the VDD33TRIM register relates to the VDD33OUT specification (that is, 0b1111 = 3.3 V), however this does not mean that the default output of the internal 3.3 V regulator will be VDD33OUT, as explained in [Figure 5](#).

Trimming of Internal Regulators

When the user modifies the value of the PMC_TRIMR[VDD33TRIM] field, they must be aware of the impact it has on the variation limits of the internal 3.3 V regulator. [Figure 7](#) can be used to explain this.

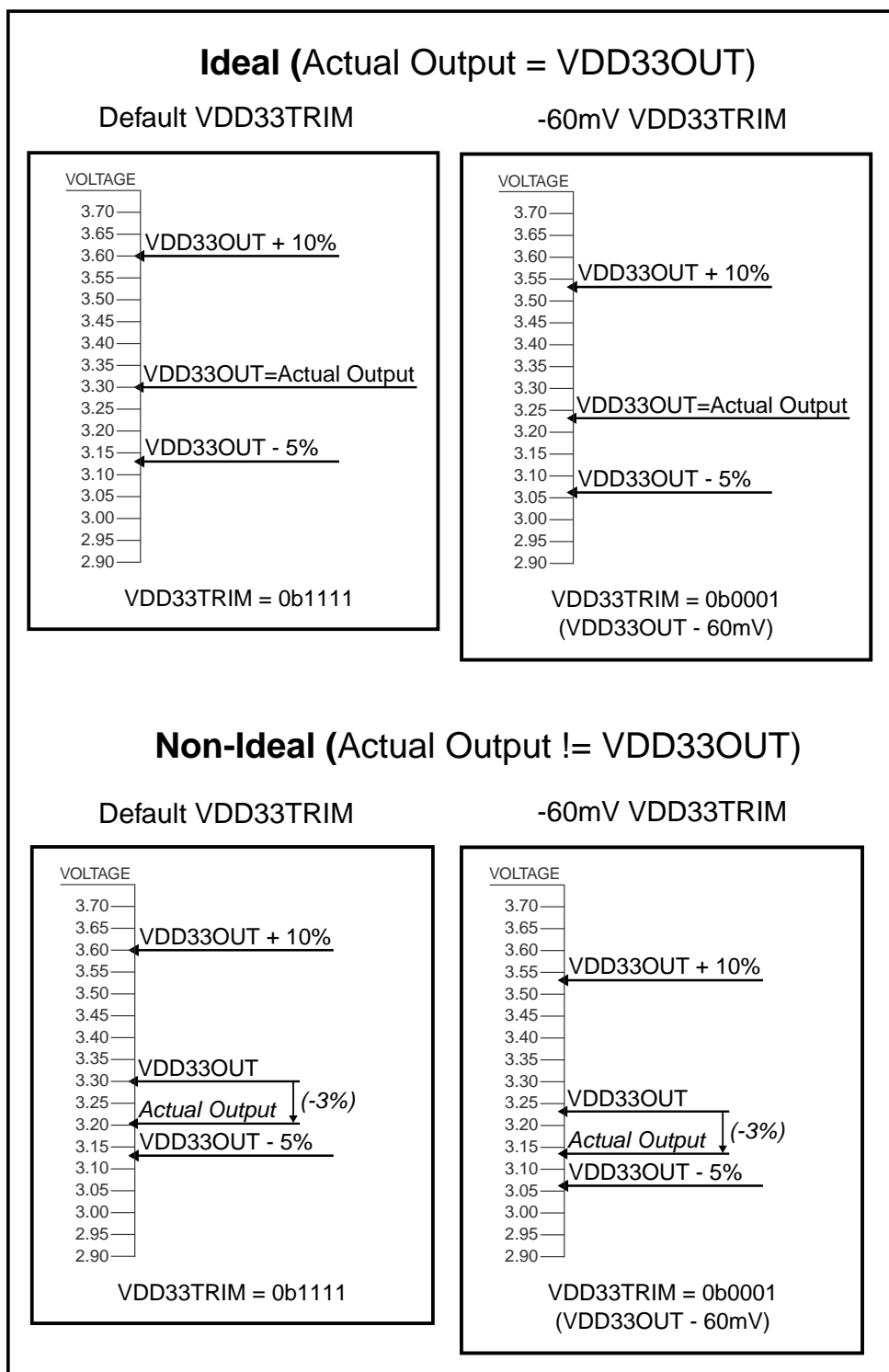


Figure 7. Impact of user trimming of VDD33TRIM field

As in [Figure 5](#), there are two scenarios to consider:

- In an ideal scenario — The default output of the regulator (read by the user via the eQADC) is equal to the VDD33OUT specification. The variation of the regulator is therefore +10% to -5% of the VDD33OUT specification.

If the user trims the VDD33TRIM register to 0b0001 (that is, -60 mV), then the new output of the regulator will be VDD33OUT -60 mV. The variation of the internal regulator will also shift by the same offset.

- In a non-ideal scenario — The output of the internal 3.3 V regulator does not equal the VDD33OUT specification. The value read by the eQADC will relate to the actual output of the internal 3.3 V regulator, which in this example is 3% less than the VDD33OUT specification (that is, 3.2 V). As discussed earlier, the variation of the internal 3.3 V regulator will still be relative to +10% to -5% of the VDD33OUT specification.

If the VDD33TRIM register is trimmed to 0b0001 (that is, -60 mV), then the new output of the regulator will be the previous output (read by the eQADC) minus 60 mV (that is, $3.2\text{V} - 60\text{mV} = 3.14\text{ mV}$ in this example). The variation of the internal 3.3 V regulator will also shift by the same offset.

5 Potential Hazards with Trimming

In the previous example, the minimum variation of the internal regulator is within specification for the VDD33 supply. If the user had programmed the VDD33TRIM field with an offset of -240 mV, then the minimum limit of the variation would be 2.93 V. If the internal 3.3 V regulator was left unmonitored (that is, the software performed no further trimming) the variation of the internal 3.3 V regulator could drop the output below 3.0 V and therefore exceed the minimum specification for the VDD33 supply.

This effect is also prevalent in the maximum limit of the variation, if the internal supply is positively trimmed.

If the user plans to trim the internal regulators only once after startup, then care must be taken that the variation of the internal regulator is within specification.

6 Implementing a PMC Monitoring Strategy

Using a good power supply monitoring strategy. It is possible to trim the internal supplies to a value that could potentially put the internal regulator out of spec. An understanding of how the output of the internal regulators can vary is required.

- Variations of the internal regulators are typically related to two conditions, loading and temperature. The loading of an internal regulator is related to the specific software being run, however the variation of the regulator under a constant temperature is typically relatively low. For example, it is unlikely that the internal 3.3 V regulator vary from +10% to -5% due to loading alone.
- Typically, temperature plays a larger impact in the variations of the internal regulators. For example, it is possible that the internal 3.3 V regulator will maintain +5% at -40 degrees Celsius, but change to -5% at 125 degrees Celsius. As temperature is typically slow changing (in relation to the speed of the MCU) it is easier to control and monitor the impact it has on the internal regulators compared to the impact from loading.

If the user implements a power supply strategy that monitors the output of the internal regulators every 10 or 100 milliseconds (using the internal eQADC channels), then you can track changes to the output of the regulator by temperature. A temperature sensor is also implemented on the MPC56xx family of MCUs allowing you to read the MCU temperature (again, via an internal eQADC channel) and correlate this to changes in the internal regulator outputs.

If the power supply strategy software detects a drift of the output of the internal regulators due to temperature, then it can trim the internal regulator accordingly to maintain a constant output.

As this process occurs on a 10's or 100's of milliseconds basis, the software can keep the actual output of the internal regulators within MCU supply specifications, even if the variation limits are out with specification.

7 Trimming of LVD circuits

LVDs undergo the same procedure of trimming as internal regulators. Therefore this section only points out key differences, or items of note.

To summarize the trimming steps of the LVD circuits:

- **Untrimmed** — During start-up, while the MCU is in reset
As with the internal regulators, the bandgap is used to generate a reference point for the LVD threshold.
- **Bandgap Trimmed** — Occurs on the de-assertion of reset
As with the internal regulators, the bandgap trimming tightens the variation of the LVD thresholds.
- **User Trimming** — When the user trims the internal regulators via software
The user is able to trim the LVD thresholds in exactly the same manner as the internal regulators.

The key difference between the LVD trimming and the internal regulator trimming, is that the LVDs do not undergo any loading. This means that the bandgap trimming has more of an impact on the LVD tolerance, whereby the trimming of the bandgap is largely passed onto the LVD. This results in the LVD circuits having less variation compared to the internal regulators.

8 User Trimming — Use Cases

There are several use cases where the user may want to trim the internal regulator or LVD thresholds. The following use cases benefit from trimming the internal regulator:

- **Reducing current consumption**

One way to reduce current consumption on the MCU is to trim the internal regulators to a lower voltage. This is especially prevalent with the internal 1.2 V regulator that draws the majority of the MCU current. If the regulator can be trimmed lower (by 5%), this then results in a 5% reduction in current consumption, which can provide an additional margin to the external supply from which the current is sourced.

- **Compensating for voltage (IR) drops under high loading**

When the MCU is under high loading, it is possible that the voltage on the internal regulators droop due to the increased loading. In this event, it is possible that the voltage level drops close to an LVD threshold. Therefore, it would be beneficial to monitor the internal regulators and increase the voltage by trimming under periods of high loading. This maintains a stable voltage level for the internal regulator.

For example, high loading on the 1.2 V internal regulator can arise from intensive core and cache usage. If the user knew that a DSP routine that was locked in cache was about to be executed, then the user software could trim the internal regulators to a higher voltage to compensate for a potential IR drop when the DSP routine begins.

This can also apply to the internal 3.3 V regulator for situations where the flash loading significantly increases due to a specific software operation.

The following use cases benefit from trimming the LVD thresholds:

- **Tightening the acceptable tolerance of a supply**

One role of the LVD circuit is to monitor that the supplies are operating within a given tolerance. If the user has a specific tolerance requirement for a supply, then trimming the LVD provides tighter monitoring of the supply.

A benefit of the PMC LVDs are that they have the flexibility to generate either an interrupt or create a reset event.

It may be beneficial to the user to configure an LVD to report low voltage warnings. If the LVD was trimmed to a tight tolerance to its respective supply, then upon a breach of the LVD threshold an interrupt is generated. In this interrupt service routine the user's software could analyze the number of threshold occurrences, and on a certain number of iterations it could reduce the LVD threshold (via trimming) and configure the LVD to generate a reset event if the updated threshold is breached.

This strategy allows the user to closely monitor a power supply and gather statistical information on the supply, without causing a big impact on the system.

- **Intentionally drooping supply without reset of the MCU**

In some conditions it is possible that the application hardware could droop the 5 V supply to a low level, perhaps out-with specification, but does not expect the MCU to reset. One condition where this is especially prevalent is during a cold crank condition in a powertrain application. In a cold crank event the battery voltage can droop down to 4 V, thereby having an impact on the 5 V supply to the MCU.

In a cold crank event, it is desirable to keep the MCU alive and operational (but potentially ignoring certain ADC data or I/O). It is possible to do this by trimming the LVD circuits for the 5 V LVDs. If the user could predict when a cold crank situation was about to occur (using the on-chip temperature sensor to assist this decision), then the users software could trim any 5 V LVD circuits to either ignore a threshold or generate an interrupt on the the threshold.

This could allow the battery to droop the 5 V supply without the reset circuits being triggered.

9 Summary

This application note has shown the different trimming steps involved for internal regulators and LVD circuits on the PMC module of the MPC5674F. It has explained the control that the user has for these trimming stages, and has shown how this can be applied to real world use cases.

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