

Architectural Differences Between i.MX51 and i.MX53

The i.MX51 and i.MX53 multimedia applications processors represent two of Freescale Semiconductor’s ARM Cortex-A8 based multimedia-focused products; offering high performance processing optimized for low power consumption.

The i.MX51 and i.MX53 processors have similar features. Their similar implementation allows a natural migration from i.MX51 to i.MX53. The implementation of i.MX53 offers improved performance, power efficiency, and additional multimedia capabilities which help reduce BOM costs in some use-cases over i.MX51. The flexibility of these two processors allows them to be used in a wide variety of applications such as the following:

- Tablets
- Smartbooks
- Mobile Internet Devices (MID)
- Portable Media Players (PMP)
- Portable Navigation Devices (PND)
- High-End PDAs
- Gaming Consoles
- Automotive Infotainment
- Industrial and medical Devices

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1 Overview

The i.MX51 and i.MX53 contain a large number of digital and analog modules. For a more detailed description of all of the modules and features for each, refer to the product datasheet and/or reference manual for i.MX51 and i.MX53. [Table 1](#) shows the key feature differences and improvements of i.MX51 and i.MX53 that will be discussed in this application note.

Table 1. Comparative Feature Summary of the i.MX51 and i.MX53

Feature	i.MX51	i.MX53
Core	Cortex-A8 800 MHz (Consumer) 600 MHz (Automotive/Industrial)	Cortex-A8 Upto 1.2 GHz (Consumer) 800MHz (Automotive/Industrial)
Memory	512 MB, x32 LP-DDR1, DDR2	2 GB, x32 DDR2, LV-DDR2, DDR3, LP-DDR2
Max Memory Speed	200 MHz clock, (400 Mbps x32)	400 MHz clock, (800 Mbps x32)
NAND	SLC/MLC, 8-bit ECC	SLC/MLC, 16-bit ECC
Video Decode	HD720p30	HD1080p
Video Encode	D1	HD720p
3D GPU	OpenGL/ES 2.0 27 Mtri/s, 166 Mpix/s	OpenGL/ES 2.0 33 Mtri/s, 200 Mpix/s
2D GPU	OpenVG 1.1, 166 Mpix/s	OpenVG 1.1, 200 Mpix/s
LCD Resolution	WXGA (1280 x 800) 60 fps	UXGA (1600 x 1200) 60 fps
LCD Interface	Parallel	Parallel, LVDS (x2)
Video Out	Component HD720 60 fps	VGA HD1080p60
HDD Interface	P-ATA	P-ATA, S-ATA II 1.5 Gbps
Ethernet	10/100 Mbps	10/100 Mbps + IEEE1588
USB	OTG + PHY Host + ULPI (x3)	OTG + PHY, Host + PHY Host + ULPI (x2)
Automotive Interface	-	CAN (x2), MLB50
Audio Acceleration	-	ASRC
Audio Interfaces	SSI (x3), S/PDIF Tx	SSI (x3), S/PDIF Tx/Rx, ESAI
Expansion Ports	SD/MMC4.2 (x4) SPI (x3), UART (x3), I2C (x3)	SD/MMC 4.3 (x3) SD/MMC 4.4 (x1) SPI (x3), UART (x5), I2C (x3)

1.1 Product Part Families

Note that both i.MX51 and i.MX53 have individual part families. This means that there are multiple versions of each part with the possibility of different features/modules enabled or disabled in each. Each part in the family is intended for a specific market segment (consumer, automotive or industrial). For

example on i.MX51 (at the time of this publication), the available versions are: i.MX512, i.MX513, i.MX514, i.MX515, and i.MX516. For a complete list of currently available part versions and their included features/modules, refer to the latest datasheet for either i.MX51 or i.MX53.

2 System Core

The i.MX51 and i.MX53 represent two of Freescale Semiconductor's ARM Cortex-A8 based multimedia applications processors. Since they both utilize the ARM Cortex-A8 processor based on the ARMv7 architecture they are flexible enough to meet the requirements for power-optimized devices and performance-optimized consumer applications. Figure 1 shows the basic high-level block diagram of the system core that is representative of both i.MX51 and i.MX53.

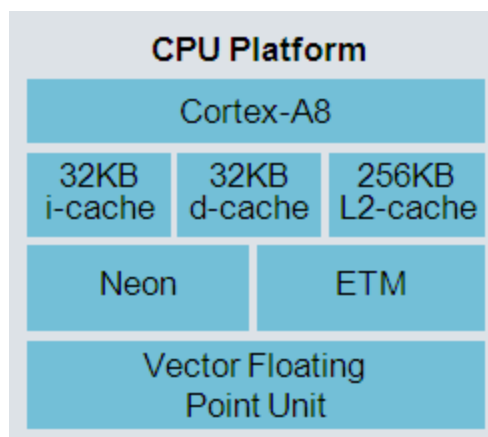


Figure 1. i.MX51 and i.MX53 System Core

The Cortex-A8 processor is a high-performance, low-power, cached application processor that provides full virtual memory capabilities. The features of the processor include:

- Full implementation of the ARM architecture v7-A instruction set
- 64-bit AMBA AXI v1.0 for the main memory interface supporting multiple outstanding transactions, used by the ARM Cortex-A8 platform, major on-chip multimedia accelerators (such as VPU, IPU, and GPU), and the External Memory Interface (EMI).
- A pipeline for executing ARM integer instructions
- Dynamic branch prediction
- Neon co-processor, a 128-bit Single Instruction Multiple Data (SIMD) engine. Using Neon for some audio, video, and/or graphic applications can help distribute workloads across the SoC.
- Optimized Level 1 cache (a 32KB instruction i-cache, and 32KB data d-cache) is integrated tightly into the processor with a single-cycle access time. The cache combines minimal access latency with hash way determination to maximize performance and minimize power consumption.
- Level 2 cache (256KB L2-cache) is integrated into the core for ease of integration, power efficiency, and optimal performance.
- A full Memory Management Unit (MMU) enables the Cortex-A8 to run rich operating systems in a variety of applications. It includes separate instruction and data Translation Look-Aside Buffers (TLBs) of 32 entries each.

- Non-pipelined Vector Floating Point (VFP) co-processor (VFPv3)
- Embedded Trace Macrocell (ETM) support for non-invasive debug

The i.MX53 is a follow-on to the i.MX51 with improved performance, power efficiency, and multimedia capabilities. The ARM Cortex-A8 is a high-performance superscalar microarchitecture that has the ability to scale in speed. This is the key difference between the implementation of the Cortex-A8 in the i.MX51 and i.MX53. [Table 2](#) shows the system core frequency speed differences of i.MX51 compared with i.MX53.

Table 2. iSystem Core Differences i.MX51 and i.MX53

Application	i.MX51	i.MX53
Consumer	up-to 800 MHz	up-to 1.2 GHz
Automotive/Industrial	up-to 600 MHz	up-to 800 MHz

3 Memory

The External Memory Interface (EMI) block that controls all external memory accesses (read/write/erase/program) from all the masters of the system (Cortex-A8, IPU, and VPU) to different external memories has remained almost the same between i.MX51 and i.MX53. There were some significant updates to enhance the performance but the blocks and their general architecture is still very similar between the two. The following sections will highlight the major differences/improvements.

[Figure 2](#) shows the high-level block diagram of the memory interface that is representative of both i.MX51 and i.MX53.

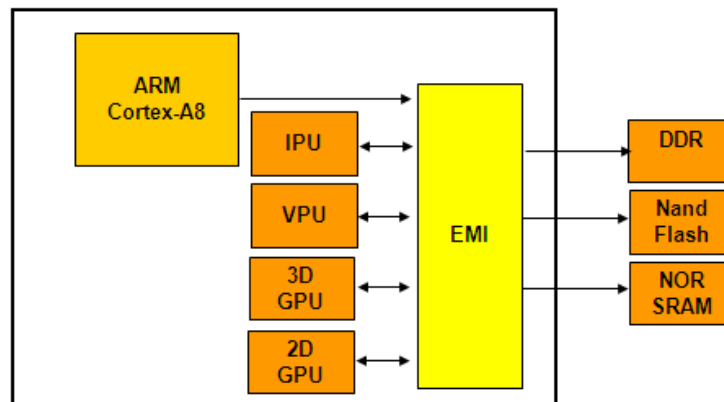


Figure 2. High-Level External Memory Interface Block Diagram

3.1 External DDR

The Enhanced DRAM Controller (eSDCTL) is a sub-block of the EMI which contains all the necessary logic to communicate with external DDR memory. The following are the key differences or improvements implemented on i.MX53:

- Increased address range, up to 2 GB on i.MX53 (1 GB per chip select); up from 512 MB on i.MX51.
- Added LP-DDR2 and LV-DDR2 support
- Added DDR3 support
- Increased DDR bus clock to support speeds up-to 400 MHz (up from 200 MHz on i.MX51)
- Increased internal AXI bus speed to support frequency up-to 200 MHz (up from 166 MHz on i.MX51)

3.2 NAND

The NAND Flash Controller (NFC) is a sub-block of the EMI which is composed of various control logic units, a 4.5Kbyte internal RAM and an internal ECC engine. The NFC can interface standard NAND Flash memory devices. The main functionality and logic behind the i.MX51 and i.MX53 is essentially the same. The key improvement on the i.MX53 is listed below.

- Increased hardware ECC to 14/16-bit (from 8-bit on i.MX51)
- Added a data share mode for NFC and WEIM (NOR/SRAM); in addition to Address/Data sharing.

4 Key Multimedia Hardware Accelerators

To boost multimedia performance both i.MX51 and i.MX53 have some integrated on-chip hardware accelerators. Having built-in multimedia hardware accelerators allows applications to off-load the workload from the core and free it up to perform other tasks.

4.1 Graphics

Both i.MX51 and i.MX53 have similar on chip 2D/3D vector graphics accelerators. These embedded graphics engines help accelerate 2D and 3D graphics operations. The i.MX51 and i.MX53 allow best-in-class vector and 3D rendering since the following hardware accelerators are included on-chip:

- Embedded OpenGL/ES2.0 graphics engine
- Embedded OpenVG1.1 vector graphics engine

Embedded two graphics engines allows:

- Crisp and vivid UIs
- Photo-realistic games
- Advanced browser use cases with great Adobe-Flash user experience
- OpenGL/ES2.0 graphics engine is backwards compatible with OpenGL/ES1.1 and allows smooth upgrade paths.

[Table 3](#) highlights the key differences between i.MX51 and i.MX53 graphics support. The design/implementation of the graphics engines on both i.MX51 and i.MX53 are similar. The key differences include an increased bus speed on the graphics engines to 200 MHz on i.MX53 (up from 166MHz on i.MX51). In addition the dedicated graphics memory GMEM was increased to 256 KB on

i.MX53 (up from 128 KB on i.MX51). These upgrades have resulted in the i.MX53 performance improvements shown in [Table 3](#).

Table 3. Comparative Graphics in i.MX51 and i.MX53

Feature		i.MX51	i.MX53
LCD Support	30 Hz	>1080i (1920x1080)	>1080i (1920x1080)
	60 Hz	SXGA (1280x1024), 720p	UXGA (1600x1200), 1080p
	100 Hz	XGA (1024x768)	WXGA (1366x768)
On-The-Fly-Combining		Single Displays: 3 planes, Two Displays: 2+2 or 3+1 planes More planes through offline processing	
2D Graphics	OpenVG1.1	Accelerated – dedicated OpenVG core	
3D Graphics	OpenGL/ES1.1	Accelerated	
	OpenGL/ES2.0	27M tri/sec, 166 Mpxl/s	33M tri/sec, 200 Mpxl/s
Adobe Flash	Flash Lite	Open VG1.1/H.264 decode	
	Flash 10	OpenGL/ES2.0/H.264 decode	

4.2 Video

Similar to the graphics accelerators, the i.MX51 and i.MX53 both have an embedded Video Processing Unit (VPU). Having an on chip hardware video accelerator gives the features:

- Multi-standard video playback/record
- HD video decode for broadcasting video, video-on-demand, user generated content, and P2P
- HD video encode for video chat
- Video transcoding
- YouTube, Skype, Hulu

Both i.MX51 and i.MX53 have similar VPU architectures. [Figure 3](#) illustrates the key enhancements in the performance of i.MX53 in comparison to i.MX51.

Feature	Format	Profile	i.MX51	i.MX53
Low-Power Audio Decode			SW	SW
Low-Power Video Decode	MPEG-2	Main-High	HW	HW
	H.264	BP/MP/HP	HW	HW
	VC1	SP/MP/AP	HW	HW
	RV10	8/9/10	HW	HW
	MPEG4/Xvid	SP/A SP	HW	HW
	DivX	3/4/5/6	HW	HW
	H.263	P0/P3	HW	HW
	Sorenson H.263	N/A	SW	HW
	SVC, AVS, VP6/7...	N/A	SW	SW
	MJPEG	Baseline	HW, 32MP/sec	HW, 40MP/sec
Low-Power Video Encode	H.264	Baseline	HW, 15Mbps	HW
	H.263	P0/P3	HW, 15Mbps	HW
	MPEG4	Simple	HW, 15Mbps	HW
	MPEG2	Main-Main	HW/SW, 15Mbps	HW/SW
	MJPEG	Baseline	HW, 64MP/sec	HW, 80MP/sec
Video Telephony (SiP, H323) – H.264 BP			HW	HW
Transcode (DLNA) – (M)DMS/(M)DMP			HW	HW
Video de-interlacing			HW	HW
Further Video Processing (deblocking/deringing, resizing, CSC)			HW	HW

Note: in all cases, the HW CODEC meets or exceeds the bit-rate requirements specified in the standards

	1080i/p30, 40 Mbps
	720p30, 20 Mbps
	720p20
	D1 (PAL/NTSC)

Figure 3. iComparative VPU Features of .MX51 and i.MX53

Note: Freescale does not provide the software required for the MPEG2 encode as part of the BSP release.

4.3 Audio

One improvement on i.MX53 over i.MX51 is the addition of the Asynchronous Sample Rate Converter (ASRC) module to the i.MX53. This audio hardware accelerator enables on-the-fly sample rate conversion between various audio streams. The ASRC's main purpose is to convert the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. Figure 4 illustrates the basic high level architecture of the ASRC and its possible sources on i.MX53.

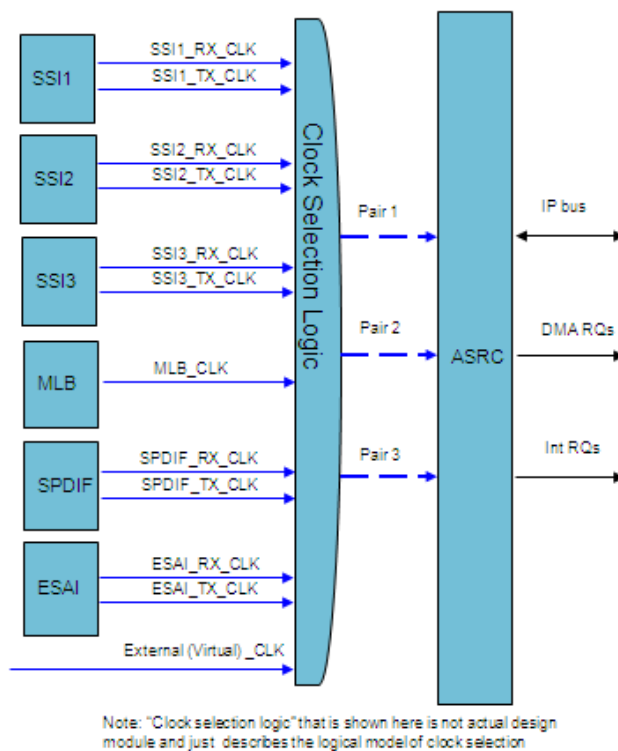


Figure 4. i.MX53 Audio Hardware Accelerator

Some of the ASRC features include:

- Supports concurrent sample rate conversion of up to 10 channels of about -120 dB THD+N
- Supports up-to three sampling rate pairs (as shown in Figure 4).
- Designed for rate conversion between common audio rates 32 kHz, 44.1 kHz, 48 kHz, and 96 kHz (sampling rates which are integer divisors are also supported i.e. 8 kHz, 16 kHz, etc..)
- Other sampling rates in the range of 30 kHz – 200 kHz are also supported but with reduced audio performance.
- Automatic accommodation to slow variations in the incoming and outgoing sampling rates.
- Tolerant to some sample clock jitter.
- 24-bit \leftrightarrow 32-bit re-alignment

5 External Devices

The general purpose modules used to communicate with external devices have remained fairly similar between i.MX51 and i.MX53. There have been some improvements or additions to i.MX53, which in some cases can help reduce the overall BOM costs when designing systems. The sections below will highlight the key differences or improvements.

5.1 Hard Disk Drives (HDD)

In addition to the general external memory interfaces (for example, DDR, NOR and NAND Flash), both i.MX51 and i.MX53 have support for external Hard Disk Drives. They both include a Parallel-ATA (PATA) module. This is an interface standard for the connection of storage devices such as hard disk drives. In addition to HDD support, there is also support for solid state drives, floppy drives, CD-ROM drives, and other devices which use the PATA standard.

The architectural improvement of i.MX53 over i.MX51 is the addition of the on-chip Serial-ATA (SATA) module. SATA is the technology replacement to PATA, and it is now becoming the most common HDD interface in new systems. [Table 4](#) shows the differences between i.MX51 and i.MX53.

Table 4. HDD Interface

i.MX51	i.MX53
P-ATA	P-ATA, S-ATA II 1.5Gbps

5.2 Ethernet

Both i.MX51 and i.MX53 processors, provide external network support through the Fast Ethernet Controller (FEC) module. The FEC module supports both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver functions are required to complete the interface to the media. The FEC supports three different MAC-PHY interfaces for connection to an external Ethernet transceiver: 10/100 Mbps MII, 10/100 Mbps RMII, and the 10 Mbps-only 7-wire interfaces that uses a subset of the MII pins. The key improvement on i.MX53 is the added support for the IEEE 1588 protocol standard.

Table 5. Network Support

i.MX51	i.MX53
10/100Mbps	10/100Mbps + IEEE1588

5.3 Displays

Both i.MX51 and i.MX53 have integrated display controllers that are part of the Image Processing Unit (IPU). The IPU provides comprehensive support for the flow of data from several sources to a display device. It provides related image processing, manipulation, synchronization and control capabilities. The i.MX51 and i.MX53 have similar IPU modules, some of their key features are:

- Hardware implemented image processing routines like scaling, rotation, and post-processing
- Multiple display outputs
- Display quality enhancement: color adjustment, smart gamut mapping, gamma correction and contrast enhancement
- Efficient memory bus utilization: selective read for combining.

- Power efficiency: dynamic backlight power optimization, partial screen refresh from internal frame buffer

The key improvements on i.MX53 over i.MX51 include the addition of integrated LVDS and VGA display ports. This will greatly help to reduce BOM costs in some system designs since both LVDS and VGA options are integrated on-chip for the i.MX53. In addition, the increased internal bus clock speed (200 MHz on i.MX53 in comparison to 166MHz on i.MX51) helps improve performance and possible output resolutions. [Table 6](#) highlights the key improvements.

Table 6. i.MX51 vs i.MX53 Display Support

Feature	i.MX51 (IPUv3EX)	i.MX53 (IPUv3M)
Number of simultaneous outputs	Two: full dual-display support	
Legacy I/F	Parallel (up to 24-bits) and serial up-to two parallel displays (24-bits and 16-bits simultaneously)	Parallel (up to 24-bits) and serial up-to two parallel 24-bit displays simultaneously
LVDS I/F	Through external bridge	Integrated bridge (x2) Up to UXGA (1600 x 1200), or 2xWXGA (1366 x 768) at 60 Hz, 24 bpp
VGA I/F	Through external bridge	Integrated bridge Up to WSXGA (1680 x 1050) at 60 Hz, 24 bpp
Analog TV-out	Composite, S-video and component Up to 720p (1280 x 720) at 60 fps, or 1080i (1920 x 1080) at 30 fps	Rate increased from i.MX51 Up to 1080p (1920 x 1080) at 60 fps
Screen refresh rate	Up to 80 MP/sec For example, SXGA (1280 x 1024) @ 60 Hz or HDTV (1920 x 1080 at 30 fps, or 1280 x 720 @ 60 fps)	Up to 120 MP/sec For example, UXGA (1600 x 1200) or 1080p (1920 x 1080) at 60 Hz
Memory I/F – throughput (clock from IPU to M4IF)	64-bit, 133 MHz	64-bit, 200 MHz

Note: Even though there are many display options (such as x2 LVDS, VGA and Parallel/Serial) only two display channels can be active simultaneously.

5.4 USB

Both i.MX51 and i.MX53 include a high-speed Universal Serial Bus (USB) v2.0 controller and an integrated USB transceiver macrocell interface (UTMI) PHY. The On-the-Go (OTG) USB interface is capable of operating as either a USB device or a USB host. The i.MX51 and i.MX53 contain almost identical USB support, the improvement to i.MX53 was the addition of another PHY interface to one of the HOST ports. All of the USB ports on both i.MX51 and i.MX53 support up to 480Mbps High Speed (HS) standard. [Table 7](#) shows the USB support comparison.

Table 7. USB Support

i.MX51	i.MX53
HS OTG + PHY HS Host + ULPI (x3)	HS OTG + PHY, HS Host + PHY HS Host + ULPI (x2)

6 Miscellaneous Modules and Interfaces

The following section will cover some of the general modules integrated into i.MX51 and i.MX53. For a complete list and a more detailed description of all of the modules and features included in each, refer to the product datasheet and/or reference manual for i.MX51 and i.MX53.

6.1 Automotive

The i.MX51 and i.MX53 have similar architectural implementations. One key area where they differ is in the addition of automotive specific hardware support on i.MX53. The following sections will highlight the new improvements on i.MX53, which will better support automotive focused applications.

6.1.1 Controller Area Network (CAN)

The CAN protocol was originally designed but not limited to be used as a vehicle serial data bus. It meets specific automotive requirements like real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The i.MX53 has two separate integrated FlexCAN modules. This module on i.MX53 is a full implementation of the CAN protocol specification v2.0B, which supports both standard and extended message frames. It also includes a flexible number of message buffers (16, 32, or 64) which are stored in an embedded RAM dedicated to the FlexCAN module for improved performance. The addition of the FlexCAN module on i.MX53 over i.MX51 is a key architectural improvement for automotive focused systems.

6.1.2 Media Local Bus (MLB)

The MLB standard (commonly used in automotive applications) is a multiplexed protocol defined by Standard Microsystems Semiconductor Company (SMSC) to transfer multimedia data between the MOST ring and supporting system level ICs. MOST is a technology that defines mechanisms for sending streaming data and packet-based data and provides a complete application framework to control interaction between devices on the network. The i.MX53 has an integrated MLB module which supports the complete MLB specification which supports up-to 50Mbps. This module offers serial to parallel conversion of the 3-pin MLB signals into 32-bit parallel words and vice versa for transfers to and from system memory. This implementation provides an MLB port for all relevant MLB signals and an application port to interface to the i.MX53. The addition of the MLB module on i.MX53 over i.MX51 is another key architectural improvement for automotive focused systems.

6.2 Audio (ESAI)

In addition to the general audio interfaces included in both i.MX51 and i.MX53 (such as SSI and S/PDIF modules) a new dedicated audio interface was added to i.MX53 to enhance its audio support. The i.MX53 includes the Enhanced Serial Audio Interface (ESAI) module as part of its rich set of multimedia peripherals. The ESAI module provides a full-duplex serial port for communication with a variety of serial devices. The ESAI was designed with two independent transmitter and receiver sections, each with its own clock generator. The ESAI provides the following features:

- Independent (asynchronous mode) or shared (synchronous mode) transmit and receive sections with separate or shared internal/external clocks and frame syncs, operating in master or slave modes
- Up to six transmitters and four receivers
- Programmable data interface modes supported are I2S, LSB aligned, MSB aligned, and AC97 support
- Programmable word length (8, 12, 16, 20 or 24 bits)
- Flexible selection between system clock or external oscillator as input clock source, with programmable internal clock divider and frame sync generation
- Time Slot Mask registers for reduced CPU overhead (for both transmit and receive)
- 128-word transmit FIFO shared with six transmitters
- 128-word receive FIFO shared with four receivers

6.3 General Serial Interfaces

The i.MX51 and i.MX53 processors are geared to be multimedia powerhouses and provide a rich set of hardware accelerators focused on multimedia. In addition to this they also include peripherals for external communications such as UART and I²C. There were some minor architectural improvements in these interfaces between i.MX51 and i.MX53. The changes included updating the version standard that is supported for the module such as in the SD/MMC support, or to the number of module instances included. [Table 8](#) lists some of the general updates between i.MX51 and i.MX53.

Table 8. General Interfaces

i.MX51	i.MX53
SD/MMC v4.2 (x4)	SD/MMC v4.3 (x3), SD/MMC v4.4 (x1)
UART (x3)	UART (x5)
SPI (x3), I2C (x3)	SPI (x3), I2C (x3)

6.4 General Enhancements

6.4.1 IO Voltage Level Support

The i.MX53 also added more flexibility over the supported IO voltage levels on non-DDR pins. The i.MX53 now supports up to 3.3V and has GPIO support on most non-DDR pins. This is an improvement

over the IO voltage level support on i.MX51. For more details on all the pins and their supported voltage levels, refer to the data sheet.

6.4.2 Internal LDOs

Another general enhancement integrated into i.MX53 that is absent on i.MX51 is the addition of on-chip LDO voltage regulators for the PLL supplies. There are two on-chip linear regulators on i.MX53 which provide the option to drive the VDD_ANA_PLL and VDD_DIG_PLL supplies internally (1.8V and 1.2V respectively). When enabled there is no need to drive the supplies externally, by default this option is enabled. The internal LDO voltage is programmable but should not be set outside the target functional range for proper PLL operation. [Table 9](#) shows the internal LDO voltage range.

Table 9. LDO Functional Voltage Range

	Min	Typ	Max
VDD_DIG_PLL	1.15 V	1.2 V	1.3 V
VDD_ANA_PLL	1.7 V	1.8 V	1.95 V

7 Revision History

Table 10 provides a revision history for this application note.

Table 10. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	2/2011	Initial Release.

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