

# MPC564xA Power and Reset

## Including Operation of the On-Chip Regulators and Regulator Controller

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The Qorivva MPC564xA is designed for mid-range gasoline and direct injection engines and advanced transmissions. The Qorivva MPC564xA offers enhanced powertrain functionality, such as on-chip emission control and also addresses the harsh environments of engines and transmissions.

Internally, the MPC564xA requires multiple power supply voltages; however, the device can run from a single 5 V power supply by generating the other voltages from internal regulators and an internal regulator controller. The major power supply for the devices is 5 V, which powers the internal regulators and is used for the pin input and output voltages. In addition, 3.3 V is required for the internal pad prebuffers and flash memory. The majority of the internal logic including the FMPLL is powered by 1.2 V. These voltages can all be generated from the internal regulators and regulator controller. The SRAM has a separate supply input for stay-alive features, if they are wanted. If using the device's external bus or external debug trace features, an external 3.3 V supply is also required.

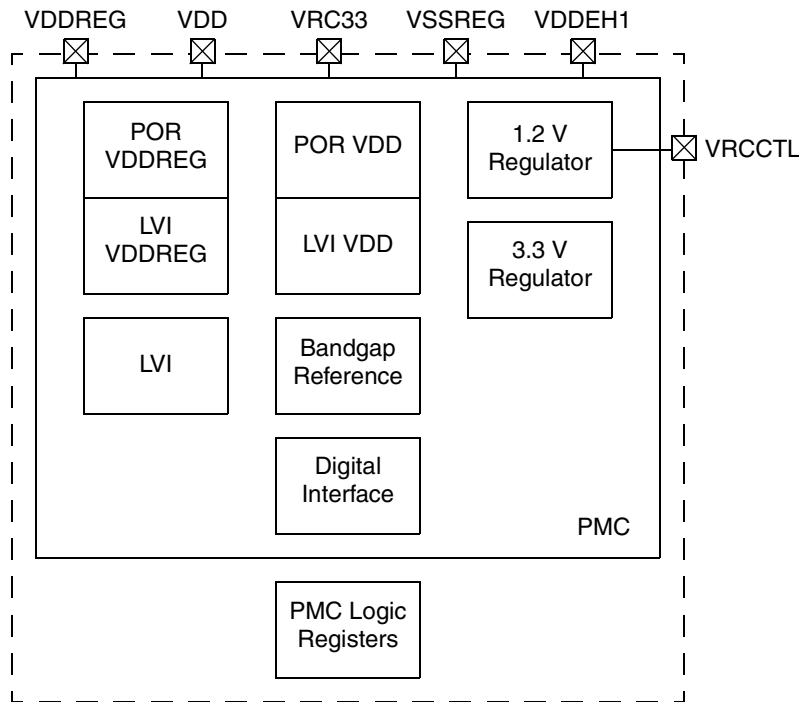
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This application note describes the power supply options for the MPC564xA as well as the required external circuitry for all of the power supplies, including digital supplies, analog supplies, the SRAM standby supply, and the phase-locked loop supply. Also included is a section on the device’s reset configuration options.

# 1 Power Management Controller overview

The MPC564xA power management controller (PMC) handles all of the on-chip voltage regulators, regulator controllers, the low-voltage inhibit (LVI) circuitry, and power-on reset (POR). The figure below shows a simplified block diagram of the PMC.



**Figure 1. MPC564xA PMC block diagram**

The MPC564xA devices have four supply voltage levels, nominally 5 V, 3.3 V, 1.2 V, and 1.0 V (the 1 V supply level is only valid as an option for the power supply for Standby RAM, VSTBY). The PMC controls the internal voltage supplies, with the exception of VSTBY, which has its own regulator.

Externally, only a 5 V supply is required as the other voltages can be supplied by internal regulators.

The PMC contains circuitry to generate the internal 3.3 V supply and to control the regulation of the 1.2 V supply with an external NPN ballast transistor. The PMC also contains low voltage inhibit (LVI) and power-on reset (POR) circuits for the following:

- the 1.2 V supply
- the 3.3 V supply
- the 3.3 V / 5 V supply of the closest I/O segment (VDDEH1)
- the 5 V supply of the regulators (VDDREG)

All of the above supply voltages have voltage monitors. The VDD regulator and all monitors are adjustable. Further details on trimming these regulators can be found in AN4264, *MPC5674F PMC Trimming of Internal Regulators and Low Voltage Detection*.

VDDREG can be tied to VSS to disable the 3.3 V and 1.2 V internal regulators, but doing so also disables the user-programmable LVIs. The 3.3 V regulator can also be disabled by asserting the V33DIS bit in the Non Volatile User Option (NVUSRO) register in the flash memory and resetting the device as described in [Section 3.2, “Using internal and external supplies.”](#)

## 2 Power supply signal properties

The three different package options for the MPC564xA MCU means that there are a different number of pins available for the power supplies, depending on the package. It also means that in some cases, some supplies are not available external to the device. The signal properties table in MPC5644ARM, *MPC5644A Microcontroller Reference Manual* and MPC5644A, *MPC5644A Microcontroller Data Sheet*, shows which supplies are available on each package. All supply pins that are available on the package should be connected to a supply voltage.

### 2.1 Regulator supply

[Table 1](#) describes all pins related to the regulator power supply.

**Table 1. MPC564xA regulator supply pins**

Signal Name	Nominal Voltage	Direction	Description
VDDREG	5V	Input	VDD regulator input—source voltage for on-chip regulators and low-voltage detect circuits.
VDD	1.2V	Input	Internal logic supply—core supply for input or decoupling, nominally 1.2 V. Can be powered by the 1.2 V internal regulator controller or an external 1.2 V supply.
VRCCTL	—	Output	Regulator control is the output from the regulator that controls the external bypass transistor for the 1.2 V regulator. This is a current that is varied to change the gain of the external NPN transistor to hold a constant voltage on the transistor emitter (connected to the VDD signals).
VRC33	—	Output	Internal regulator output to bypass capacitor or external power supply.
VSS	Ground	Input	Ground pin.

In the case where there are multiple pins with the same signal name—VDD, for example—they can be connected together.

### 2.2 I/O supply

The MPC564xA allows flexibility in the selection of voltage levels on many of the supplies that power input and output pins. These supplies are labeled VDDE or VDDEH and are broken into segments. Each segment can be connected to different supply voltages if required. The VDDE supplies are generally 3.3 V (nominal voltage) or lower. The VDDEH supplies are “high” supplies and can be connected to either a

## Power supply signal properties

nominal 3.3 V or 5.0 V. Alternate functions are powered by the supply that powers the primary function of each signal.

The following table shows all pins related to the I/O supply.

**Table 2. MPC564xA I/O supply pins and segmentation**

Signal Name	Nominal Voltage	Direction	Description
VDDEH1	3.3–5 V	Input	eTPU A: eTPUA[10:31]
VDDE2	3.0–3.3 V	Input	EBI: CS[0:3], RD_WR, BDIP, WE[0:1], OE, TS, TA
VDDE3	9.0–3.3 V	Input	EBI: ADDR[12:15]
VDDEH4	3.3–5 V	Input	EMIOS: EMIOS[0:23] eTPUA: eTPUA[0:9], TCRCLKA
VDDE5	3.0–3.3 V	Input	EBI: DATA[0:15] Reset and Clocks: CLKOUT and ENGCLK
VDDEH6	3.3–5 V	Input	FlexCAN A and B: CNTXA, CNRXA, CNTXB, CNRXB ESCI A, B and C: TXDA, RXDA, TXDB, RXDB, TXDC, RXDC DSPI B: SCKB, SINB, SOUTB, PCSB[0:6] Reset and Clocks: XTAL, EXTAL, RESET, RSTOUT, PLLREF, PLLCFG1, RSTCFG, BOOTCFG[0:1], WKPCFG
VDDEH7	3.3–5 V	Input	EMIOS: EMIOS[14:15] GPIO: GPIO[98:99], GPIO[203:207], GPIO[219] JTAG and Nexus: EVTI, EVTO, MCKO, MDO[0:15], MSE[0:1], TCK, TDI, TDO, TMS, RDY, JCOMP <sup>1</sup> DSPI A: SCKA, SINA, SOUTA, PCSA[0:5] EQADC: AN[12:15]
VDDE-EH	3.0–5 V	Input	EBI: ADDR[16:31]
VDDE12	3.0–3.3 V	Input	Calibration Bus: CAL_CS[0:3], CAL_ADDR[12:30], CAL_DATA[0:15], CAL_RD_WR, CAL_WE[0:1], CAL_OE, CAL_TS

<sup>1</sup> For proper operation, the JTAG and Nexus Pins require that VDDEH7 be 5.0 volts.

It is possible to switch off the 3.3 V supplies for VDDE given the following conditions:

- all segment supply pins are pulled up to 5 V through a weak pull-up
- no I/O pins are toggling while the supply is off, and
- no wakeup pins are used on that segment.

This supply cannot be completely turned off as there are internal parasitic paths present which could lead to the supply partially turning on.

### NOTE

VDDEH7 is the I/O ring supply for some of the ADC I/O channels. Since ADC channels can operate in the range from 0 V to VDDA, the ADC I/O supply cannot be different from the analog supply, VDDA, otherwise the MPC564xA could have spurious current paths in design. For example, if VDDEH7 is 3.3 V, VDDA is 5 V, and channel voltage is 5 V, the ESD diodes in VDDEH7 segment will get forward biased. For proper operation of JTAG and NEXUS, VDDEH7 should always be 5 V.

## 2.3 Standby supply

The VSTBY pin is the SRAM standby supply; that is, it is the power supply input that is used to maintain a portion of the contents of internal SRAM during power-down. Further description of this supply can be found in [Section 3.3, “SRAM standby supply.”](#)

## 2.4 PLL supply

The VDDPLL input pin is the FMPLL supply voltage. The nominal voltage on the MPC564xA is 1.2 V. This is different from some other Qorivva products, such as the MPC567xF, which supply the PLL with 3.3 V through VDDSYN. This supply can be sourced from VDD if the internal 1.2 V regulator controller is enabled.

## 2.5 Analog supply

The following table shows all pins related to the analog power supply, solely for the eQADC module.

**Table 3. MPC564xA analog supply pins**

Signal Name	Nominal Voltage	Direction	Description
VDDA	5 V	Input	eQADC supply
VSSA	Ground	Input	eQADC ground supply

On the 176 pin package there is one pair of VDDA and VSSA. On the larger pin count packages there are two pairs of VDDA and VSSA, VDDA0/VSSA0 and VDDA1/VSSA1. Each VDDA on the device should have a 10 uF and a 10 nF capacitor pair close to the pin. An 8 ms wait time from VDDA power up to the enabling of the eQADC is required to pre-charge the external capacitor on REFBYPC pin. This time must be guaranteed by crystal startup time plus reset duration.

### NOTE

VRH, VRL and REFBYPC are voltage references and external 100nF bypass capacitor pins for the eQADC, but do not supply power. VRL and VRH should be decoupled with 10nF and 100nF capacitors.

## 3 Power supply options

The MPC564xA MCU is designed for a wide range of applications. Based on system requirements and available power supplies, some applications may require different methods of powering the device.

[Table 4](#) below summarizes the options available for powering the MPC564xA.

**Table 4. MPC564xA power supply options**

Configuration	VDDREG	3.3 V supply (VRC33)	VRC33 is a . . .	1.2 V regulator controller	VRCCTL is a . . .	V33DIS <sup>1</sup>
<b>Figure 2:</b> Internal regulators used	5 V	Internal	3.3 V output	Internal	1.2 V output	0
Internal 3.3 V regulators used, 1.2 V supplied externally without ballast transistor	5 V	Internal	3.3 V output	External	NC	0
<b>Figure 4:</b> External regulated 3.3 V supply used without disabling the internal regulator (LVI monitor active)	5 V	External	input 3.3 V	Internal	1.2 V output	1
External regulated 3.3 V and 1.2 V supply used with a disabled internal regulator (LVI monitor enabled)	5 V	External	input 3.3 V	External	NC	1
External regulated 3.3 V and 1.2 V supply used with a disabled internal regulator (LVI monitor disabled)	3.3	External	input 3.3 V	External	NC	1
<b>Figure 5:</b> VDDREG supply grounded (PMC and LVI off)	0 V	External	input 3.3 V	External	NC	—

<sup>1</sup> See Section 3.2 for a description of V33DIS

Three of these options are shown as figures in the later sections of this document. The other two can be derived from the figures and descriptions.

### 3.1 Using the 3.3 V internal regulator and 1.2 V regulator controller

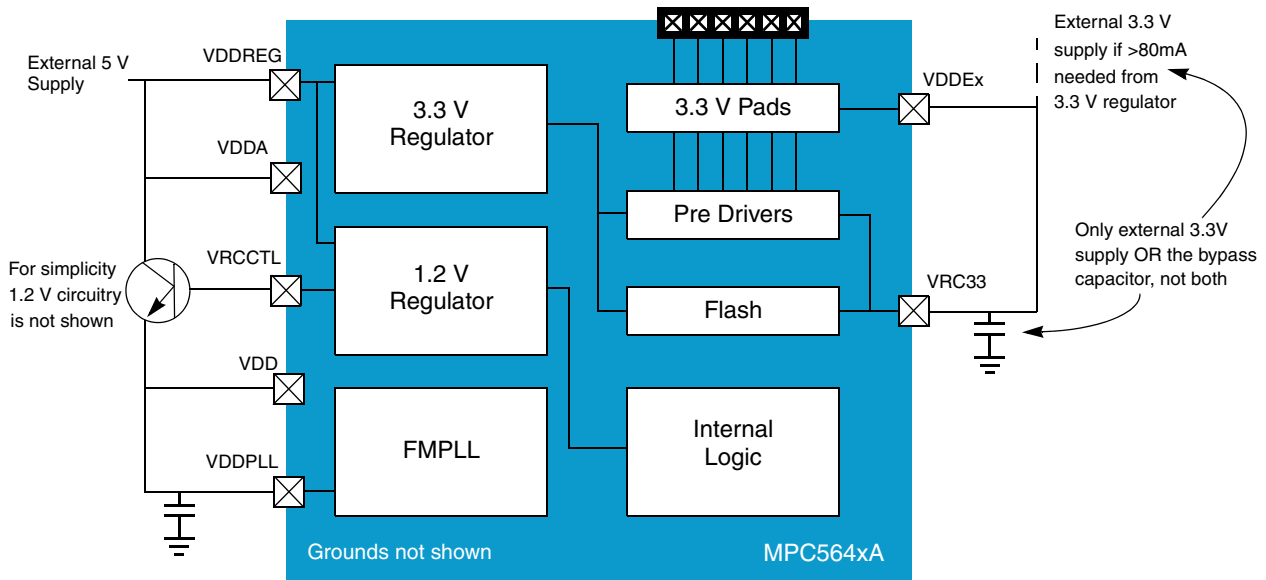
The MPC564xA contains an internal regulator that can be used to generate 3.3 V from the main VDDREG supply. A regulator controller is available for the low-voltage supply (1.2 V). External capacitors are required for both the 3.3 V and the 1.2 V supplies. Additional external circuitry is required for the 1.2 V regulator controller including an external ballast transistor.

#### 3.1.1 Internal 3.3 V regulator

A 3.3 V regulator is fully contained within the device. This regulator is enabled automatically if VDDREG is greater than 4.5 V as illustrated in [Figure 2](#) below. If VDDREG is less than 4.5 V, then the 3.3 V regulator is disabled and the 3.3 V supply (VRC33) should be powered from an external supply as shown in [Figure 4](#).

The internal 3.3 V regulator can only provide up to 80 mA of current. Therefore, it is not large enough to provide power to either the external development bus or the Nexus trace signals. When using the external bus, FlexRay, or Nexus trace, an external 3.3 V supply is required.

The PMC's 3.3 V supply sense signal is connected internally to the output of the internal 3.3 V regulator, VRC33. Therefore, when using the internal 3.3 V regulator, VDDE and VRC33 must be connected with as little inductance as possible on the target circuit board.



**Figure 2. Typical external 5 V supply configuration**

**NOTE**

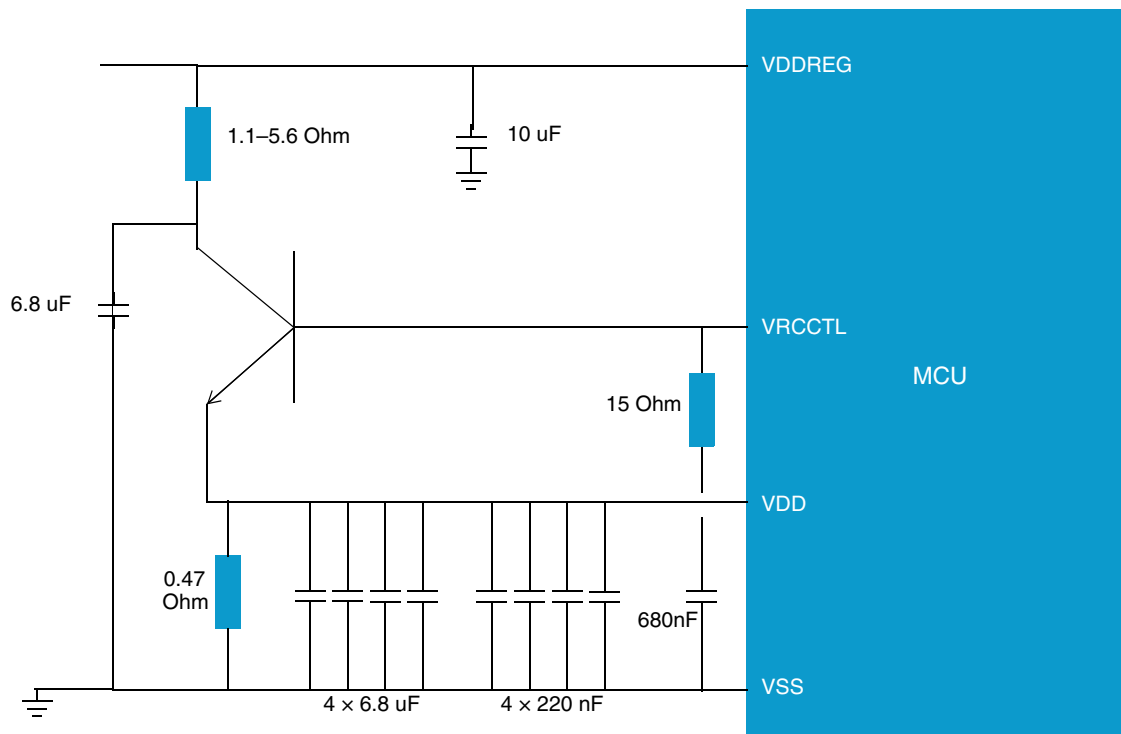
The latest version of MPC5644A, *MPC5644A Microcontroller Data Sheet*, should be consulted for the latest specifications regarding external components and voltage ranges.

Connecting VRC33 and VDDEx requires an external bypass capacitor in the range of 600 nF to 2  $\mu$ F. When using an external 3.3 V for the pins' supply the external bypass capacitor is not required.

The bypass capacitor shown on VDDPLL has been simplified for the sake of clarity, and should be a 10nF and 100nF in parallel.

**3.1.2 Internal 1.2 V regulator**

The majority of the internal circuitry in the MCP564xA operates on a 1.2 V nominal supply voltage. The device includes an on-chip regulator controller for providing this voltage. The linear regulator circuit provides a low-noise, stable 1.2 V supply, but requires a significant amount of current and power dissipation. The linear 1.2 V regulator controller requires an external transistor and bypass capacitors. It operates in a closed loop mode. Care is needed to ensure that the switching frequency is isolated from any noise-sensitive circuitry in the target system. [Figure 3](#) below shows the typical configuration of the regulator circuit which can also be found in MPC5644A, *MPC5644A Microcontroller Data Sheet*, along with the characteristics of the bipolar NPN pass transistor. One of the four pairs of 6.8  $\mu$ F and 200 nF capacitors should be placed on each corner of the MCU.



**Figure 3. Core voltage regulator controller external components**

**NOTE**

The latest version of MPC5644A, *MPC5644A Microcontroller Data Sheet*, should be consulted for the latest specifications regarding external components.

**3.1.2.1 1.2 V regulator recommended components**

The recommended bipolar NPN pass transistors are the NJD2873 (for particularly high current draw applications) or a generic BCP68 transistor (sufficient for lower power applications). Care needs to be taken when selecting a BCP68 transistor to ensure that it meets the circuit's requirements over the whole temperature range and that it operates away from the saturating level. It will require a series resistor to assist in the power handling of the drop from 5 V to 1.2 V. Proper heat-sinking is also needed. The NJD2873 has been specified to meet the requirements for the MPC5500 and MPC5600 devices and is therefore the preferred transistor. In addition, the NJD2873 is in a DPAK package that allows a higher power dissipation. The typical package for the BCP68 is the SOT-223-4. Additional information on how to make the correct transitory selection for your applications current profile can be found in AN3254, *Power Supplies on the MPC5500*.



## 3.2 Using internal and external supplies

An externally regulated 3.3 V supply can be used in tandem with the internal 1.2 V linear regulator. Figure 4 below shows this configuration; however, it does not show all of the external 1.2 V circuitry. See Section 3.1.2, “Internal 1.2 V regulator” for the complete requirements.

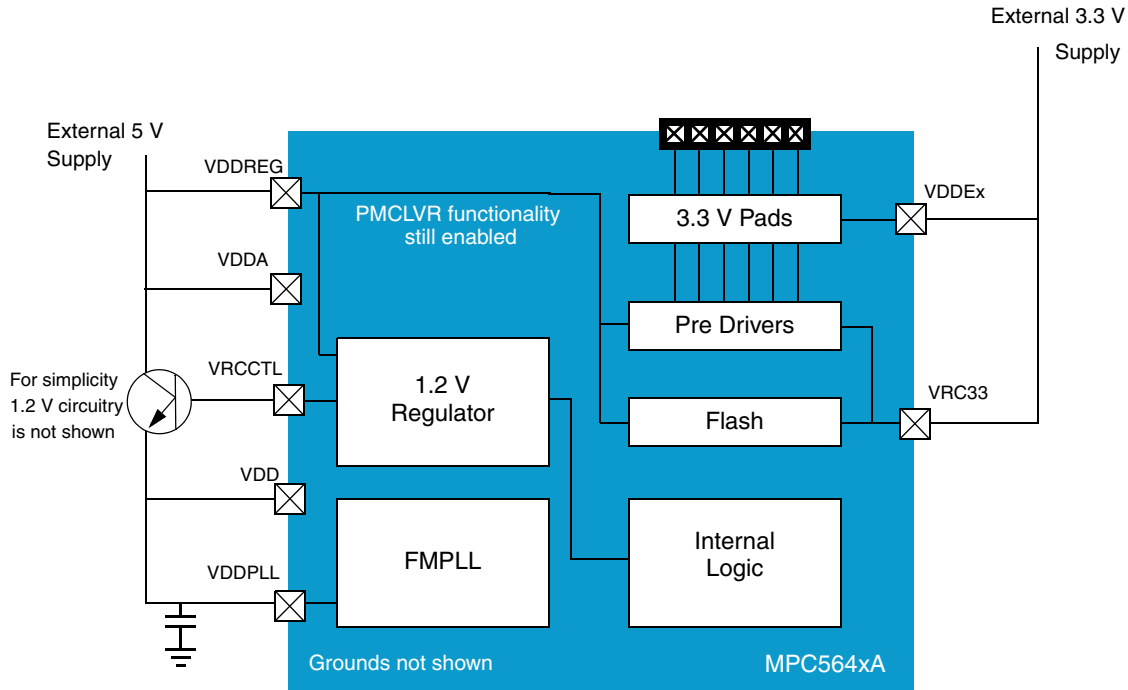


Figure 4. Typical external 3.3 V (only) supply configuration

### NOTE

The latest version of MPC5644A, *MPC5644A Microcontroller Data Sheet*, should be consulted for the latest specifications regarding external components.

The V33DIS bit, located in the Non Volatile User Option (NVUSRO) register in flash memory, controls whether the internal 3.3 V regulator is enabled. The PMC Status Register also contains a read-only V33DIS bit which is read only and indicates whether the regulator is shut down. Setting V33DIS in NVUSRO does not deactivate the 3.3 V regulator until the next POR event which means that this Disable Internal Regulator software request is not initiated until the 1.2 V POR trip point is reached after the POR. While the device is recovering from the POR, the 3.3V regulator circuitry is disabled and the V33DIS bit in the PMC Status Register is updated to reflect the regulator’s status. This means that if you wish to disable the regulator in this configuration you must first power on the device, set V33DIS, and then reset. To disable the 3.3 V LVR circuitry from the outset, VDDREG must be grounded as shown in Figure 5.

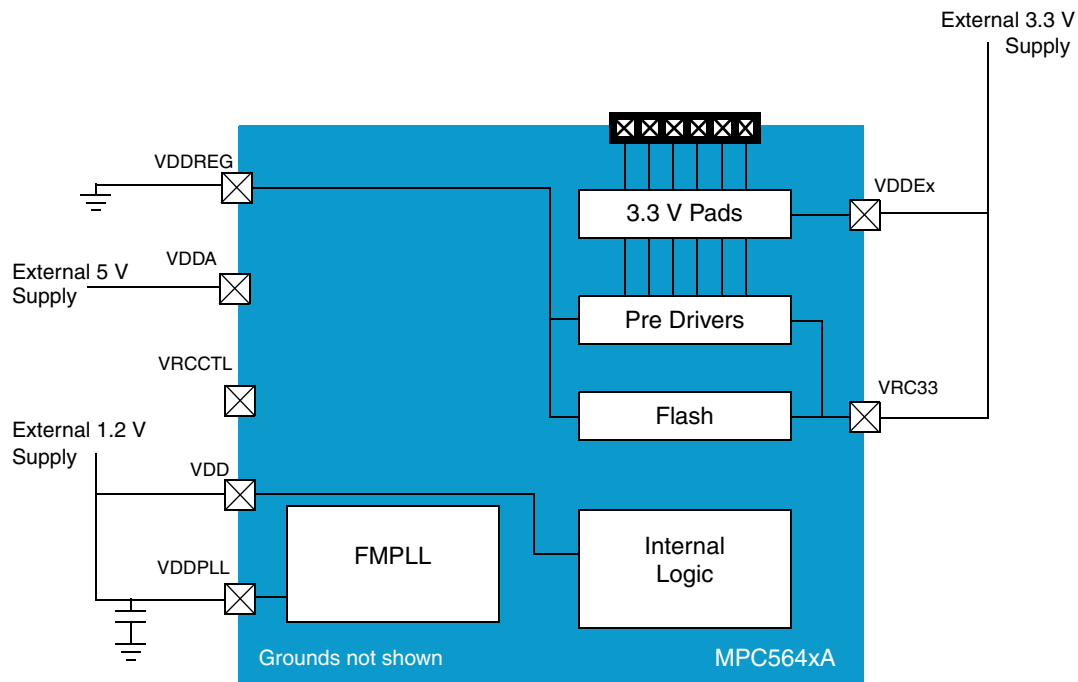
**NOTE**

In some instances, a software requirement to disable the internal power supply may cause two 3.3 V supplies to be active at the same time. Power supplied by an external 3.3V regulator in to VRC33 pins while the internal 3.3 V regulator is also enabled is acceptable as long as the external 3.3 V supply remains within the specification for VRC33.

External 3.3 V supply specification overshoots are likely to cause damage to the internal circuits of the MCU. For more information on the allowed range, refer to the absolute maximum ratings in MPC5644A, *MPC5644A Microcontroller Data Sheet*.

While external 3.3 V supply specification undershoots are unlikely to damage the device, functionality of the MCU cannot be guaranteed under these conditions.

The MPC564xA can be powered totally by external supplies. The 3.3 V internal regulator is disabled by connecting VDDREG to ground (0 V). As an external 1.2 V supply will also be used, VRCCTL should be left open as shown in Figure 5. To use the eQADC module in this configuration, VDDA must be connected to a 5 V supply.



**Figure 5. Typical external 3.3V and 1.2V supply configuration**

**NOTE**

The latest version of MPC5644A, *MPC5644A Microcontroller Data Sheet*, should be consulted for the latest specifications regarding external components.

### 3.3 SRAM standby supply

The MPC564xA includes a power supply option for maintaining the contents of a portion of the internal SRAM when power to the rest of the device is off.

There are two options for the VSTBY power supply to provide power to the SRAM when the main device power supplies are turned off.

When the VSTBY pin is between 0.95 V and 1.2 V the voltage powers the SRAM directly when VDD is powered off. If VSTBY is between 2.0 V and 5.5 V, an internal standby regulator is enabled and this supply provides power to the SRAM when VDD is off.

If the SRAM standby feature is not required in the system, the best option is to connect the VSTBY pin to ground which completely disables the standby SRAM function. It is also possible to connect VSTBY to either an external 3.3 V supply or to the 5 V supply that powers the rest of the device.

#### NOTE

VSTBY must not be left floating. If VSTBY is left floating and floats to a voltage above 1.2 V, but less than 2.0 V, access to the SRAM will be disabled. If the voltage floats above 2.0 V, it is likely that insufficient current will be available to power the internal standby regulator which could cause the standby supply to float to a level that will disable access to the SRAM. The assumption in the device is that if the standby voltage to the SRAM is the same or higher than the VDD supply voltage, the VDD supply voltage must be powering down and therefore the SRAM should be disabled to prevent corruption of the SRAM data.

The table below shows the electrical specifications for VSTBY; however, the latest version of the device data sheet should be consulted.

**Table 5. SRAM standby operation**

Characteristic	VSTBY connection	Minimum	Maximum
No SRAM standby	Ground	0 V	0.2 V
—	Illegal Range	0.2 V	0.95 V
SRAM Standby	Standby Regulator Disabled	0.95 V	1.2 V
—	Illegal Range	1.2 V	2.0 V
SRAM Standby	Standby Regulator Enabled	2.0 V	5.5 V

If the proper voltage is on VSTBY, then VSTBY will provide power to the SRAM anytime the device is in power-on reset (POR). POR is an internal signal that is asserted if any of the monitored supplies are lower than their specified values.

## 4 Device reset configuration

The basic configuration of the FMPLL, boot location, and weak pull resistors are set during reset. The states of the control pins for these features are latched four clocks prior to the negation of the  $\overline{\text{RSTOUT}}$  input of the device. The following table shows all of the reset configuration pins.

**Table 6. Boot configuration I/O**

Pin	Function	Dependency
BOOTCFG[0:1]	Boot Configuration Input	BOOTCFG0 only on 324 package, 208 and 176 always 0
PLLREF	Clock Generation Configuration Input	RSTCFG
WKPCFG	Weak Pull Configuration Input	None
RSTCFG	Reset Configuration	Only on 324 package, 208 and 176 are always 0

Since multiple external devices could assert the MCU  $\overline{\text{RESET}}$  signal (power supply reset out, debugger, external independent watchdog), all devices connected to  $\overline{\text{RESET}}$  should be configured for open drain (or open collector depending on the technology) with a strong pull-up (less than 4.7 K) resistor installed in the system on the  $\overline{\text{RESET}}$  signal.

## 4.1 Boot configuration

Once the Boot Assist Module (BAM) has configured the MMU, the BAM program checks the BOOTCFG field of the reset status register (RSR) which was loaded with the levels of the BOOTCFG[0:1] pins during the reset.

The BAM program uses the BOOTCFG[0] bit to determine where to read the reset configuration word, and whether to initiate a FlexCAN or eSCI boot. For the 176-pin QFP and 208-ball BGA MPC564xA packages, BOOTCFG[0] is always 0 since the EBI interface is not available.

The BOOTCFG[1] pin is sampled during the assertion of the  $\overline{\text{RSTOUT}}$  signal, and the value is used to update the RSR and the BAM boot mode.

In the normal boot process, the BAM looks for a valid Reset Configuration Half-Word (RCHW) in the internal flash at the various possible boot locations. If a valid RCHW is not found, then serial boot mode is entered.

**Table 7. Boot mode selection**

BOOTCFG[0:1]	Censorship Control	Serial Boot Control	Boot Mode	Flash	Nexus	Password
00	Other Values	Any Value	Internal—Censored	Enabled	Disabled	Flash
	0x55AA		Internal—Public	Enabled	Enabled	Public
01	Any Value	0x55AA	Serial—Flash Password	Enabled	Disabled	Flash
		Other Values	Serial—Public password	Disabled	Enabled	Public
10	Other Values	Any Value	External without arbitration—Censored	Disabled	Enabled	Public
	0x55AA		External without arbitration—Public	Enabled	Enabled	Public
11	Illegal					

Serial boot mode allows the device to boot over either the eSCI (a simple, standard RS-232 D type interface) or via the FlexCAN module.<sup>1</sup> Both interfaces are monitored until activity is seen on one interface. Once an initial activity is seen on an interface, that interface becomes the boot interface. The

boot protocol allows software to be downloaded into the device via the serial interface. Control will be passed to that software once loaded into memory. See the documentation for each device for additional information on the serial boot process.

## 4.2 FMPLL configuration

The default configuration of the PLL is set by the PLL configuration pins of the device: PLLREF and RSTCFG. The CLKCFG[0:2] bit field sets the basic PLL operating mode as shown in [Table 8](#) below.

**Table 8. Clock mode selection**

CLKCFG[0]	CLKCFG[1]	CLKCFG[2]	Clock Mode
0	0	0	Bypass mode with external reference and PLL off
0	0	1	Bypass mode with crystal reference and PLL off
0	1	0	Bypass mode with external reference and PLL running
0	1	1	Bypass mode with crystal reference and PLL running
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Normal mode with external reference
1	1	1	Normal mode with crystal reference

CLKCFG[0] is zero after a reset event, meaning the FMPLL is bypassed and the FMPLL is disabled. CLKCFG[1] is set after a reset event, meaning the FMPLL is enabled.

The state of the CLKCFG[2] bit is determined by the logical state applied to the PLLREF pin during reset which is readable from the FMPLL Enhanced Synthesizer Control Register, ESYNCR1; therefore, the PLLREF input must be kept stable while system reset is asserted.

On the 324 BGA package there is also an RSTCFG pin that effectively locks the FMPLL reference selection in to crystal oscillator mode when set; that is, when RSTCFG is high, the FMPLL reference is the XTAL oscillator regardless of the level of PLLREF. When RSTCFG is not bonded out on to the package, it is tied to zero internally giving selection control the PLLREF pin.

After reset, the mode can be changed by writing to the CLKCFG field in the ESYNCR1 register.

The MPC564xA device has a pin labelled as PLLCFG1 to be compatible with other devices in the family but this pin has no FMPLL configuration functionality.

## 4.3 Weak pull configuration

The default configuration of the pull devices connected to the timer pins of the device can be controlled with the state of the Weak Pull Configuration pin (WKPCFG) during reset. The value of this signal is latched by the device four clocks prior to the negation of RSTOUT (low to high transition). The pull device

1. The eSCI Rx/D input pin requires an external pull resistor. It is possible to prevent FlexCAN boot if the start bit (low) is detected on Rx/D.

## Power-on reset

can either be a pull-up or a pull-down. This default value remains in effect until changed in the Pad Configuration Register (PCR) for the signal.

When a pin is configured as an output, the weak internal pull up/down is disabled regardless of the Weak Pull Enable (WPE) or Weak Pull Select (WPS) settings in the SIU\_PCR and Weak Pull Configuration Pin (WKPCFG) level.

**Table 9. Weak pull configuration**

Power Supply	Description
0	The pins controlled by the WKPCFG will have pull DOWN devices enabled by default
1	The pins controlled by the WKPCFG will have pull UP devices enabled by default

## 5 Power-on reset

The PMC controls the power-on reset (POR) for the MCU. When the critical<sup>1</sup> power supplies are below minimum levels, the MCU is held in a reset state. The PMC POR holds the device in reset until the power supplies have reached a level high enough so that the  $\overline{\text{RESET}}$  input can be propagated through the device. The key supplies are the 1.2 V core voltage, VDDREG regulator input voltage, and the VDDEH6 power supply that powers the  $\overline{\text{RESET}}$  pin. During POR, the device I/O pins are held in a safe state that depends on which power supplies are on and which are turned off. This is shown in the Power up/down sequencing section of MPC5644A, *MPC5644A Microcontroller Data Sheet*.

**Table 10. Supply signals that control POR assertion**

Power Supply	Data Sheet Symbol	Parameter	Minimum	Typical	Maximum
VDD	Por1.2V_r	POR 1.2V rising	Por1.2V_r – 35%	0.709 V	Por1.2V_r + 35%
	Por1.2V_f	POR 1.2V falling	Por1.2V_f – 35%	0.638 V	Por1.2V_f + 35%
VDDREG	Por5V_r	POR 5V rising	Por5V_r – 35%	2.6 V	Por5V_r + 50%
	Por5V_f	POR 5V falling	Por5V_f – 35%	2.4 V	Por5V_f + 50%
VDDEH6	—	RESET low-voltage detect (Enabled during reset)	2.0 V	—	3.0 V

### NOTE

The latest version of the MPC564xA Data Sheet should be consulted for the latest specifications.

Full device operation is not guaranteed at this voltage, only that the  $\overline{\text{RESET}}$  signal will be able to propagate through the device.

If all external power supplies are being used, VDDREG, which powers the internal regulators, is not a factor in the POR sequence.

During the initial POR, the voltage on VDDEH6 (the power supply that powers the  $\overline{\text{RESET}}$  input), as well as several other supplies, also control the exit of the power-on reset. After the MCU exits reset, user

1. *Critical* is defined as sufficient voltage to allow reset to propagate through the device.

software can enable even more supplies to cause a reset assertion if the supply dips below the specified voltages. The PMC Configuration bits shown in Table 11 affect the internal  $\overline{\text{RESET}}$  assertion initially after a POR (and consequently the  $\overline{\text{RSTOUT}}$  output), the first assertion of reset during POR, and also the Low Voltage Detect (LVD) circuits. The LVDs can also be set to cause an interrupt. These are also shown in the table. They can be enabled or disabled by the user in software.

**Table 11. Low voltage reset control bits in PMC\_MCR**

PMC_MCR Bit	Description	Default Setting
LVRER	Reset supply (VDDEH6) low-voltage reset enable	1 (LVI causes reset)
LVREH	VDDEH low-voltage reset enable	0 (LVI does not cause reset)
LVR50	VDDREG low-voltage reset enable	0 (LVI does not cause reset)
LVR33	VDDPLL (3 V) low-voltage reset enable	1 (LVI causes reset)
LVRC	Core-voltage-supply VDD (1.2 V) low-voltage reset enable	1 (LVI causes reset)
LVIER	Reset supply (VDDEH6) low-voltage interrupt enable	0 (Interrupt request disabled)
LVIEH	VDDEH low-voltage interrupt enable	0 (Interrupt request disabled)
LVI50	VDDREG low-voltage interrupt enable	0 (Interrupt request disabled)
LVI33	VDDPLL (3 V) low-voltage interrupt enable	0 (Interrupt request disabled)
LVIC	Core-voltage-supply VDD (1.2 V) low-voltage interrupt enable	0 (Interrupt request disabled)

**NOTE**

Please note that in the MPC564xA devices, an LVI reset (LVR) is equivalent to a POR in the Reset Status Register (RSR).

## 5.1 Power up/down sequencing

As long as the following rule is met, there is no power sequencing required among power sources during power up and power down in order to operate within specification

- When VDDREG is tied to a 5 V supply, VRC33 must be powered by the internal 3.3 V regulator.

### 5.1.1 Power up

The recommended power up supply behavior is as follows: Use 25 V/millisecond or slower rise time for all supplies. Power up each VDDE/VDDEH first and then power up VDD.

If VDDE/VDDEH is powered up first, then a threshold detector three-states all drivers connected to VDDE/VDDEH. There is no required wait time between VDDE/VDDEH and VDD power up. If there are multiple VDDE/VDDEH supplies, they can be powered up in any order. For each VDDE/VDDEH supply not powered up, the drivers in that VDDE/VDDEH segment exhibit the characteristics described in the next paragraph.

If VDD is powered up first, all pads are loaded through the drain diodes to VDDE/VDDEH. This presents a load that pulls the pad down to a diode above VSS. Current injected by external devices connected to the pads must meet the current injection specification. If there is no injected current, or if the injected current

## Summary

is within the specified limit, there is no issue with this power up sequence. There is no limit to how long after VDD powers up before VDDE/VDDEH must power up.

### 5.1.2 Power down

The recommended power down supply behavior is as follows: for power down, drop VDD to 0 V first, and then drop all VDDE/VDDEH supplies. There is no limit on the fall time for the power supplies. This is a recommendation and not an absolute requirement for correct operation.

If VDD is powered down first, then all drivers are three-stated. There is no limit to how long after VDD powers down before VDDE/VDDEH must power down.

If VDDE/VDDEH is powered down first, then all pads are loaded through the drain diodes to VDDE/VDDEH. This presents a heavy load that pulls the pad down to a diode above VSS. Current injected by external devices connected to the pads must meet the current injection specification. There is no limit to how long after VDDE/VDDEH powers down before VDD must power down.

### 5.1.3 Power sequencing and POR dependent on VDDA

During power-up or power-down, VDDA ramp up is allowed to lag the other power supplies by up to 1 V, to prevent any forward-biasing of device diodes that causes leakage current and/or POR. If the voltage difference between VDDA and VDDEH is more than 1 V, the following will result:

- Triggering of POR (ADC monitors on VDDEH1 segment which powers the  $\overline{\text{RESET}}$  pin) if the leakage current path created, when VDDA is sufficiently low, causes sufficient voltage drop on VDDEH1 node monitored crosses low-voltage detect level.
- If VDDA is between 0–2 V, powering all the other segments (especially VDDEH1) will not be sufficient to get the part out of reset.
- Each VDDEH will have a leakage current to VDDA of a magnitude of  $((\text{VDDEH} - \text{VDDA} - 1 \text{ V (diode drop)})/200 \text{ K})$  up to  $(\text{VDDEH}/2 = \text{VDDA} + 1 \text{ V})$ .
- VDD has the same behavior; however, the leakage will be small even though there is no current limiting resistor since  $\text{VDD} = 1.32 \text{ V max.}$

## 6 Summary

This application note has shown the different power supply options for the internal 3.3 V regulator and the 1.2 V regulator controller as well as some information on the board-level pin configuration options for controlling the reset configuration on the MPC564xA device. It has explained options and trade-offs that must be considered when developing the MPC564xA application and hardware.



## 7 Revision history

Table 12 describes changes and revisions to this document.

**Table 12. Revision history**

Revision	Description of changes
0	Initial version
1	<ul style="list-style-type: none"> <li>• <a href="#">Table 2</a>: nominal voltage for VDDE2, VDDE3, VDDE5, and VDDE12 changed from “1.8–3.3V” to “3.0–3.3V.” Changed “EMIOS” to “EBI” in VDDE5 description. Added the following footnote: “For proper operation, the JTAG and Nexus Pins require that VDDEH7 be 5.0 volts.”</li> <li>• <a href="#">Section 4.1, “Boot configuration”</a>: added the following footnote: “The eSCI RxD input pin requires an external pull resistor. It is possible to prevent FlexCAN boot if the start bit (low) is detected on RxD.”</li> <li>• <a href="#">Section 4.2, “FMPLL configuration”</a>: added PLL configuration pin names (PLLREF and RSTCFG). Changed “CLKCFG[0:1]” to “CLKCFG[0:2].”</li> <li>• <a href="#">Section 5, “Power-on reset”</a>: added the following note: “If all external power supplies are being used, VDDREG, which powers the internal regulators, is not a factor in the POR sequence.”</li> <li>• Editorial changes and improvements.</li> </ul>

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