## Abstract
This application note provides guidelines for the handling and board mounting of NXP’s QFP packages including recommendations for printed-circuit board (PCB) design, board mounting, and rework.

### Document information

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<th>Information</th>
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<tr>
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<td>quad flat package QFP</td>
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1 Introduction

This application note provides guidelines for the handling and board mounting of NXP's QFP packages. Included in this application note are recommendations for the design of Printed Circuit Boards (PCB), board mounting, and rework. Generic information of package properties, such as Moisture Sensitivity Level (MSL) rating, board level reliability, mechanical and thermal resistance data are also provided. Because semiconductor components are electrically and mechanically sensitive devices, proper precautions for handling, packing and processing QFP packages are described.
2 Scope

This application note contains generic information about various QFP packages assembled at NXP and NXP’s assembly and test vendors. Refer to Section 9 "Downloading package information from the NXP website" for step-by-step instructions for retrieving package information. For more details about NXP products, visit www.nxp.com or contact the appropriate product application team. Development efforts are required to optimize the board assembly process and application design per individual product requirements. Additionally, industry standards (such as IPC and JEDEC), and prevalent practices in the board assembly environment are good references.
3 Quad Flat Package (QFP)

3.1 Package description

The Quad Flat Package (QFP) is a surface mount integrated circuit package. The standard form is a leaded plastic package with a flat rectangular body, usually square. Leads extend from all four sides of the body. The leads are formed in a gull wing shape to allow solid footing during assembly to a PCB. Standard Pb-free lead finish is matte tin.

Thermally enhanced QFPs may be offered with an Exposed Pad (EP). These QFPs are denoted with the prefix 'H', such as HLQFP, or the suffix 'EP', such as LQFP-EP. The exposed pad is on the bottom of the QFP and acts as a ground connection and/or a heat sink for the package. The pad can be soldered to the PCB to dissipate heat.

QFP main features are:

- Package size: 5 x 5 mm$^2$ to 32 x 32 mm$^2$
- Terminal Counts: 32 to 240
- Terminal pitch: 0.4 mm to 0.8 mm
- Terminal plating: Sn, Ni-Pd-Au
- Package thickness:
  - H/LQFP: 1.4 mm
  - H/TQFP: 1.0 mm
  - QFP: > 1.6 mm
- Meets RoHS, ELV and REACH
- Halogen-free and lead-free compliant

Figure 1 shows examples of some standard QFP packages.
3.2 Package dimensioning

QFPs are offered in industry-standard sizes and thicknesses with various options of lead quantity and pitch. See Table 1. Refer to NXP package case outline drawings to obtain detailed dimensions and tolerances.

Table 1. Standard NXP QFP Offerings

<table>
<thead>
<tr>
<th>Package type</th>
<th>Thickness</th>
<th>5 x 5</th>
<th>7 x 7</th>
<th>10 x 10</th>
<th>12 x 12</th>
<th>14 x 14</th>
<th>14 x 20</th>
<th>20 x 20</th>
<th>24 x 24</th>
<th>28 x 28</th>
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<tbody>
<tr>
<td>LQFP</td>
<td>1.4</td>
<td>X</td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HLQFP</td>
<td>1.4</td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TQFP</td>
<td>1.0</td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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</tr>
<tr>
<td>HTQFP</td>
<td>1.0</td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>QFP</td>
<td>&gt;1.6</td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PQFP</td>
<td>3.6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
</tr>
</tbody>
</table>

3.3 Package cross section

The cross-section drawings in Figure 2 are included to show representative internal leadframe design differences between EP and standard QFP packages. Standard QFP packages have a mold compound that encompasses the entire bottom side of the package. The EP design exposes the die pad, which increases thermal performance.

Figure 2. Difference Between Standard and Exposed Pad QFP
4 Printed circuit board guidelines

4.1 PCB design guidelines and requirements

As the package size shrinks and the lead count increases, the dimensional tolerance and positioning accuracy affects subsequent processes. Special care must be taken when preparing for testing, especially in the test contactor cavity design and contactor pin location. Part interchangeability is also a concern when two separate suppliers provide production parts for the PCB. The optimized PCB layout for one supplier could have issues (manufacturing yield and/or solder joint life) with the other supplier's parts. When more than one source is expected, the PCB layout should be optimized for both parts.

A proper PCB footprint and stencil designs are critical to surface mount assembly yields and subsequent electrical and mechanical performance of the mounted package. The design starts with obtaining the correct package drawing. Package Case Outline (PCO) drawings are available at www.nxp.com. Follow the procedures in Section 9.2 "Retrieving package outline drawing, MCD and MSL rating". An example of a case outline drawing is shown in Figure 3. The goal is a well soldered QFP gull wing lead, as is shown in Figure 4.

![Figure 3. Example of 14 x 14 mm LQFP case outline drawing](image-url)
4.2 PCB pad design

4.2.1 General pad guidelines

NXP follows the Generic Requirements for Surface Mount Design and Land Pattern Standards from the Institute for Printed Circuits (IPC), IPC-7351B. This document and an accompanying land pattern calculator can be purchased from the IPC’s website http://www.ipc.org. Inside the document are guidelines for most QFPs, based on assumed package dimensions. Some general guidelines for QFP footprints are:

- Lead foot should be approximately centered on the pad with equal pad extension from the toe and the foot.
- Typically, the pad is extended 0.5 mm beyond the QFP foot at both the heel and the toe.
- Care should be taken that PCB pads do not extend under the QFP body, which can cause issues in assembly.
- Pad width should be approximately 60 % of the lead pitch. See Table 2.
- Pitch needs to be designed in metric units using the exact dimensions of 0.40, 0.50, 0.65, and 0.80 mm.

Note: Some legacy products may have alternate pitches.

<table>
<thead>
<tr>
<th>Lead Pitch (mm)</th>
<th>Pad Width (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.40</td>
<td>0.26</td>
</tr>
<tr>
<td>0.50</td>
<td>0.30</td>
</tr>
<tr>
<td>0.65</td>
<td>0.38</td>
</tr>
<tr>
<td>0.80</td>
<td>0.50</td>
</tr>
</tbody>
</table>

Using the example of the 14 x 14 mm QFP in Figure 3, the PCB pad width should be designed at 0.38 mm for this 0.65 mm lead pitch package. To determine the placement and length of the pads, obtain the tip-to-tip dimension from the package drawing,
Figure 3. This dimension has a range of 16.95 to 17.45 mm or a nominal dimension of 17.20 mm. Similarly, the foot length has a range of 0.65 to 0.95 mm with a nominal of 0.80 mm. Therefore, the pad should be 1.80 mm in length, which is the 0.80 mm nominal foot length with a 0.50 mm extension on the heel and toe sides. See Figure 5.

Exposed pad QFP packages are thermally/electrically enhanced leadframe technology based, and the bottom of the package provides the primary heat removal path as well as excellent electrical grounding to the PCB. In an EP package the die attach pad is down-set within the package such that the pad is exposed during the mold process, as shown in Figure 6. White arrows here stand for heat flow. To optimize thermal performance, the PCB design should include a thermal plane, as shown in Figure 6.

Although the land pattern design for EP lead attachment on the PCB should be the same as that for conventional, non-thermally/electrically enhanced packages, extra features are required during the PCB design and assembly stage for effectively mounting thermally/electrically enhanced packages. In addition, repair and rework of assembled packages may involve some extra steps, depending upon the current rework practice within the company.

4.2.2 Thermal/electrical land pad guidelines

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4.2.3 Spacing between PCB pads for leads and exposed pad

To maximize both removal of heat from the package and electrical performance, a land pattern must be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 7. The size of the land pattern can be larger, smaller, or even take on a different shape than the exposed pad on the package. However, the solderable area, as defined by the solder mask, should be at least the same size/shape as the exposed pad area on the package to maximize the thermal/electrical performance. A clearance of at least 0.25 mm should be designed on the PCB between the outer edges of the land pattern and the inner edges of leads pad pattern to avoid any shorts. This topic is discussed in more detail in Section 5.2 "Solder stencil and solder paste".

Alternatively, the land pattern for the exposed pad can be segmented into a symmetric array of square or rectangular lands, as shown in Figure 8. This also applies to packages with multiple exposed pads. The land array can be created either by segmentation of a full copper area by solder mask openings or by NSDM defined copper lands. The recommended edge length/width of a matrix land is between 1.0 to 2.0 mm. Distance
between the lands should be 0.40 mm. The segmented PCB design facilitates the solder paste flux outgassing during reflow, thereby promoting a lower voiding level of the completed solder joint. The maximum size of a single solder void is limited by the dimensions of a single matrix segment at the same time.

Figure 8. Segmented exposed pad land pattern design

4.2.4 Vias in the PCB EP pad

While the land pattern on the PCB provides a means of heat transfer/electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). These vias act as heat pipes. The number of vias is application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number of vias. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern on a 1.2 mm grid, as shown in Figure 9.

It is also recommended that the via diameter be 0.30 to 0.33 mm with 1.0 oz. copper via barrel plating. This specification is recommended to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the exposed pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be "tented" with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 0.1 mm (4.0 mils) larger than the via diameter.

Note: These recommendations are to be used as a guideline only.
4.2.5 Via pad finishes

Almost all PCB finishes are compatible with QFPs including Hot Air Solder Leveled (HASL), Organic Solderability Protectant (OSP), Electroless Nickel Immersion Gold (ENIG), Immersion Sn and Immersion Ag.

4.2.6 Solder mask layer

In general, the solder mask should be pulled away from both the input and output pads. The solder mask opening around the PCB pads can be as large as the spacing between pads. The area between the pads may be too thin for the solder mask resulting in the solder mask lifting off from the PCB. See Figure 10. A potential solution is modification of the solder mask along the pad-to-pad spacing so only the toes of the pads are covered with solder mask for better PCB strength.
5 Board assembly

5.1 Assembly process flow

A typical Surface Mount Technology (SMT) process flow is depicted in the SMT process flow in Figure 11.

![SMT process flow diagram](image)

Figure 11. SMT process flow

5.2 Solder stencil and solder paste

For maximum thermal/electrical performance, it is required that the exposed pad on the package be soldered to the land pattern on the PCB. This can be achieved by applying solder paste on both the pattern for lead attachment as well as on the land pattern for the exposed pad. While for standard (non-thermally/electrically enhanced) leadframe based packages the stencil thickness depends on the lead pitch and package co-planarity, the package standoff must also be considered for the thermally/electrically enhanced packages to determine the stencil thickness. For a nominal standoff of 0.1 mm, the stencil thickness of 0.10 to 0.15 mm, depending upon the pitch, is recommended. The EP stencil aperture openings should be 0.25 mm smaller than the copper pads on the PCB, as shown in Figure 12. This will allow for proper registration of the stencil to the pad pattern. A large stencil opening could result in a poor release. To overcome this, the aperture opening should be subdivided into an array of smaller openings, similar to the thermal land pattern shown in Figure 13. These guidelines will result in the solder joint area to be about 80 to 90 % of the exposed pad area.

![Reduced solder stencil aperture for exposed pad](image)

Figure 12. Reduced solder stencil aperture for exposed pad
An array pattern is recommended in the stencil opening for the large thermal pad region. A large opening or aperture in the thermal region allows "scooping" to occur during screen printing. Other reasons for segmenting the thermal regions include minimizing solder standoff mismatch with terminal pads, minimizing solder voids in the thermal region, and minimizing chances of bridging with terminal pads.

Several different array patterns are recommended in this section. Smaller QFP package sizes do not require any thermal pad pattern on the PCB and stencil, unless to minimize solder voids. On larger packages, stencil thermal openings should be segmented in smaller regions. Examples are shown in Figure 14. The spacing between segments either on the stencil or on the PCB should be 0.15 mm or more. Narrower spacing between segments can become a manufacturing issue.

The stencil opening should be approximately 50 to 80 % of the total PCB thermal pad area. This stencil-PCB thermal pad ratio ensures proper coverage of the thermal pad area with fewer voids and minimizes the possibility of overflow bridging to the adjacent lead.

Solder paste is one of the most important materials in the SMT assembly process. It is a homogenous mixture of metal alloy, flux, and viscosity modifiers. The metal alloy particles are made in specific size and shape. Flux has a direct effect on soldering and cleaning, and it is used to precondition the surfaces for soldering by removing minor surface contamination and oxidation. There are two different flux systems commonly available. The first type requires cleaning such as standard rosin chemistries and water soluble chemistries. Standard rosin chemistries are normally cleaned with solvents, semi-aqueous solutions or aqueous/saponifier solutions while the water soluble chemistries are cleaned with pure water. The second flux system type requires no cleaning, but
normally a little residue will remain on the PCB after soldering. It is recommended to use low-residue and no-clean solder paste for soldering. However, the end user should evaluate their entire process and usage to ensure desired results.

The spread of solder paste during reflow partially depends upon the solder paste alloy. SnPb solder alloys spread significantly better than the many lead-free pastes (i.e., SnAgCu, SnAgBiCu, etc.), given the same reflow temperature.

5.3 Component placement

The high lead interconnection and insertion density suggests that precise and accurate placement machines are preferred. To meet this tight requirement, the placement machine should be equipped with optical recognition systems, i.e., vision system, for the centering of the PCB as well as the components during the pick and place motion. A placement accuracy study is recommended to calculate compensations required. NXP follows EIA-783 standard for tape-and-reel orientation as is shown in Figure 15.

![Figure 15. QFP orientation in tape-and-reel](image)

5.4 Soldering

A typical profile band is shown in Figure 16. The actual profile parameters depend upon the solder paste used and recommendations from paste manufacturers should be followed. Temperature profile is the most important control in reflow soldering and it must be fine tuned to establish a robust process. In most cases, thermocouples should be placed under the heaviest thermal mass device on the PCB to monitor the reflow profile. Generally, when the heaviest thermal mass device reaches reflow temperatures, all other components on the PCB will reach reflow temperatures as well.

Nitrogen reflow is recommended to improve solderability and to reduce defects such as solder balls.
Figure 16. General solder reflow phases

It is also recommended to monitor the temperature profile of package top surfaces to validate the package peak temperature does not exceed MSL classification of individual devices.

For all devices on the PCB, the solder paste needs to be taken into account for the reflow profile. Every paste has a flux, and the flux dominates the reflow profile for steps like soak time, soak temperature, and ramp rates. Peak reflow temperature is the melting temperature of the metals in the paste, plus a "safety" margin to ensure that all solder paste on the PCB reflows. The reflow profile for exposed pad packages need not be any different than the one used for non-thermally/electrically enhanced packages.

The reflow profile should follow the paste supplier's "recommended" profile. Deviation from the recommended profile should be evaluated first using a copper (Cu) coupon test. The horizontal size for a typical solder paste volume is measured as either a diameter or as "x" and "y" lengths. The Cu coupon is then reflowed and the solder paste volume is measured for either diameter or "x" and "y". The goal is have a reflow profile with the most horizontal spread. For best results, the Cu coupon should be lightly sanded before use to remove Cu-oxide build up.

5.5 Inspection

Whenever possible, non-destructive vision/optical inspection and X-ray inspection are recommended to verify any open or short-circuit after reflow soldering.
5.6 Common QFP defects

Figure 17. Three common QFP defects
6 Repair and rework procedure

The following items must be observed when performing repair and rework:

- The influence of the heat on adjacent packages must be minimized. Care should be taken to not exceed the temperature rating of the adjacent package.
- Heating conditions will differ due to differences in the heat capacities of the PCB (board thickness, number of layers) and mounted components used; thus, the conditions must be set to correspond to the actual product and its mounted components.
- NXP follows industry standard component level qualification requirements, which include three solder reflow passes. The three reflow passes simulate a board level attached to a double-sided board and includes one rework pass. The removed QFP package should be properly disposed of, to prevent mixing removed components with new components.

6.1 Repairing

Repair of single solder joints is generally possible but requires proper tools. A soldering iron can be used to repair soldering defects for packages that have leads that extend beyond the package periphery, including the QFP package. Difficulty with fine pitch applications could occur with the use of soldering irons. The soldering iron temperature and usage must be set so that the package surface temperature does not exceed its maximum allowable temperature.

6.2 Reworking

If a defective component is observed after board assembly, the device can be removed and replaced by a new one. This rework can be performed using the heating methods described below.

A typical QFP rework flow process is:

1. Tooling preparation
2. Package removal
3. Site redressing
4. Solder paste printing
5. Remount package
6. Reflow soldering
7. Visual check

**Note:** The NXP product quality guarantee/warranty does not apply to products that have been removed, thus, component reuse should be avoided if at all possible.

In any rework, the PCB is heated. The thermal limits of PCB and components (e.g. MSL information) have to be followed. During heating, the combination of rapid moisture expansion, materials mismatch, and material interface degradation can result in package cracking and/or delamination of critical interfaces within the components and PCB. To prevent moisture induced failures, it is recommended that the PCBs and components have had strict storage control with a controlled environment such as dry air or nitrogen. In addition, a prebake is recommended to remove the moisture from the components and the PCB prior to removal of the QFP. An example of a prebake is to place boards with SMT components in an environment of 125 °C for 24 hours or boards with temperature sensitive components in 95 °C for 24 hours. This is typically done if an assembled board
has exceeded the maximum storage time out of the dry pack. See the label on packing material for this time specification.

Individual process steps for reworking a QFP package are as follows:

### 6.2.1 Tooling preparation

Various rework systems are available on the market. In general, the rework station should have a split light system, an XY table for alignment, and a hot air system with a top and bottom heater for component removal. For processing QFP packages, a system should meet the following requirements:

- **Heating:** Controlled hot air transfer (temperature and air flow) to both the QFP package and its mounted PCB is strongly recommended. Figure 18 illustrates various heating nozzles. The heating should be appropriate for the correct package size and thermal mass. PCB preheating from under the board is recommended. Infrared heating can be applied, especially for preheating the PCB from the underside, but it should only augment the hot air flow from the upper side (component side). Nitrogen can be used instead of air. Additional information can be found in Section 6.2.2.

- **Vision system:** The bottom side of the package as well as the site on the PCB should be observable. For precise alignment of the package to PCB, a split light system should be implemented. Microscope magnification and resolution should be appropriate for the pitch of the device.

- **Moving and additional tools:** Placement equipment should have good accuracy. In addition, special vacuum tools might be required to remove solder residue from PCB pads.

![Figure 18. Examples of typical QFP heating nozzles](image)

### 6.2.2 Package removal

If a component is suspected to be defective and should be returned, no further defects must be introduced to the device during the removal of the component from the PCB. Any additional defects could interfere with subsequent failure analysis. The following recommendations are intended to reduce the chances of damaging a component during removal:

- **Moisture removal:** Dry bake components before removal at 125 °C for 16 – 24 hours for boards with SMT components or 95 °C for 16 to 24 hours for boards with temperature sensitive components.

- **Temperature profile:** During desoldering, ensure the package peak temperature is not higher, and temperature ramps are not steeper, than the standard assembly reflow process.
• **Mechanics:** Do not apply high mechanical forces during removal. High force can damage the component and/or the PCB, which could limit failure analysis of the package. For large packages, pipettes can be used, implemented on most rework systems. For small packages, tweezers may be more practical.

If suspected components are fragile, it is especially necessary to determine if they can be electrically tested directly after desoldering, or if these components have to be preconditioned prior to testing. In this case, or if safe removal of the suspected component is not possible or too risky, the whole PCB or the part of the PCB containing the defective component should be returned.

To remove the faulty component from the board, hot air should be applied from the top and bottom heaters. An air nozzle of correct size should be used to conduct the heat to the QFP component leads such that a vacuum pick up tool can properly remove the component. The temperature setting for the top heater and the bottom heater is dependent on the component rating. Many assembly sites have extensive in-house knowledge on rework, and their experts should be consulted for further guidance.

If the PCB is large, it is important to avoid bending of the printed circuit material due to thermal stress, so a bending prevention tool must be placed on the bottom of the printed circuit board, and a bottom heater installed to allow heating of the entire printed circuit board to raise work efficiency.

### 6.2.3 Site redressing

After the component is removed, the PCB pads have to be cleaned to remove solder residue to prepare for the new component placement. This may be done by vacuum desoldering, solder sucker, solder wick braid, etc. after applying flux. Remaining solder residue and projections cause the solder stencil to not closely adhere to the substrate during solder paste printing, leading to improper solder paste supply during component mount.

Moreover, when the solder residue flows all the way to an adjacent through-hole, the solder paste printed on the pad can be transferred, via suction, to the through-hole during reflow, which may cause improper connection. A solvent may be necessary to clean the PCB of flux residue. A desoldering station can be used for solder dressing. It should be noted that the applied temperature should not exceed 245 °C. Applied temperatures above 245 °C can contribute to the PCB pad peeling from the PCB. This is typically a manual operation with quality being directly attributed to experience and skill.

Non-abrasive or soft bristle brushes should be used. This is because abrasive brushes, such as steel brushes, can contribute to bad solder joints. Prior to placing a new component on the site, solder paste should be applied to each PCB pad by printing or dispensing. A no-clean solder paste is recommended.

### 6.2.4 Solder paste printing

Solder supply during rework is done using specialized templates and tools. A mini stencil with the same stencil thickness, aperture opening, and pattern as the normal stencil is placed in the component site. A mini metal squeegee blade deposits solder paste in the specific area. See Figure 19. The printed pad should be inspected to ensure even and sufficient solder paste before component placement.

In situations where neighboring parts are at close proximity with the QFP components, and the mini-stencil method is not an option, apply solder paste carefully on each pad...
using a paste dispensing system. The volume of solder paste must be controlled to prevent shorting on the component and/or neighboring components.

6.2.5 Package remount

After preparing the site, the new package can be placed onto the PCB. When remounting the package, it is recommended to use rework equipment that has good optical or video vision capability. A split light system displays images of both package leads and PCB pads by superimposing two images. Alignment of the leads and pads is completed with an adjusting XY, which enables correct soldering. See Figure 20.

Regular lead array QFP exhibits self-alignment in any direction including X-axis shift, Y-axis shift, and rotational misplacement. The exposed pad might not exhibit a strong self-alignment capability, which is required for precise placement of the component on the PCB.

6.2.6 Reflow soldering

The new component is soldered to the PCB using the same temperature profile as the normal reflow soldering process, shown in Section 5.4 "Soldering". During soldering, the package peak temperature and temperature ramps cannot exceed those of the standard assembly reflow process.

In IR or convection processes, the temperature can vary greatly across the PC board depending on the furnace type, size and mass of components, and the location of components on the assembly. Profiles must be carefully tested to determine the hottest and coolest points on the assembly. The hottest and coolest points should fall within the recommended temperature range in the reflow profile. To monitor the process,
thermocouples must be carefully attached to the solder joint interface between the package and board with very small amounts of thermally conductive grease or epoxy. The materials used in rework have a higher potential to create conductive traces and corrosion, compared to standard materials. Clean the PCB if it has not been cleaned in the "normal" process, or the rework was not done using "no clean" materials.
7 Board level reliability

7.1 Testing details

Solder Joint Reliability (SJR) testing is performed to determine a measure of board level reliability when exposed to thermal cycling. Information provided here is based on experiments executed on QFP devices using a daisy chain bond configuration. Actual surface mount process and design optimizations are recommended to develop an application specific solution. For automotive grade product applications, NXP typically prefers to reach a minimum of 2000 cycles before first solder joint failure in SJR experiments. The widely accepted temperature range for testing is -40 to +125 °C. Consumer SJR temperature cycling conditions may vary widely, depending on the application and specific user. Typically, NXP consumer SJR testing is performed from 0 to +100 °C.

Table 3 shows the NXP standard test set-up for performing board level solder joint reliability testing.

<table>
<thead>
<tr>
<th>Table 3. Board level reliability testing: material and test setup</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Printed circuit board</strong></td>
</tr>
<tr>
<td>• 1.58 mm thickness</td>
</tr>
<tr>
<td>• Four Cu layer</td>
</tr>
<tr>
<td>• OSP surface finish</td>
</tr>
<tr>
<td><strong>Test board assembly</strong></td>
</tr>
<tr>
<td>• Pb-free solder paste SAC387</td>
</tr>
<tr>
<td>• Reflow peak temperature for SAC assembly ~ 240 °C</td>
</tr>
<tr>
<td>• Pb solder paste Sn63Pb37</td>
</tr>
<tr>
<td>• Reflow peak temperature for SnPb assembly ~ 220 °C</td>
</tr>
<tr>
<td>• 0.100 to 0.150 mm thickness (depending on the device pitch), Ni plated, laser cut and electropolished stainless steel stencil</td>
</tr>
<tr>
<td><strong>Cycling conditions</strong></td>
</tr>
<tr>
<td>• Continuous in situ daisy chain monitoring per IPC-9701A</td>
</tr>
<tr>
<td>• Air-Temperature Cycling (ATC) for Automotive</td>
</tr>
<tr>
<td>– –40 °C / +125 °C</td>
</tr>
<tr>
<td>– 15 minute ramp / 15 minute dwell</td>
</tr>
<tr>
<td>– 1.0 hour cycle time</td>
</tr>
<tr>
<td>• Air-Temperature Cycling (ATC) for commercial &amp; industrial</td>
</tr>
<tr>
<td>– –0 °C / +100 °C</td>
</tr>
<tr>
<td>– 10 minute ramp / 20 minute dwell</td>
</tr>
<tr>
<td>– 1.0 hour cycle time</td>
</tr>
<tr>
<td><strong>Package test vehicle</strong></td>
</tr>
<tr>
<td>• Production BOM package including die (die mechanically present, without wire bond connection)</td>
</tr>
<tr>
<td>• Daisy chain bond pattern on lead frame to allow continuous monitoring</td>
</tr>
</tbody>
</table>

7.2 Solder joint reliability results

NXP experimentally gathers board-level reliability data for a variety of packages. Results from these experiments, including Weibull plots, may be requested by customers by contacting the NXP sales team.
8 Thermal characteristics

8.1 General thermal performance

Because the thermal performance of the package in the final application will depend on a number of factors (i.e. board design, power dissipation of other components on the same board, ambient temperature), the thermal package properties provided by NXP should only serve as a guideline for the thermal application design. In applications where the thermal performance is considered to be critical, NXP recommends to run application specific thermal calculations in the design phase to confirm the on-board thermal performance.

Exposed pad packages may require the exposed pad to be connected to the PCB for thermal and/or electrical measurement. For optimized thermal performance, it is recommended to form a thermal pass into the PCB by connecting the exposed pad to the top and/or bottom and/or inner copper layers of the PCB. The PCB copper area and number of thermal vias connected to the exposed pad required to achieve the proper thermal performance on the PCB is application specific and will depend on the package power dissipation and the individual board properties (thermal characteristics of the application PCB).

8.2 Package thermal characteristics

Junction temperature is a function of die size, on-chip power dissipation, package thermal characteristics, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

Additional factors that need be considered in PCB design and thermal rating of the final application amongst others are:

- Thermal resistance of the PCB
  - Thermal conductivity of PCB traces
  - Number of thermal vias
  - Thermal conductivity of thermal vias
- Quality and size of PCB solder joints
  - Effective PCB pad size
  - Potential solder voiding in the thermal path solder joints that may reduce the effective solder area

The thermal characteristics of the package provide the thermal performance of the package when there are no nearby components dissipating significant amounts of heat. The stated values are meant to define the package thermal performance in a standardized environment.

Thermal properties of the individual products are usually given in the NXP product data sheets, as appropriate. Product data sheets are available under www.NXP.com. Customers may request additional thermal properties.

8.3 Package thermal properties – definition

The thermal performance of QFP packages with and without an exposed pad is typically specified by definition of thermal properties, such as $R_{JA}$, $R_{JC}$ and $\Psi_{JT}$ (in °C/W). Thermal characterization is performed by physical measurement and running complex simulation models under the following conditions:
• **Thermal board types:** Four layer board (2s2p) per JEDEC JESD51-7 and JESD51-5 (exposed pad packages only)
• **Boundary conditions:** Natural convection (still air) per JEDEC JESD51-2 and cold plate method per MIL SPEC-883 method 1012.1

### 8.3.1 \( R_{\theta JA} \): Theta junction-to-ambient natural convection (still air)

Junction-to-ambient thermal resistance (Theta-JA or \( R_{\theta JA} \) per JEDEC JESD51-2) is a one-dimensional value that measures the conduction of heat from the junction (hottest temperature on die) to the environment (ambient) near the package in still air environment. The heat that is generated on the die surface reaches the immediate environment along two paths:

• Convection and radiation off the exposed surface of the package
• Conduction into and through the test board followed by convection and radiation off the exposed board surfaces

### 8.3.2 \( R_{\theta JC} \): Theta junction-to-case

Junction-to-Case thermal resistance (Theta-JC or \( R_{\theta JC} \) per MIL SPEC-883 Method 1012.1) indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method per MIL SPEC-883 Method 1012.1, with the cold plate temperature used for the case temperature. The case is defined as either the temperature at the top of the package (for non-exposed pad packages), or the temperature at the bottom of the exposed pad surface (for exposed pad packages). For exposed pad packages where the pad is expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance. \( R_{\theta JC} \) can be used to estimate the thermal performance of a package when the board is adhered to a metal housing or heat sink, or when a complete thermal analysis is done.

### 8.3.3 \( \Psi_{JT} \) (Psi JT): Junction-to-package top

Junction-to-package top (Psi JT or \( \Psi_{JT} \)) indicates the temperature difference between the package top and the junction temperature, optionally measured in still air condition (per JEDEC JESD51-2) or forced convection environment (per JEDEC JESD51-6). \( \Psi_{JT} \) must not be mixed up with the parameter \( R_{\theta JC} \):

• \( R_{\theta JC} \) is the thermal resistance from the device junction to the external surface of the package, with the package surface held at a constant temperature
• \( \Psi_{JT} \) is the value of the temperature difference between package surface and junction temperature, usually in natural convection

### 8.3.4 Package thermal properties – example

An example of the thermal characteristics as typically shown in the NXP product data sheet is shown in Table 4. The example applies to a package size 20 mm x 20 mm x 1.4 mm, pitch 0.5 mm, die size ~ 6.0 mm x 6.3 mm.

<table>
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<tr>
<th>Table 4. Thermal resistance example</th>
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<tbody>
<tr>
<td>Rating</td>
</tr>
<tr>
<td>Junction to Ambient (Natural Convection)</td>
</tr>
<tr>
<td>Board Type</td>
</tr>
<tr>
<td>Four Layer Board (2s2p)</td>
</tr>
<tr>
<td>Type</td>
</tr>
<tr>
<td>( R_{\theta JA} )</td>
</tr>
</tbody>
</table>

[1] [2]
<table>
<thead>
<tr>
<th>Rating</th>
<th>Board Type</th>
<th>Type</th>
<th>Value</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction to Case</td>
<td>—</td>
<td>$R_{\theta JC}$</td>
<td>8</td>
<td>°C/W</td>
<td>[3]</td>
</tr>
<tr>
<td>Junction to Package Top</td>
<td>—</td>
<td>$\Psi_{JT}$</td>
<td>2</td>
<td>°C/W</td>
<td>[4]</td>
</tr>
</tbody>
</table>

[1] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board temperature) ambient temperature air flow power dissipation of other components on the board, and the thermal resistance.

[2] Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.

[3] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL Spec-883 Method 1012.1).

[4] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
9 Downloading package information from the NXP website

9.1 Performing a product search on NXP website

The package outline drawing and the material composition declaration sheet (MCD, in IPC-1752 reporting format) can be downloaded from the NXP website. Information on product specific moisture sensitivity levels (MSL) is available on the website, too. Note that the website screen appearance is regularly changed and may look different from the one shown in this section. However, the general procedure described should mostly apply.

To download the documents:

2. In the text box on the upper right of the screen, click and select "Products" from the drop-down menu.

3. Enter the NXP product part number in the "Search …"box.
   The next screen returns search results, and lists all part numbers and documents related to the search term.
4. On the search results screen, select the desired part number. The next screen shows the "Product Overview Page" with information on Product Documentation, Software & Tools, Buy/Parametrics, Package/Quality, Training & Support.

9.2 Retrieving package outline drawing, MCD and MSL rating

1. Click on the "Package/Quality" tab to view environmental and quality information
2. Click on the "Material Declaration" link to go to the "Chemical Content" site. Material information is displayed. MCD sheet can be downloaded in XLS, XLM, and PDF format.

3. Click the "Package" link to go to the "Package Overview" site. Package information is displayed. PDF file with package outline drawing can be downloaded.
9.3 Retrieving the packing information for the product

1. Click on the "Buy/Parametrics" tab on the "Product Overview Page" to view available product options

2. Select the preferred part number from the list and click on the link to view details of the part number.
3. Click on the "Parts Detail" link to show the product details view.

4. Find the link to the Packing Information next to the product number and download the PDF file.
10 Package handling

10.1 Handling electrostatic discharge sensitive devices

Semiconductor Integrated Circuits (ICs) and components are Electrostatic Discharge Sensitive devices (ESDS). Proper precautions are required for handling and processing these devices. Electrostatic Discharge (ESD) is one of the significant factors leading to damage and failure of semiconductor ICs and components. Comprehensive ESD controls to protect ESDS during handling and processing should be considered.

The following industry standards describe detailed requirements of proper ESD controls. NXP recommends that users understand and adhere to the standards when handling and processing ESDS.

- JESD615-A – Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- IEC-101/61340-5 – Specification for the Protection of Electronic Devices from Electrostatic Phenomena

10.2 Handling moisture-sensitive surface-mount devices

QFPs are moisture/reflow sensitive Surface Mount Devices (SMD). Proper precautions are required for Handling, Packing, Shipping and Using these devices.

Moisture from atmospheric humidity enters permeable packaging materials by diffusion. When the package is exposed to rapid temperature rise and high temperature during the reflow solder process, the following can occur:

- Moisture expansion
- Material mismatch
- Material interface degradation

These conditions can cause package cracking and/or delamination of critical interfaces, known as the popcorn effect.

Therefore, moisture-sensitive components are dried and sealed in a Moisture-Barrier Bag (MBB) before shipping, per IPC/JEDEC J-STD-033. The components are stored together with a desiccant and a moisture indicator card in the vacuum sealed bag. Remove the moisture-sensitive components only immediately prior to assembly onto the PCB. If partial lots are used, the remaining SMD packages must be resealed or placed in safe storage within one hour of opening the bag.

A label on the MBB indicates that it contains moisture-sensitive components. See Figure 21. The "Moisture Sensitivity Caution Label" contains information about the Moisture Sensitivity Level (MSL) and maximum allowed peak body temperature of the products. The same information is shown on the barcode labels of the shipping box and reels.
The MSL indicates the floor life of the component, its storage conditions, and handling precautions after the original container has been opened. The permissible time, from opening the moisture-barrier bag until the final solder reflow process, that a component can remain outside the moisture-barrier bag is a measure of the sensitivity of the component to ambient humidity.

Table 5 presents the floor life definitions per IPC/JEDEC J-STD-033. Components must be mounted and reflowed within the allowable period of time (floor life out of the bag), and component temperature must not exceed the maximum peak body temperature during the reflow process.
Table 5. Moisture classification level of floor life (IPC/JEDEC J-STD-033)

<table>
<thead>
<tr>
<th>Moisture sensitivity level</th>
<th>Floor life (out of bag) at factory ambient ≤ 30 °C/60 % RH or as stated</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Unlimited at ≤ 30 °C/85 % RH</td>
</tr>
<tr>
<td>2</td>
<td>1 Year</td>
</tr>
<tr>
<td>2a</td>
<td>4 Weeks</td>
</tr>
<tr>
<td>3</td>
<td>168 Hours</td>
</tr>
<tr>
<td>4</td>
<td>72 Hours</td>
</tr>
<tr>
<td>5</td>
<td>48 Hours</td>
</tr>
<tr>
<td>5a</td>
<td>24 Hours</td>
</tr>
<tr>
<td>6</td>
<td>Mandatory bake before use. After bake, must be reflowed within the limit specified on the label.</td>
</tr>
</tbody>
</table>

Upon opening the MBB, the floor-life clock starts. If components have been exposed to ambient air for longer than the specified time, or if the humidity indicator card indicates too much moisture after opening a moisture-barrier bag, then the components are required to be rebaked prior to the assembly process. Refer to IPC/JEDEC J-STD-033 for the baking procedure.

10.3 Packing of devices

QFP devices are contained in trays or tape-and-reel configurations. The packing media are designed to protect devices from electrical, mechanical and chemical damage, as well as moisture absorption.

Devices are shipped with dry packing or non-dry packing, depending on the MSL level of the device per IPC/JEDEC J-STD-033. See Table 6.

MSL1 components do not require dry packing.

Devices with sulfur-sensitive Au/Ag alloy plating are packed with a sulfur barrier pack to protect the device from airborne sulfur contamination.

Table 6. Dry packing requirements (IPC/JEDEC J-STD-033)

<table>
<thead>
<tr>
<th>MSL level</th>
<th>Dry before bag</th>
<th>MBB with HIC</th>
<th>Desiccant</th>
<th>MSID label</th>
<th>Caution label</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Optional</td>
<td>Optional</td>
<td>Optional</td>
<td>Not Required</td>
<td>Not required if classified at 220 to 225 °C Required if classified at 220 to 225 °C</td>
</tr>
<tr>
<td>2</td>
<td>Optional</td>
<td>Required</td>
<td>Required</td>
<td>Required</td>
<td>Required</td>
</tr>
<tr>
<td>2a to 5a</td>
<td>Required</td>
<td>Required</td>
<td>Required</td>
<td>Required</td>
<td>Required</td>
</tr>
<tr>
<td>6</td>
<td>Optional</td>
<td>Optional</td>
<td>Required</td>
<td>Required</td>
<td>Required</td>
</tr>
</tbody>
</table>

Moisture-sensitive devices are dry packed for transportation and storage. Refer to Section 10.2 "Handling moisture-sensitive surface-mount devices".

- Dry packing
  - Trays and tape-and-reels, loaded with devices, are sealed in a Moisture-Barrier Bag (MBB) that is labeled and packed in dedicated boxes with dunnage for the final shipment
  - Each dry pack bag includes the following:
    - A Moisture-Sensitive Identification (MSID) label
    - A desiccant pouch
    - A Humidity Indicator Card (HIC)
– NXP encourages recycling and reuse of materials whenever possible.
– NXP will not use packing media items processed with or containing class 1 ozone-depleting substances
– Whenever possible, NXP shall design its packing configurations to optimize volumetric efficiency and package density to minimize the amount of packing that enters the industrial waste stream
– NXP shall comply with following Environmental Standards Conformance guidelines/directives:
  – ISPM 15: Guidelines for regulating wood packaging material in international trade

The packing method, product orientation, dimensions, and labels are described in the Packing Information document. This document can be downloaded from NXP’s website at the Buy Options for each device. The different packing methods are also indicated by the ending of either the orderable part number (3-digit number or single letter), or the ending of the ordering code (3-digit number).

Note: Packing information can be found on NXP’s website following the steps described in Section 9.3 "Retrieving the packing information for the product".

Proper handling and storage of dry packs are recommended. Improper handling and storage, such as dropping dry packs, storage exceeding 40 °C/90 % RH environment, or excessive stacking of dry packs, will increase various quality and reliability risks.

10.3.1 Trays

• NXP complies with standard JEDEC tray design configuration – See Figure 23 “Example of QFP packing tray”
• Devices are oriented with pin 1 toward the chamfered corner of the tray
• Trays are designed to be baked for moisture-sensitive SMDs, but temperature rating of tray should NOT be exceeded when devices are baked. Temperature rating can be found at end-tab of tray. Recommended baking temperature of trays is 125 °C.
• Trays are typically banded together with 5 + 1 (five fully loaded trays and one cover tray) stacking, and dry packed in a moisture-barrier bag. Partial stacking (1 + 1, 2 + 1, etc.) is also available, depending on individual requirements

Figure 23. Example of QFP packing tray
10.3.2 Tape-and-reel

- NXP complies with EIA-481B and EIA-481C for carrier tape-and-reel configuration – See Figure 24
- NXP complies pin one orientation of devices with EIA-481
- Tape-and-reels are NOT designed to be baked at high temperature
- Each tape-and-reel is typically dry-packed in a moisture-barrier bag

Figure 24. Carrier tape specifications
11 References

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<th>Ref.</th>
<th>Name</th>
<th>Title</th>
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<td>Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices</td>
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Revision history

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<th>Date</th>
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<td>v.3.0</td>
<td>8/2019</td>
<td>• Updated Section 1, Section 2, and Section 3</td>
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<td></td>
<td></td>
<td>• Section 4.2.3 added new guidelines for segmented exposed pad land pattern design</td>
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<td>• Section 8, updated thermal characteristics content</td>
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<td></td>
<td></td>
<td>• Section 9, renamed and revamped content for downloading package information from NXP website</td>
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<td>• Section 10, updated content</td>
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<td>• Changed all reference of Freescale to NXP</td>
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<td>v.2.0</td>
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<td>v.1.0</td>
<td>10/2011</td>
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<td>Fig. 24</td>
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