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Application Note

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MPC56xxB Reset Timing

by: Steven McLaughlin, Armin Winter

1 Introduction

This document outlines reset timing of the MPC56xxB microcontroller family. The reset of the MPC56xxB family has six stages managed by a state machine which starts from power-up to idle where the device is ready to commence the application program.

The topic of reset includes serial/flash boot, several reset phases and low power exit sequences. Depending on the source of the reset, this will have an impact on the reset timing as the various resets will place the device at a different reset phase. Full descriptions of the reset sources are available in the device microcontroller reference manual available from www.freescale.com. This document is written to specifically explain the respective timing of each reset phase.

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2 Use Case Examples: Monitoring the Reset Timing

The following examples illustrate why it could be important to monitor the reset pin within an application.

2.1 External watchdog

External IC's can offer external watchdog functionality, e.g. the Freescale range of Power SBCs. In this instance it is essential to understand the minimum duration of the low signal on the MCU's RESET pin to safely detect an external RESET. The external watchdog should ideally be tracking functional activity on an external pin; to check if software is running, or if software is stuck for a timeout period, it would assert the reset pin.

2.2 Low Power Wake-Up

For an automotive application of RF key fob, a specific reaction time is required. The reset timing of the system is required to be factored into calculations of how long it takes to lock/unlock an automobile. Low power wake-up includes wake-up timing with the reset sequence (e.g. standby exit on this family of microcontrollers includes this reset sequence).

2.3 Multi Microcontroller and Peripheral IC systems

There may be the case in which the microcontroller's reset pin is connected to another part of a system. In order to manage inter-processor communication and software synchronization; it is important that the minimum/maximum reset signals are monitored on all microcontrollers and other dependent integrated circuits chips on the application board.

3 RESET Sequence to Execution State

Figure 1 illustrates the microcontroller start-up sequence and highlights some internal operations which are relied upon to initialize the device to a useful condition. Figure 1 follows from a condition of applying power to the device, which activates/stabilize the voltage regulator, core and 16MHz internal RC oscillator (not shown). With this in place, various factory programmed settings are applied and the flash is initialized which allows for user programmed code to be activated and moving the device from RESET mode to its default run mode (DRUN). Details of the each phase are described in Table 1.

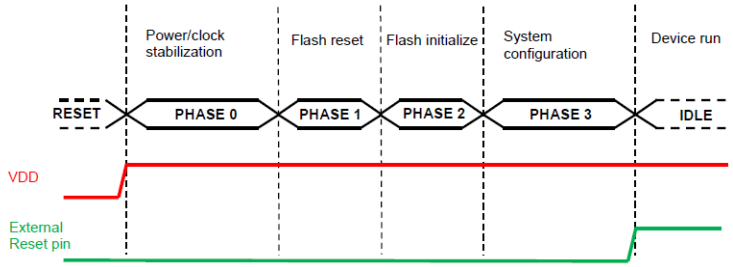


Figure 1 Typical MPC560xB Power On Reset Timing Example

4 RESET Phases and Timing

	Min (µs)	Max (µs)	Comments
POROUT Threshold Internal Regulator start-up	Approx 1000 200	Approx 1000 + ramp time of the external 3.3V supply 300	• POROUT - This time is dependent on supply ramp rate from 0 ->2.7V, hence can vary from one application to another. Measure from where supply reaches its POR threshold as per device datasheet. • Independent of IRC clock – untrimmed at this point in sequence. • 1.2V regulator startup time will be max 300µs. Max can be anything dependent on supply ramp rate.
Phase 0	18	22	• Regulator stable • A Factor of +/-10% requires to be taken into account as the FIRC is an untrimmed clock at this stage. • Entered from any phase, power-on or destructive reset event. Phase 0 tasks: 1. Power Up has completed 2. Fast internal RC oscillator(16 MHz) clock is running 3. All enabled 'destructive' resets have been processed
Phase 1	10.5	13.5	• Phase 1 is entered either on exit from PHASE0 or immediately from PHASE2, PHASE3, or IDLE. • A Factor of +/-10% requires to be taken into account as the FIRC is an untrimmed clock at this stage. Phase 1 tasks: 1. All enabled, non-shortened 'functional' resets have been processed 2. A minimum of 10 FIRC oscillator (16 MHz) clock cycles have elapsed
Phase 2	75	125	• Only entered from phase 1 • A Factor of +/-10% requires to be taken into account as the FIRC is an untrimmed clock at this stage. Phase 2 Tasks 1. Code and data flash initialization 2. A minimum of 8 FIRC oscillator (16 MHz) clock cycles have elapsed
Phase 3[1]	11	13	• Entered from phase 2 or idle • Run on trimmed IRC (depending on trimming accuracy (+-5% assumed)
Phase 3: Number of DCF Records loaded (factory program)	37	47	• 8 cycles per record (min based on 78 DCF's @16MHz+5%, max assumes 88 DCFs @16MHz-5%)
Phase3: DCF Records to shadow flash (user program)	User	User	• User defined. Individual records to be fetched and executed equals 8 cycles.

Table 1 Reset Timing of each of the Reset Phases

[1] Phase 3 can be elongated based on number of DCF reads that are going to be done by SSCM during power up. Device will continue to be in Phase 3 till external reset is asserted.

It should be noted that (device configuration) DCF records are only applicable to MPC564xB/C MCUs. These are used by the (SSCM) system status and control module at boot to program various functions/parameters of the device such as (MBIST) memory built in self test and the (CSE) cryptographic service engine module (hardware security module). The latter will have an impact upon the reset timing if enabled and how these are configured will impact the reset timing. Refer to MPC564xB Reference Manual available from www.freescale.com for information on the STCU (self-test control unit) and CSE modules.

Table 1 and Figure 2 can be viewed together to visualize the steps that are necessary through reset. The state machine that manages the execution of the phases waits for a minimum duration until all processes of that phase have been completed prior to moving onto the next phase.

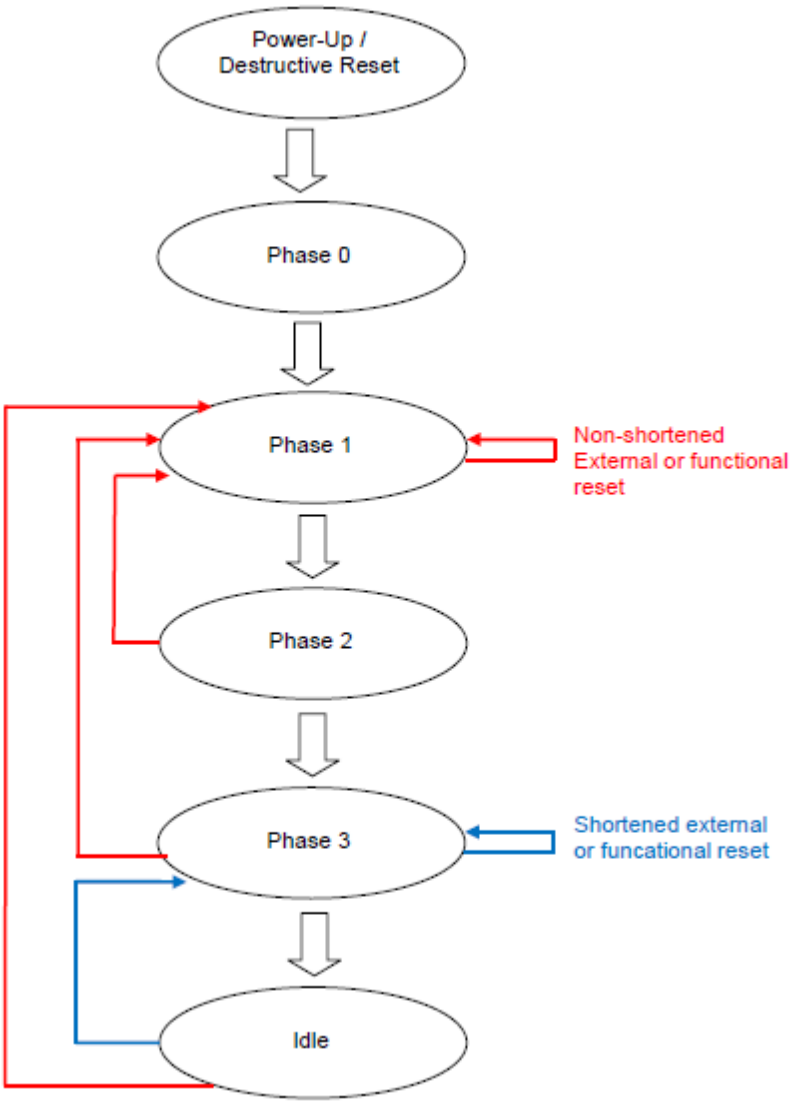


Figure 2 Reset Phases

4.1 Reset Types

Figure 2 phases can be entered through various types of reset. The type of reset generated will depend upon the source of the reset. The arrows illustrate the possible entry to each of the phases. The MCU reference manual provides a full explanation of the reset types (including sources), however, the bullets below are a summary of the possible reset types and the phases they occupy:

- Destructive Reset: Phase 0 + Phase1 + Phase 2 + Phase 3
- External Reset: Phase1 + Phase 2 + Phase 3
- Functional Reset*: Phase1 + Phase 2 + Phase 3 *NOTE: When RGM_FESS.SS = 1, reset phase only from Phase 3 (skipping Phase 1 & 2)
- Long reset: Phase1 + Phase 2 + Phase 3
- Short reset: Phase 3

NOTE

Time to move from DRUN -> RUNx is totally dependent on application software.

5 External Pin Configuration during RESET

During reset the external pins are tri-stated i.e. they do not accept inputs or provide outputs. The pins will only become functional once the reset idle phase has been reached. There are some functional pins (e.g. boot pins PA[8] and PA[9]) which will function during reset, but cannot be used for any other purpose.

6 RESET Pin External Components

The following information has been derived from the datasheet and estimates the ‘worst case’ cross over voltage level and timing for the reset pin to begin sampling.

For external components connected to the RESET pin, the following points should be noted with regarding to the timing and the input high/low levels of activation on this pin.

- The minimum level at which an input high will register is 0.65*Vdd
- The maximum frequecy at which the FIRC, internal default clock, will run is 20MHz (50ns period) (untrimmed)

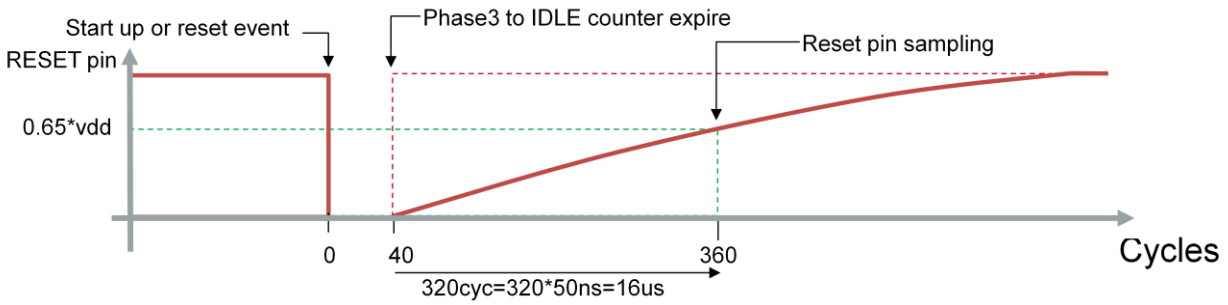
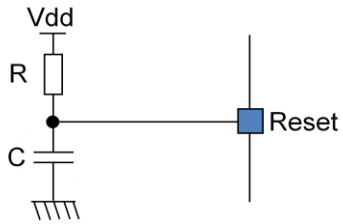


Figure 3 Activity on the Reset pin to begin sampling

During startup, the external reset pad (which is bidirectional) is pulled low by reset generation module (RGM) until "Phase3 to IDLE counter" expires (40 cycles). If the external reset is held low for more than 320 cycles then the external reset bit is set.
If the external reset is released before this then the external reset flag is not set. In the case of normal execution ongoing, then the appropriate reset status flag is set as soon as external reset arrives.

On the reset pin, a 10kΩ pull-up resistor is sufficient and if additional capacitance is required on this pin, then based on the pull up resistor and timing constraint, it can be determined the recommended capacitor value:

Example: $16\mu s=R*C$; $C_{max}=16*10^{-6}/10*10^{3}$; $C_{max}=1.6nF$



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