

i.MX 6SoloX Migration Guide

Migrating from i.MX 6Solo to i.MX 6SoloX

1 Introduction

1.1 Purpose

This Application Note provides an introduction to the i.MX 6SoloX architecture by highlighting the differences with the i.MX 6 Series processor upon which it is based, namely the [i.MX 6Solo](#). This document is intended to be a migration guide for development teams that are porting platforms from [i.MX 6Solo](#) to i.MX 6SoloX.

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1.2 Scope

The i.MX 6SoloX was developed with extensive reuse of existing Freescale designs including:

- Extensive reuse and alignment with [i.MX 6Solo](#)
- Modules reused/modified from [i.MX 6SoloLite](#)
- Modules reused/modified from [Vybrid](#)

Due to the close alignment with the [i.MX 6Solo](#) design, this white paper will be structured as a change summary from the [i.MX 6Solo](#) features. In addition, references to modules that have been reused or modified from [i.MX 6SoloLite](#) and [Vybrid](#) will be provided.

The i.MX 6SoloX architecture introduces new features that provide differentiation from other members of the i.MX 6 Series. Some key differentiators include:

- i.MX 6SoloX is the first i.MX 6 Series processor to provide asymmetric multiprocessing (AMP) by integrating Cortex-A9 and Cortex-M4 CPUs. Features that allow multiple execution environments to communicate and safely share resources are supported in hardware.
- Integrated Ethernet support has been upgraded to provide dual 1 Gigabit ports with AVB support.
- Analog integration has been enhanced by including general-purpose and video ADC interfaces.

This white paper will highlight new features added to the i.MX 6SoloX design that require additional consideration when porting designs based on [i.MX 6Solo](#).

1.3 Audience

The content of this document is targeted towards system integrators and software developers migrating from platforms based on [i.MX 6Solo](#).

2 Feature Change Summary

This section will summarize the architectural changes for i.MX 6SoloX with respect to [i.MX 6Solo](#).

Category	Feature	Change from i.MX 6Solo	Comment
CPU	Cortex-A9 L2 Cache Size	L2 reduced from 512KB to 256KB.	i.MX 6Solo/6DualLite includes 512KB to support SMP configurations with dual Cortex-A9 CPUs (i.MX 6DualLite).
	Cortex-A9 L2 Cache as OCRAM	L2 memory array (256 KB) can be configured as OCRAM to extend the available on-chip memory.	This feature is supported on i.MX 6SoloLite .
	Cortex-M4 Platform	Add Cortex-M4 platform: <ul style="list-style-type: none"> • 16KB I-Cache • 16KB D-Cache • 64KB TCM (tightly coupled memory) divided into 32KB lower (TCML) and 32KB upper (TCMU) regions 	<p>Secondary processor for fast-boot, low-power processing, and robust CAN message handling.</p> <p>The Cortex-M4 platform from Vybrid is reused with the following changes:</p> <ul style="list-style-type: none"> • Add core MPU for additional control of memory attributes • Updated memory map to reflect alignment with i.MX6 family. • No interrupt routing. All IRQs are mapped to Cortex-M4 and Cortex-A9 CPUs. • MU (messaging unit) provides interprocessor interrupts. • Direct boot from Cortex-M4 is not supported. • Boot vector will be in TCML and populated by Cortex-A9. • Exclusive access support (synchronization primitives supported using LDREX and STREX instructions)
Interprocessor Communication & Synchronization	SEMA4	1 instance of the SEMA4 module added to support hardware-enforced semaphores.	SEMA4 module is reused from Vybrid .
	MU	1 instance of the MU (messaging unit) module added to support interprocessor communication between the Cortex-A9 and Cortex-M4	

Category	Feature	Change from i.MX 6Solo	Comment
Multicore Isolation/Sharing	RDC	Add RDC module (resource domain controller) to support domain-based access control to shared resources.	
	SEMA42	Add 2 instances of SEMA42 module to support safe access to shared peripherals.	SEMA42 is similar to SEMA4 with the following key differences: <ul style="list-style-type: none"> SEMA42 increases the number of access domains from 2 to 15 SEMA42 does not have interrupt to indicate semaphore release RDC programming model supports the option to require hardware semaphore for peripherals shared between domains. Signaling between the SEMA42 and RDC binds peripherals to semaphore gates within SEMA42.
	AIPSTZ, SPBA	Updated to support domain-based peripheral access control.	RDC programming model is used to configure peripheral access rights for each domain.
	DSEC, DEXSC	Updated to support domain-based access control of memory regions.	RDC programming model is used to configure memory regions and access rights for each domain.
Timers	WDOG	Increase WDOG instances from 2 to 3.	Additional WDOG for Cortex-M4 usage.
Internal Memory	OCRAM_S	Add 16KB on-chip memory in the always-on power domain.	OCRAM_S can be used by software for state retention of the CPU and other hardware blocks.
	Secure RAM	Increase Secure RAM size from 16KB to 32KB.	
External Memory	QSPI	2 instances of Quad SPI added.	Each QSPI instance supports dual-channel and DDR capability. QSPI module is reused from Vybrid .
	RAW NAND	Upgrade BCH40 to BCH62 to support 62-bit ECC and randomization.	
Security	HAB	HAB updates to improve secure boot times	HAB will support a new fast authentication option that reduces the required signatures from 4 to 2 without compromising the level of security.

Category	Feature	Change from i.MX 6Solo	Comment
Video	VPU	VPU removed.	Video encode/decode requires Cortex-A9 software.
	VDOA	VDOA removed.	Not needed since VPU removed.
Camera, Display, & Graphics	VADC	Video ADC added to support NTSC/PAL analog video input.	Provides cost-effective support of analog rearview cameras. VADC module is reused from Vybrid .
	VDEC	Add composite video decoder to provide NTSC/PAL decoding.	Decodes NTSC/PAL signals from analog camera into YUV. VDEC module is reused from Vybrid .
	HDMI	HDMI transmitter removed.	
	MIPI/CSI-2	MIPI/CSI-2 receiver removed.	
	MIPI/DSI	MIPI/DSI transmitter removed.	
	IPU	IPU removed.	IPU functionality replaced with CSI + PXP + LCDIF
	CSI	2 parallel CSI ports added.	CSI module from i.MX 6SoloLite will be reused with the following modifications: <ul style="list-style-type: none"> Support 24-bit YUV input Support simple video deinterlacing Support field input signal
	PXP	PXP can be used to support CSC, compositing, rotation, and resize operations previously supported by IPU.	PXP module from i.MX 6Solo will be reused.
	GIS	GIS (General Interrupt Service) module added.	GIS can be used to automate the flow of data from the camera to the display.
	LCDIF	2 instances of LCDIF added.	LCDIF module from i.MX 6SoloLite will be reused with the following modifications: <ul style="list-style-type: none"> Blending of overlay buffer with same height and width as display buffer Local/global alpha blending of overlay buffer
	LVDS	Reduced from 2 channels to 1.	
GPU	GC880 and GC320 removed. GC400T added.	GC400T provides integrated 2D and 3D support.	
EPDC	EPDC (Electrophoretic Display Controller) removed.		

Category	Feature	Change from i.MX 6Solo	Comment
Audio	SAI	Add 2 SAI instances to increase the number of I2S audio interfaces from 2 to 5 (3 SSI + 2 SAI).	Unlike the SSI, the SAI interfaces do not flow through AUDMUX. The SAI modules support increased FIFO depth (64x32-bit) over the SSI. The SAI module is reused from Vybrid . Note: The ESAI from i.MX 6Solo is also available on i.MX 6SoloX.
Connectivity	ENET	Increased ENET instances from 1 to 2. Both ENET instances support AVB.	ENET module from i.MX 6Solo updated with the following modifications: <ul style="list-style-type: none"> • Dual 64-bit AXI bus interface • Improved bus fabric priority control • 8K RX & TX FIFO size • Unaligned buffer support • Interrupt coalescing • AVB support
	MIPI_HSI	MIPI_HSI removed.	
	MLB	MLB support for MOST150 removed. DTCP cipher accelerator removed.	MLB module from i.MX 6Solo reused with the following modifications: <ul style="list-style-type: none"> • Only MOST25, MOST50 supported. • DTCP removed.
	UART	Increase UART instances from 5 to 6.	
	PWM	Increase PWM instances from 4 to 8.	
	SPI	Increase SPI instances from 4 to 5.	
	ADC	2 instances of 12-bit ADC added.	ADC module from Vybrid is reused.
Analog	Temperature Sensor	Temperature sensor will be modified to have three programmable trip points (low, high, panic). The panic trip point will be capable of generating a system reset.	The changes to the sensor functionality allow an interrupt to be generated when temperatures fall outside of the programmed window. The panic reset provides a hardware failsafe when temperatures reach dangerous levels.

Category	Feature	Change from i.MX 6Solo	Comment
Power	LDO_PU	LDO_PU removed. VDDPU_CAP pins removed.	GPU will be powered from VDDSOC. IPU and VPU modules powered by LDO_PU on i.MX 6Solo are removed.
	LDO_PCIE	LDO_PCIE added. LDO_PCIE supply is VDD_SOC_IN and connects to PCIE_VP/VPTX pads.	LDO_PCIE provides power for the PCIe PHY digital logic.
	L2 Power Gating	Support L2 cache power gating.	L2 cache will support the following power gating options: <ul style="list-style-type: none"> L2 cache memory remains powered and retains state during Cortex-A9 power gating. L2 cache memory will be powered down and lose state during Cortex-A9 power gating.
	SNVS	ONOFF pin behavior updated to align with Android requirements.	
Debug	DBGMON	DBGMON added.	DBGMON is a real-time debug monitor to record last AXI transaction before system reset. DBGMON module from i.MX 6SoloLite will be reused.
	Debug Signals	Peripheral debug signals routed based on RDC configuration.	RDC configuration will be used to determine how a peripheral responds when the Cortex-M4 and Cortex-A9 enter debug modes.
System Integration	Memory Map	Cortex-A9 memory map updated to reflect IP changes.	Refer to Memory Map chapter in the Reference Manual for full details.
	IRQ Map	IRQ map updated to reflect IP changes.	Refer to IRQ map chapter in the Reference Manual for full details.
	DMA Map	DMA map updated to reflect IP changes.	Refer to DMA map chapter in the Reference Manual for full details.
	Fuse Map	Fuse map updated to reflect IP changes.	Refer to Fuse map chapter in the Reference Manual for full details.
	CSU	CSU programming model updated to reflect IP changes.	Refer to Security Reference manual for full details.
	CCM	Clock tree updated to reflect IP changes and optimize for low power.	CCM module from i.MX 6Solo reused with modifications including: <ul style="list-style-type: none"> Dedicated clock roots for IP blocks that have been removed will be removed or connected to new IP blocks. 24 MHz RC OSC option is available for use in low-power modes with XTAL powered off. Audio/Video PLL will support on-the-fly changes to provide a tunable media clock.

3 Revision History

The following table provides a revision history for this white paper.

Document Revision History

Rev. Number	Date	Revision
Rev. 0	02/2015	Initial release.

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