Freescale Semiconductor
Application Note

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Assembly Handling and Thermal Solutions for Lidless Flip Chip Ball Grid Array Packages

Contents

1 Introduction

This application note provides recommendations on the assembly handling and application of thermal management solutions for lidless Flip Chip Plastic Ball Grid Array (FC-PBGA) components.

Freescale's FC-PBGA is a laminate-based BGA packaging solution that provides competitive solutions for higher performance applications.

- Improved board-level, solder-joint reliability and lower cost compared to FC CBGA
- Custom substrate designs / ball maps for maximum routing flexibility and electrical performance
- Custom ball patterns / full arrays / depopulated arrays available, up to ~1300 I/O
- Substrates use standard organic PCB manufacturing and HDI build up technologies
- FC-PBGA footprint is a drop-in replacement (PCB design and board assembly) for WB PBGA for the same ball diameter and pitch.
- Capability to withstand lead–free reflow processes (260C reflow)
- Proven reliability in industrial environments
- Lead–free solder balls available

For more information, see Freescale's package technologies.

2 Overview of Flip Chip Plastic Ball Grid Array packages

Flip Chip Plastic Ball Grid Array (FC-PBGA) packages feature a semiconductor die or chip, which is flipped so that the active side of the device faces the package substrate. A device may have one of three FC-PBGA configurations, which are listed in the table below.

In the lidless configuration, exposure of the chip's backside allows for direct contact between the chip and heat sink, which improves the overall thermal performance of the chip. Note that, because the chip's backside is exposed, the engineer must exercise caution when placing the component on the printed circuit board, testing operations, and applying a heat-sink solution. The sections below provide guidelines for handling the assembly, and applying a heat sink.

While lidless packages achieve better thermal performance, flat- and full-lidded packages ease handling by providing a lid that both protects the die and distributes heat.

Table 1. FC-PBGA configuration options

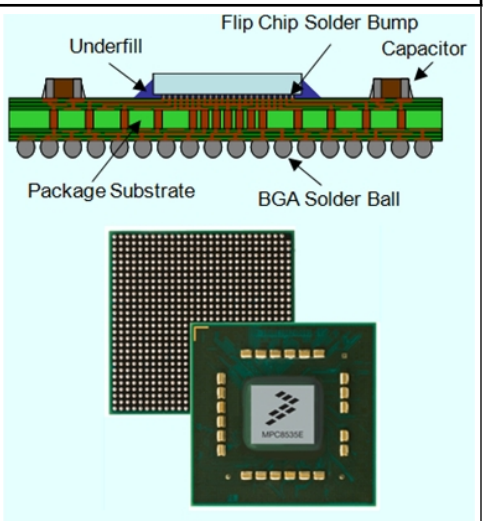
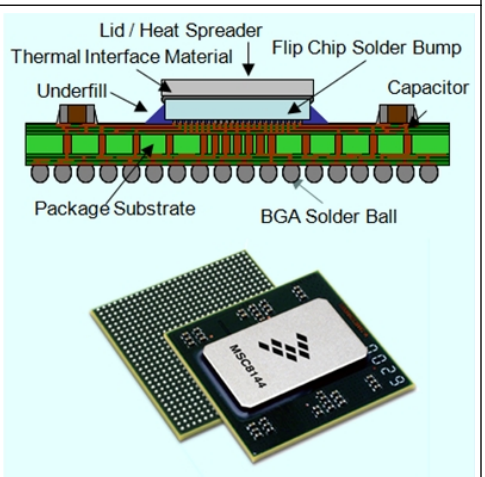
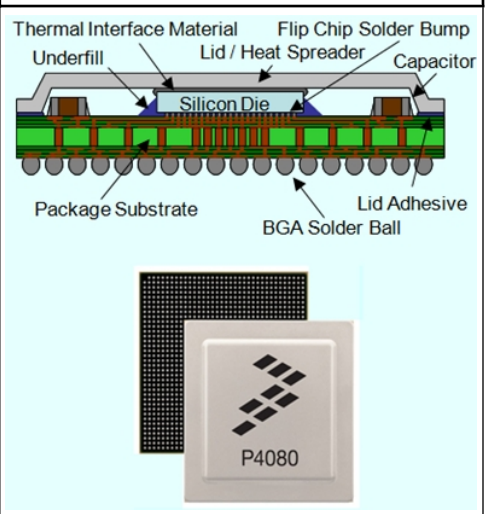
Configuration name	Characterized by...	Handling	Thermal management	Example
Lidless	No lid present	Exercise caution when placing the component on the printed circuit board.	Exercise caution when applying a heat-sink solution.	
Flat-lidded	Lid covers die	Avoid impact to lid. Lid-adhesive thermal interface material is stronger than that of the full-lidded configuration, which directly couples to the package substrate.	Warning: Applying uneven force, or bonding heat-sink to lid, can damage the lid-to-chip bond. For more information, see Attaching the heat sink to a lidless package.	

Table continues on the next page...

Table 1. FC-PBGA configuration options (continued)

Configuration name	Characterized by...	Handling	Thermal management	Example
Full-lidded	Lid covers device	Lid protects the die	Bonded adhesive, capable of withstanding the force of the heat-sink, couples the protective lid to the package substrate.	

3 Compare thermal performance for lidless and lidded packages

With a properly designed heat-sink and Thermal Interface Material (TIM) system, lidless Flip Chip Ball Grid Array components can achieve thermal resistance values better than those of a lidded package.

The following examples show relative thermal performance for thermal solutions for both lidded and lidless 780 I/O 23x23mm FC-PBGA packages.

NOTE

These simulations assume a standard JEDEC open-flow environment. This may not always be practical, or even possible, in a high-volume manufacturing environment or end application.

Table 2. Use case thermal characteristics for lidless 780 FC-PBGA 23x23mm die

Rating	Board	Symbol	Value	Units	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\Theta JA}$	28	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	19	°C/W	1, 2
Junction to ambient (@200ft/min)	Single-layer board (1s)	$R_{\Theta JMA}$	22	°C/W	1, 2
Junction to ambient (@200ft/min)	Four-layer board (2s2p)	$R_{\Theta JMA}$	15	°C/W	1, 2
Junction to board	-	$R_{\Theta JB}$	9	°C/W	2

Table continues on the next page...

Table 2. Use case thermal characteristics for lidless 780 FC-PBGA 23x23mm die (continued)

Rating	Board	Symbol	Value	Units	Notes
Junction to case (top)	-	$R_{\Theta JCtop}$	<0.1	°C/W	3

Notes:
1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Junction-to-lid-top thermal resistance determined using the MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and cold plate.

Table 3. Use case thermal characteristics for full-lidded 780 FC-PBGA 23x23mm die

Rating	Board	Symbol	Value	Units	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\Theta JA}$	22	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	14	°C/W	1, 2
Junction to ambient (@200ft/min)	Single-layer board (1s)	$R_{\Theta JMA}$	15	°C/W	1, 2
Junction to ambient (@200ft/min)	Four-layer board (2s2p)	$R_{\Theta JMA}$	10	°C/W	1, 2
Junction to board	-	$R_{\Theta JB}$	4	°C/W	2
Junction to case (top)	-	$R_{\Theta JCtop}$	0.8	°C/W	3
Junction to lid (top)	-	-	0.35	°C/W	4

Notes:
1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Junction-to-lid-top thermal resistance determined using the MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and cold plate.

This chart compares the thermal resistance of lid and lidless FC-PBGA packages.

NOTE

Simulations performed with 53x54x25mm heat sink.

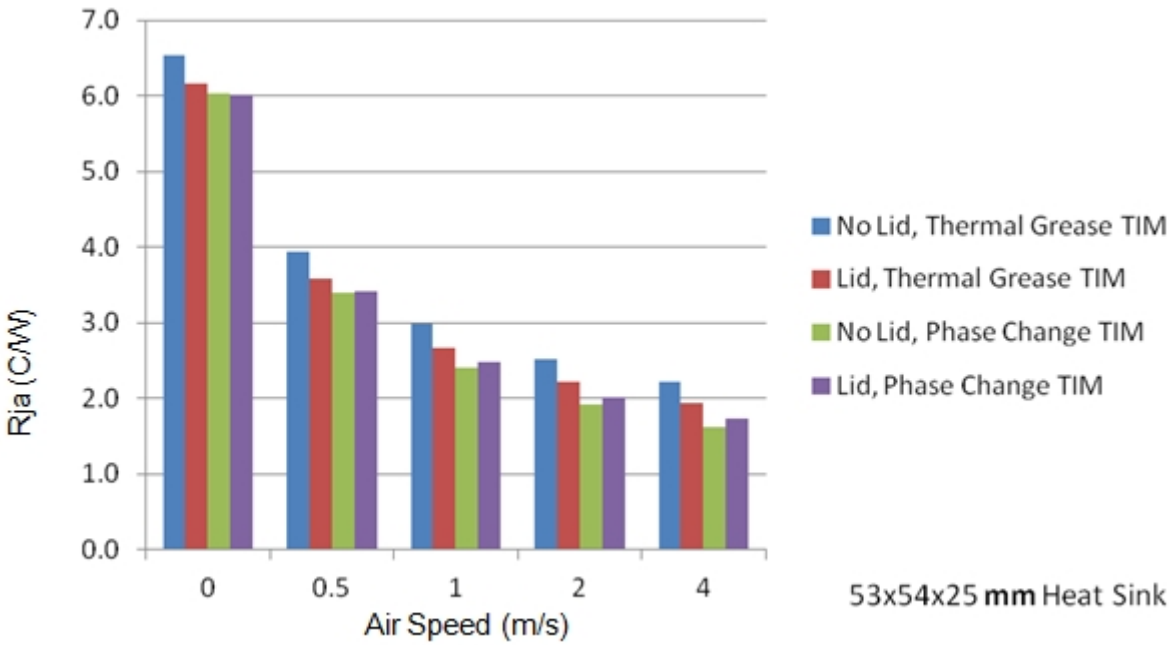


Figure 1. Thermal resistance of lid and lidless packages

4 Handling lidless FC-PBGA packages

Lidless FC-PBGA packages feature an exposed backside, or top surface, of the semiconductor chip, which is often the surface that the designer uses for vacuum-picking and placing the component onto the printed circuit board.

To prevent chipping or fracturing the exposed silicon die backside and edges, exercise caution when handling and placing lidless packages. Do not use a metal pickup tip, as this may damage the exposed die.

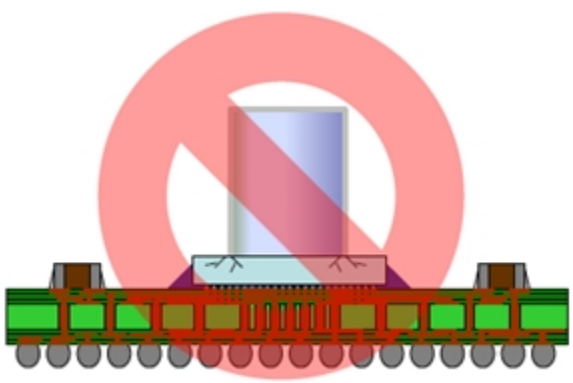


Figure 2. Do not use a metal pickup tip

When picking and placing exposed silicon devices, use a compliant-tip nozzle with a rubber tip and a closed loop head to control force, as shown in the figure below.

NOTE

Consult your pick-and-place equipment provider for pick-up tip size and material recommendations.

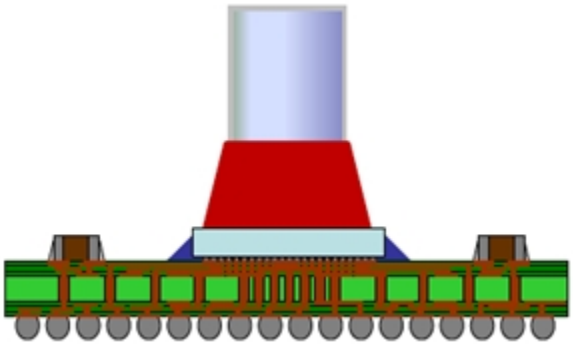


Figure 3. Use a compliant-tip nozzle

When the lidless FC-PBGA component is the tallest component on the printed circuit board, the risk of impact is high. After soldering the package to the printed circuit board, follow the list below to ensure that the lidless FC-PBGA device is not impacted.

To prevent damage, inspect all transport, flipping, and storage tooling and fixtures before using them to handle the components.

- Ensure that the tooling and fixtures do not bend or flex the printed circuit board.
- Ensure that the soldered flip-chip component, which is made from a stiff material, does not crack.

5 Choosing a thermal interface material

Consider the thermal interface material (TIM) options early in your design, as this choice depends on cost targets, package application, manufacturing dynamics, and the performance requirements of the thermal solution. By selecting the appropriate TIM, you can help reduce the size of the heat sinks and the need for larger cooling fans. In the long-term, the appropriate TIM can mitigate the potential cost of changing heat sinks or redesigning a chassis.

Because lidless flip-chip packages have a small surface area compared with that of lidded or molded packages, the combination of an adhesive TIM and heat sink is not recommended. Freescale recommends the following TIMs for lidless packages:

- Phase change TIM (PCTIM)
- Cross-linked thermal gels
- Thermal pads and tapes
- Thermal grease

For more information, see the table below.

High-performance TIMs like greases, compounds and gels, are expensive and may be more difficult to handle during installation. Thermal pads and tape offer an easier heat-sink attachment process, but with reduced performance. Phase-change TIMs provide a compromise solution, which offers ease-of-assembly with good performance.

This table provides advantages and disadvantages of the TIM types recommended for lidless packages.

NOTE

Heat sinks can be ordered with phase-change TIMs pre-applied from the supplier.

Table 4. Recommended TIMs for lidless packages

TIM	Description	Advantage	Disadvantages
Phase-change material	Remains solid at room temperature, and melts at elevated temperatures close to the package operating temperature. The material is in a liquid phase at die-operating conditions.	In its molten phase, where the material is in a viscous state, the material conforms to and wets both the heat sink and die surfaces better than any solid material. This results in a material with low thermal impedance as the thermal contact resistance is significantly reduced.	Requires about 20-40psi of pressure to achieve the recommended TIM bond-line thickness. The heat sink must have adequate loading pressure on the die.
Cross-linked thermal gels	Dispensable materials that cure into a soft compound over time.	Being viscous in pre-cure form, it has the ability to fill into gaps and voids before curing. This enables a low inter-facial thermal resistance.	Material must be dispensed on to the die surface. Requires an automated process to ensure consistent dispensation.
Thermal pads and tapes	Prefabricated thermal interface materials which are supplied at a specified thickness (~0.25-1 mm).	• Most have a core material or wire mesh to retain the structural integrity of the material. • Pre-cut to size (~20% larger than the die size). • Most are tacky on one side for self-adhesion to the heat-sink surface.	Thermal performance is relatively poor compared to the cross-linked thermal gels and phase-change material options.
Thermal grease	Typically silicone oils embedded with thermally conductive filler particles	• Highly conductive • Low thermal resistance • Flows and conforms to surfaces • May be applied with a thin bond-line thickness	Greases can pump-out and dry out over extended periods of operation. Careful application is required to maintain consistent bond-line thickness.

6 Attaching the heat sink to a lidless package

The selection and attachment of a heat sink is as important as the selection of the TIM material. Typically, the device data sheet provides the maximum allowable junction temperature for the device. Depending on the application and the Freescale device involved, most applications require a heat sink, which is selected by the customer.

For lidless configurations, use a heat sink anchored to the PCB for robust mechanical integrity. The heat sink can be anchored using a clip, spring loaded screws, or push pins. To prevent board warpage, a backing plate may be necessary on the side of the printed circuit board opposite the flip-chip device.

6.1 Aligning the heat sink and package

Attaching the heat sink to a lidless package

To avoid die damage or TIM damage during heat sink assembly to package, ensure that the heat sink base remains parallel to the package, and that a uniform layer of thermal interface material is present between the heat sink and the exposed die. The heat sink must not directly contact the exposed die surface.

NOTE

Non-parallel alignment of heat sink and die may damage the die.

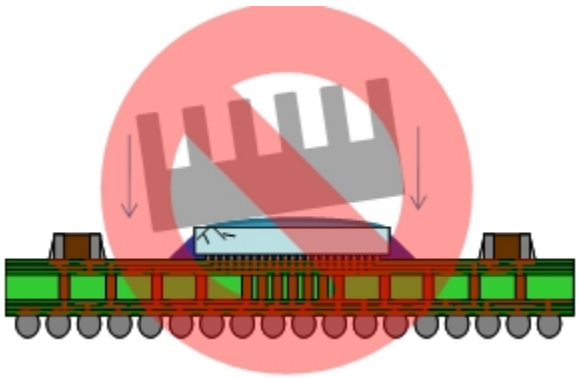


Figure 4. Non-parallel alignment of heat-sink surface and die

Use alignment foam or bumpers around the heat sink periphery to ensure that the base of the heat sink is parallel to the die surface prior to clamping. Apply even pressure on the clip anchor or pushpins located on the opposite sides of the heat sink. Uneven pressure may cause the heat sink to tilt, resulting in an uneven TIM bond-line thickness.

Important

Thermal Interface Material is not a glue. Do not rely on it for adhesion.

Ensure that the heat sink is parallel to the backside surface of the die, as shown in the figure below.

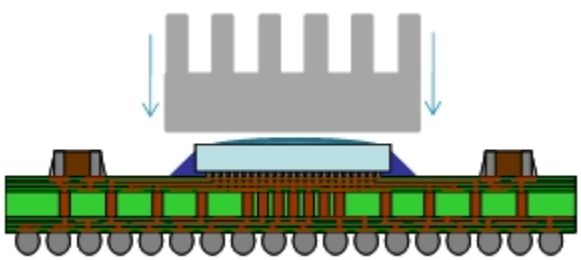


Figure 5. Parallel alignment of heat-sink surface and die

6.2 Maximum force for heat-sink attachment

Maximum allowable heat-sink attachment force varies by package body size. This table provides the maximum allowable force for common Freescale body sizes.

Table 5. Maximum force for common Freescale packages

Body size (mm)	Package I/O count	Maximum allowable force (lb)	Sphere array
19x19	525	10	18x18

Table continues on the next page...

Table 5. Maximum force for common Freescale packages (continued)

Body size (mm)	Package I/O count	Maximum allowable force (lb)	Sphere array
23x23	780	15	22x22
25x25	575	18	24x24
29x29	783	24	28x28
33x33	1023	32	32x32
37.5x37.5	1295	40	36x36
45x45	1935	60	44x44

7 Removing or reworking the heat sink attachment

Before you remove a heat sink, ensure your work area is free of materials that may cause damage, and that the backside surface of the die is clean.

To remove a heat sink, follow these steps:

1. Remove the heat sink by completing the attachment process in reverse order.
2. After removing the clip or anchoring screws, squirt or spray solvent, or other material recommend by the TIM supplier (for example, isopropyl alcohol (IPA)), at the die to heat-sink base interface to soften the TIM material.
3. Slide a dental floss under the heat sink and use a sawing motion to cut the TIM.
4. Use a lint-free cloth, and the same dental floss material mentioned in step 2, to clean the remnants of the TIM from the die surface.
5. Before mounting the new heat sink, inspect the die backside surface to ensure that there is no residual TIM or die scratching, chipping, or cracking present.

8 Revision history

This table provides a revision history for this application note.

Table 6. Revision History

Rev. number	Date	Substantive change(s)
0	02/2014	Initial public release

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