Freescale Semiconductor
Application Note

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Powerline Communication – Analog Front End

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1 Introduction

The MCR2 board is an Analog Front End (AFE) for powerline communication. It is intended to be used with any processor tower card (www.freescale.com/tower) connected via the edge PCI-E connector. It does not fit into the existing tower system due to the fact that it may handle high voltages and there is risk of an electric shock.

The MCR2 analog front end is primarily designed to be used as a development kit for power line protocols such as PRIME or G3 which communicate over the mains[1]. The transmit signal levels and signal purity satisfy the CENELEC 50065 standard. It is tuned to a broadband signal in the 35–90 kHz band. It also provides a transformer-based galvanic isolation.

The MCR2 includes these items:

- Transmitter to inject a signal into the mains
- Receiver to listen to an incoming signal
- Coupling circuit to remove the mains voltage
- Zero-crossing detector providing information about the mains zero-crossing event

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1. Mains refers to standard AC electrical power.

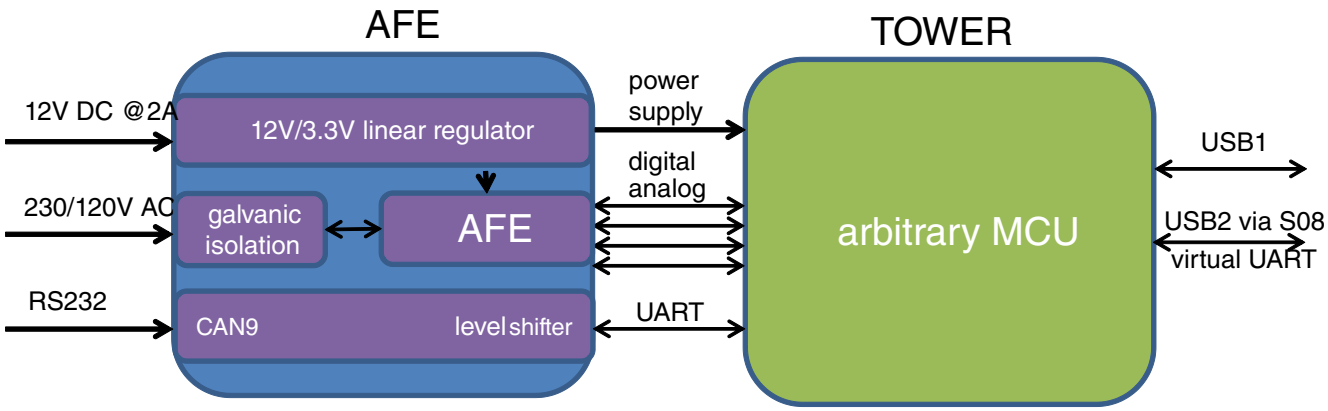


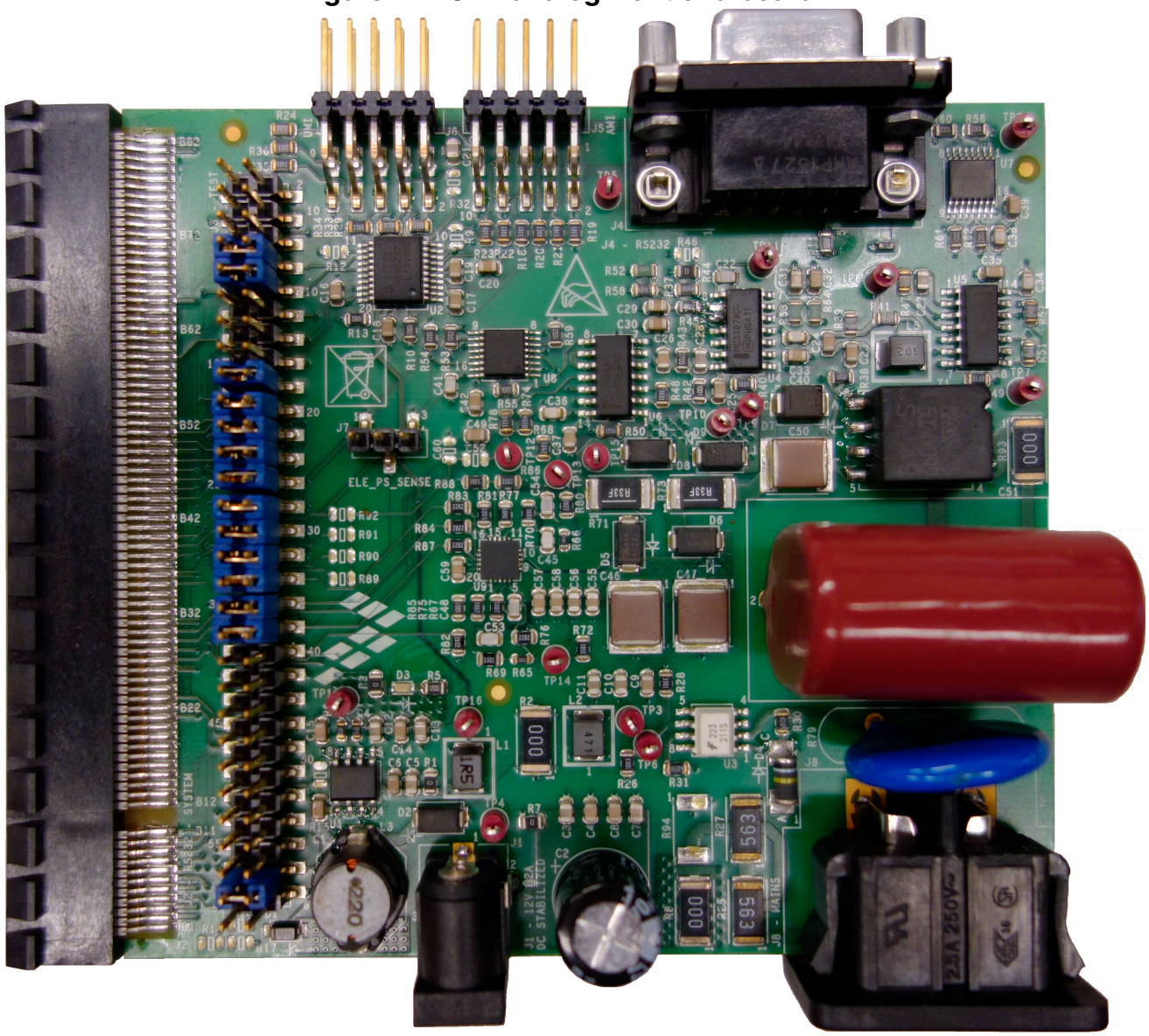
Figure 1. Block diagram

The MCR2 board has to be supplied by a 12 V aDC stabilized power supply with a 2 A peak capability. On the board, a buck voltage regulator of 12 V to 3.3 V feeds the processor tower card and the transmitter logic.

For connectivity purposes, the MCR2 provides a UART TTL to CMOS level shifter and a CANON DB9 connector, and UMI and AMI connectors with the SPI and I^2C buses on the TTL level.

The AFE board may also be used for other types of media such as DC power lines. A full schematic (SCH-2853.pdf) and an orcad layout (LAY-2853.pdf) may be found on the Freescale web pages.

Figure 2. MCR2 analog front end board



2 Connection of the MCR2 and processor tower board

The MCR2 board uses an edge PCI-e connector to connect to the arbitrary processor tower board (primary side). Although the tower system uses dedicated lines to interconnect peripherals, there are variations among boards. For this reason, the majority of the signals used here will go through the J3 header and are connected by jumpers. In the case where some signals are connected to another position, signals may be hardwired to connect them correctly. There are also some free pins on the J3 connector which may be hardwired to an arbitrary pin on the J2 edge connector.

If the tower processor board is powered from the MCR2 3.3 V power supply bus, the ELE_PS_SENSE should be set to 3.3 V by jumper on the J7 header.

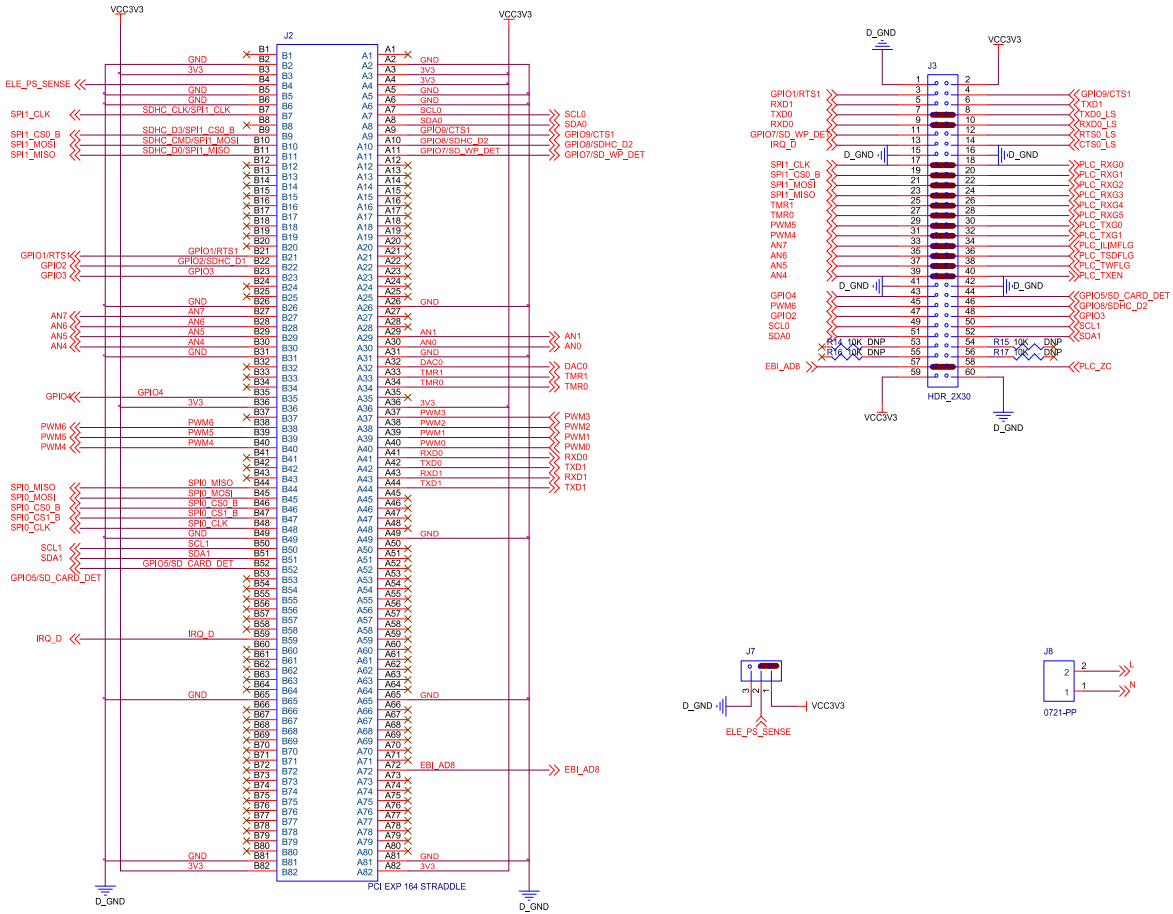


Figure 3. MCR2 AFE connection to tower processor board

3 Transmitter

The transmitter's purpose is to amplify the transmit signal generated by the microcontroller – DAC (default) or PWM periphery (selected by adding either the C49 or C52 capacitor respectively). Both the voltage and current are amplified. The amplifier provides an enable/shutdown to control output to transmit or receive.

The electrical parameters are designed in such a way that the output signal fulfills the CENELEC 50065 standard. The transmitter consists of three sub-blocks:

- Attenuator
- Amplifier
- Protection circuit

3.1 Attenuator

The transmitter offers an attenuator which uses a resistor divider and the U6 switch to decrease the output signal from the selected microprocessor's periphery. The attenuator has four steps of attenuation: 0, 9, 15, and 17 dB.

The attenuator is controlled by the two digital signals PLC_TXG0 and PLC_TXG1, connected to J2[B39] and J2[B40] respectively. If the signals are not driven, attenuation is hard-coded by the pair of resistors R53 and R54 into a 17 dB attenuation. Please check table 1 for signal levels and corresponding attenuation.

Table 1. Transmitter — attenuation control signals

Tower system name	Tower edge conn. J2	PLC signal name	Signal logic state			
PWM4	J2[B40]	PLC_TXG0	0	1	0	1
PWM5	J2[B39]	PLC_TXG1	0	0	1	1
	Attenuation	[dB]	0	9	18	17

Digital input electrical parameters are in table 2.

Table 2. Voltage levels of digital signal

Digital VCC3V3 = 3.3V	Input Low max [V]	Input High min [V]
PLC_TXGx	1	2.5

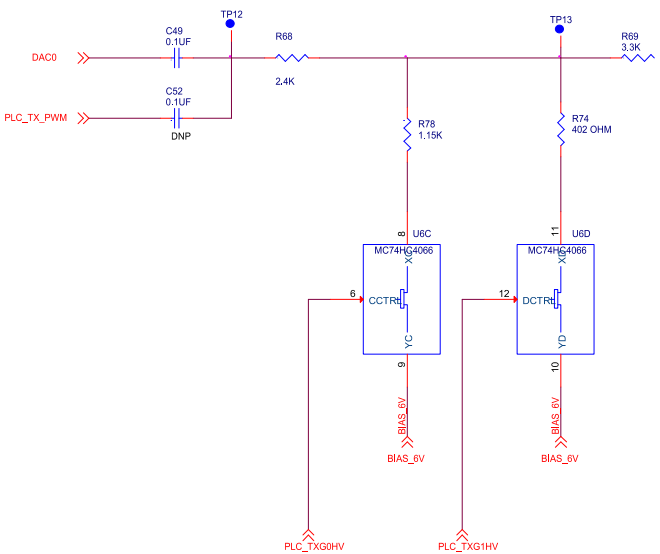
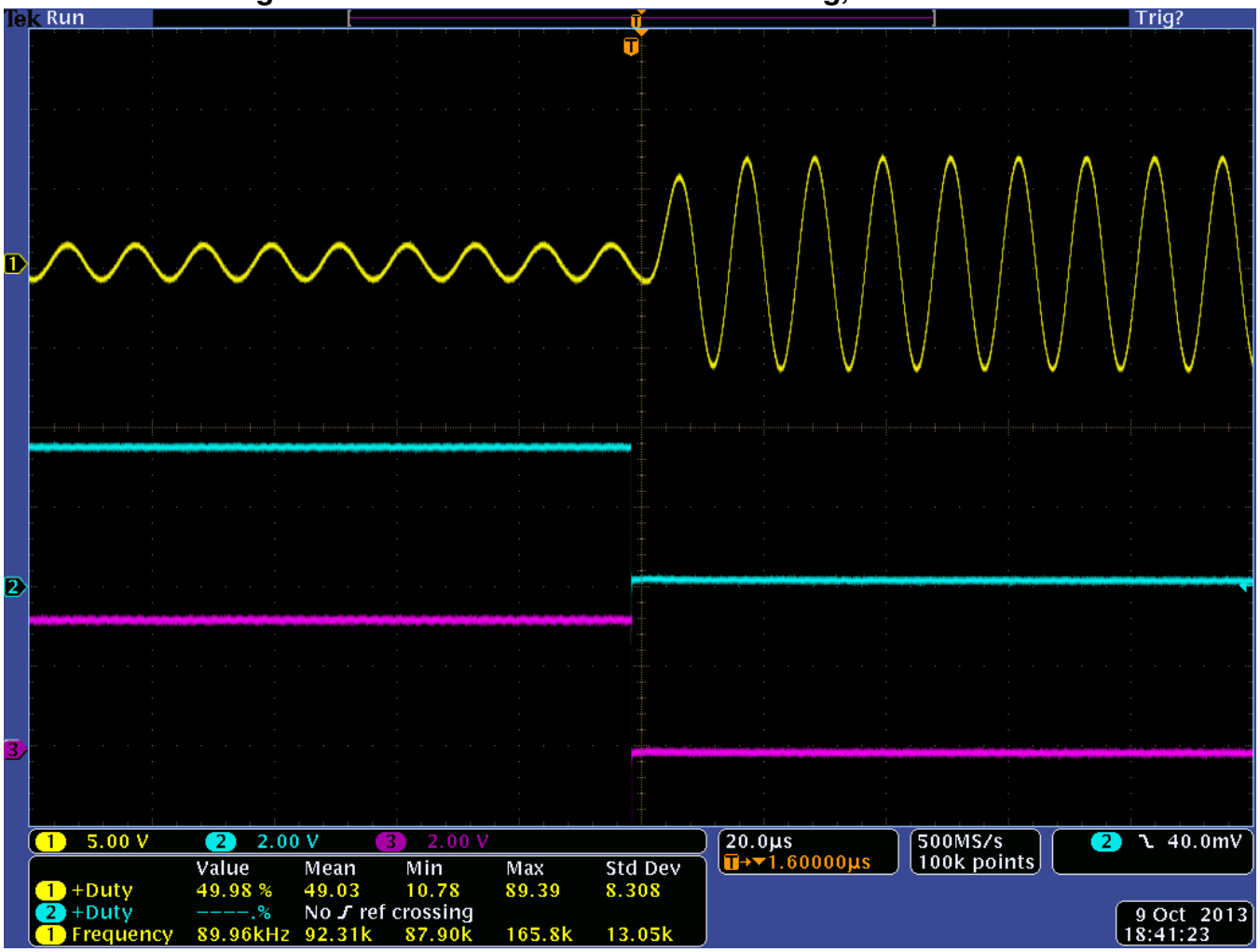


Figure 4. MCR2 transmit attenuator

The attenuation switching is almost immediate, as shown in the figure below.

Figure 5. Transmitter attenuation switching, 17dB -> 0dB



3.2 Amplifier

The transmit amplifier is built up around the NCS5650 PLC Line Driver – the U9 component. It is capable of driving up to 2 A peak into the isolation transformer T1, with an output swing of 12 V_{PP}.

The transmit amplifier design is formed around a fourth-order low-pass Butterworth filter (multi-feedback topology), and the cut-off frequency is set to 115 kHz.

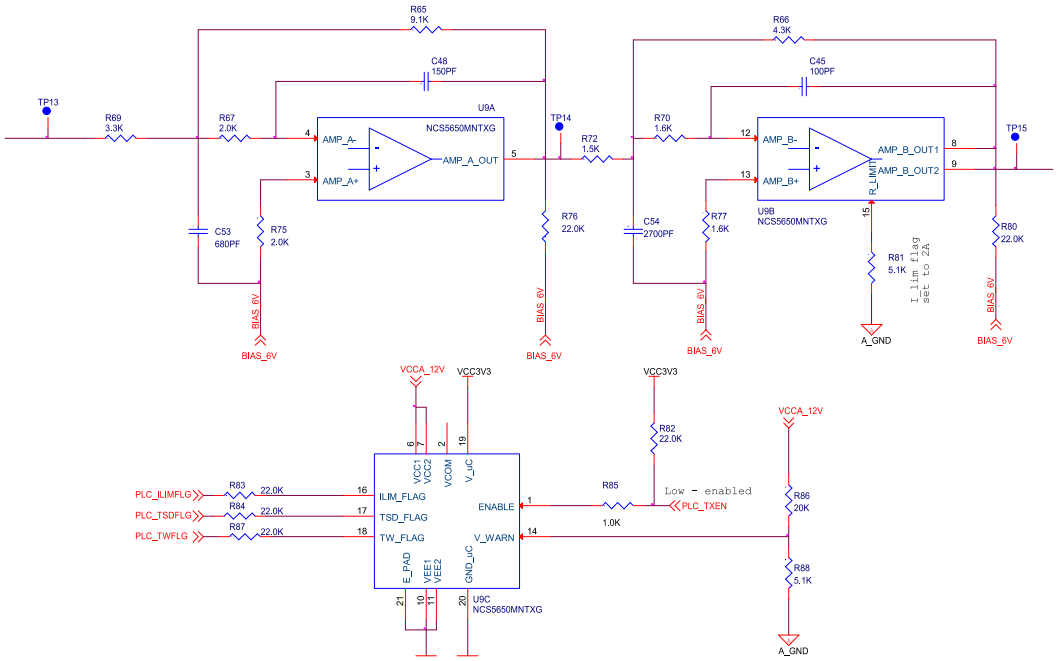


Figure 6. Transmitter amplifier

Each gain stage has a gain of 9 dB, giving a total gain of 18 dB. The maximal output voltage swing is 12 V_{PP} (on the TP15 pin, provided that the power supply voltage VCCA_12V is 13.2 V). The input signal from the microcontroller is decreased by the filter input loss, plus loss on the attenuator (joined together by resistors R68, R78, R74 / R69). The input filter loss plus attenuation gives a maximal input signal voltage from the microcontroller of around 2.6 V_{PP}, so that the DAC should use a ~3 V reference voltage.

Check table 3 for the voltages on the amplifier stages. The TP12 voltage corresponds to the output of the microcontroller (DAC or PWM), while the TP15 voltage is the amplified signal after the last gain stage, in fact, the input to the protection circuit and coupling. Values measured in the table are valid for a 50 kHz signal.

Table 3. Transmitter voltage levels input (TP12), after attenuator (TP13), and output (TP15)

Attenuation [dB]	TP12 [Vpp]	TP13 [Vpp]	TP15 [Vpp]
0	2.6	1.6	12.6
9	2.6	0.7	5.5
15	2.6	0.35	2.7
17	2.6	0.278	2.12

In the following picture,the transfer function of the transmit path for four different attenuations is shown. The input signal is 2.7 V_{PP} generated from the signal generator AFG 3022B. Output is measured at the artificial mains network L2–16, as described in the CELENCE EN50065 standard.

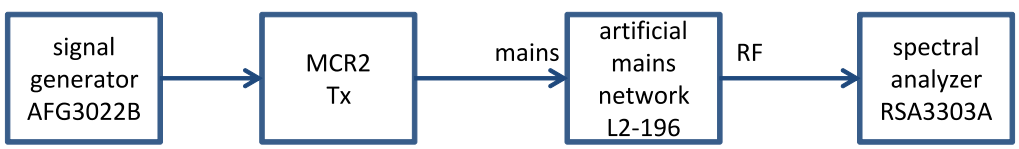


Figure 7. Measurement of the MCR2 AFE transmit path, frequency response

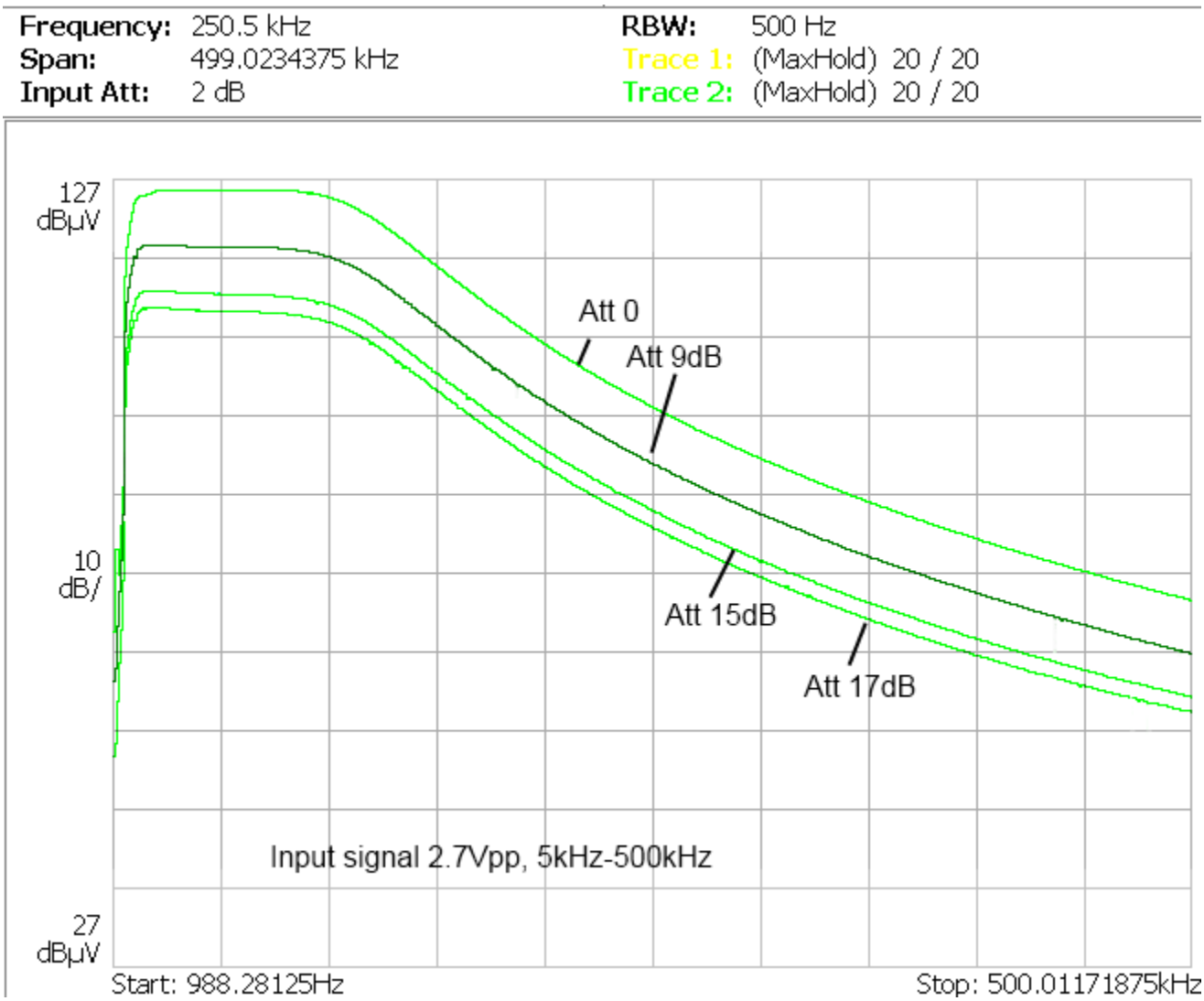


Figure 8. Transmitter transfer function with various attenuations selected

4 Control transmitter amplifier

During reception, the transmitter amplifier has to be disabled — otherwise the received signal will be short-cut. The amplifier is controlled by the PLC_TXEN signal, and when it is in shutdown mode, the amplifier output goes into high impedance mode. If the PLC_TXEN signal is not driven, the transmitter is disabled by default by pullup resistor R82.

The device provides two independent thermal flags with hysteresis. Thermal warning flag PLC_TWFLG is there to let the user know the internal junction temperature has reached a user-programmable thermal warning threshold (set to 105 °C by R86, R88). Thermal shutdown flag PLC_TSDFLG indicates the internal junction temperature has exceeded 150 °C and the device has been shut down.

There is also a current limitation feature that indicates that the output current has reached the programmed maximal value. The maximal current is set to 2 A by resistor R81. When the current exceeds the programmed value, PLC_ILIMFLG is set and action should be taken — for example, the required output voltage may be decreased.

Table 4. Transmitter control / flag signals and connection to the tower edge connector

PLC signal name	Tower system name	Tower edge conn. J2	State 0	State 1
PLC_ILIMFLG	AN7	J2[B28]	OK	Overcurrent
PLC_TSDFLG	AN6	J2[B29]	OK	Shutdown
PLC_TWFLG	AN5	J2[B30]	OK	Temp. > 105 °C
PLC_TXEN	AN4	J2[B31]	Enabled	Disabled

PLC_TXEN, PLC_TWFLG, PLC_TSDFLG, and PLC_ILIMFLG have electrical parameters stated in table 5.

Table 5. Transmitter flag signals and enable signal — electrical parameters

Digital Vdd = 3.3 V	Low max [V]	High min [V]
PLC_ILIMFLG	0.8	2
PLC_TSDFLG output		
PLC_TWFLG		
PLC_TXEN input	0.8	2

The transmitter amplifier on/off switching time is important, due to the limited time between packet reception and transmission. The transmit ON settling time is very short, as shown in picture 9.

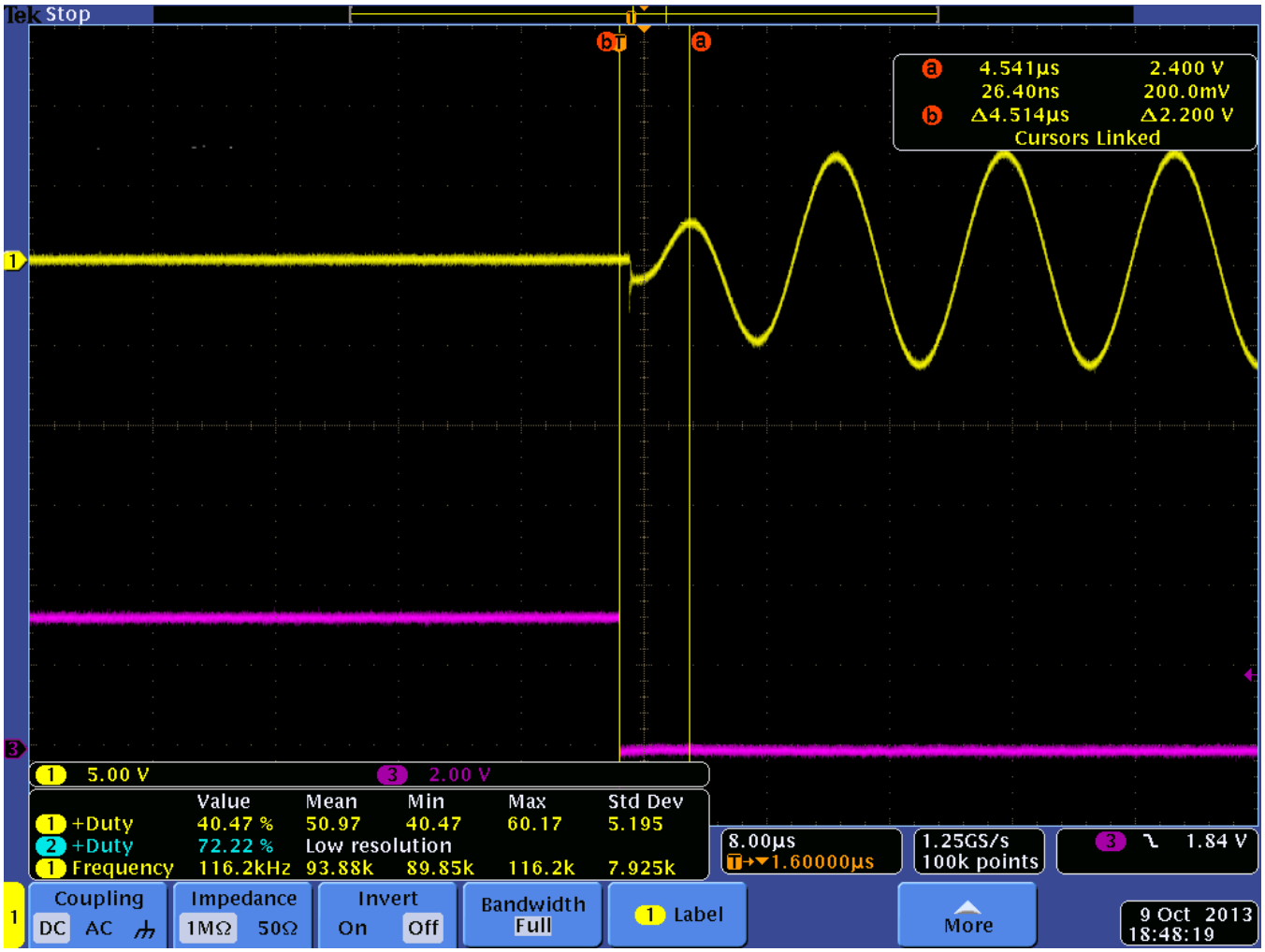


Figure 9. Transmitter amplifier ENABLE settling time

4.1 Protection unit

The transmitter protection circuit is an essential part of the analog front end because the mains is a very hostile environment with a common mode or differential overvoltage. Also, coupling capacitor C51 can inject a high current into the circuit during a hot plug into the mains. Therefore, there is a heavy protection circuit securing the line driver output. The protection circuit introduces an unwanted 0.66 Ω resistivity to the transmitter coupling path.

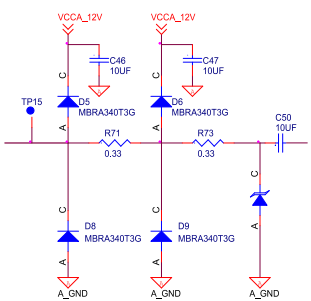


Figure 10. Transmitter amplifier protection circuit

5 Receiver

The receiver's purpose is to amplify the received input signal coming from the mains to a level appropriate to the microcontroller ADC. The receiver path consists of a passive high-pass input filter with a corner frequency of 25 kHz, followed by two PGA stages with a combined gain from 0 dB to 63 dB, and the final stage is a high-pass filter with a corner frequency of 110 kHz. After a final low-pass filter, the signal has a 1.5 V DC level and 3 V_{PP} output swing. Therefore the ADC converter should use ~3 V as its voltage reference.

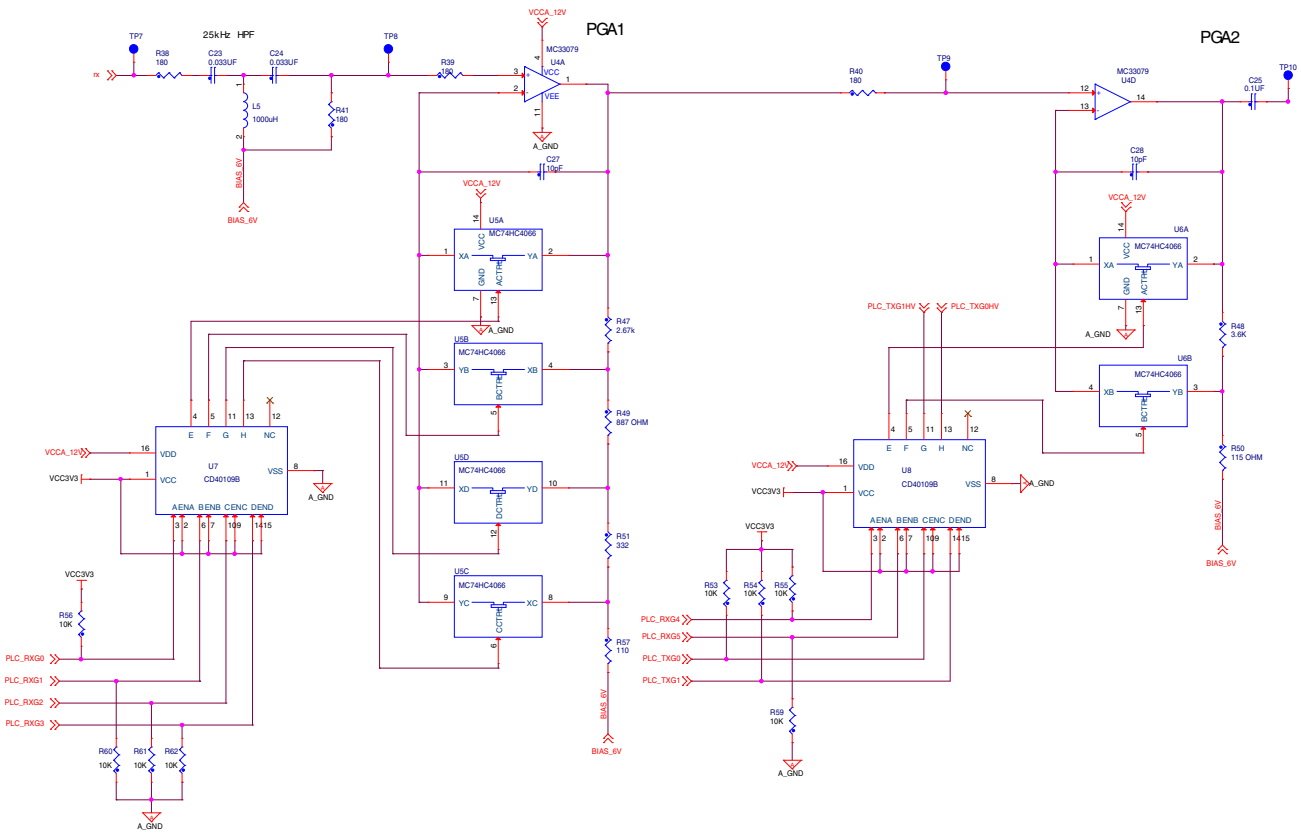


Figure 11. Receiver high-pass filter and two PGA stages

5.1 High-pass filter

There is a third-order high-pass filter built up from passive components C23, C24, and L5 with a cut-off frequency of 25 kHz. The filter has an input impedance of 180 Ω and uses the 180 Ω load resistor R41. The filter has a signal-in band attenuation of 6 dB. The filter removes low-frequency noise and should prevent the following PGA stages from saturation.

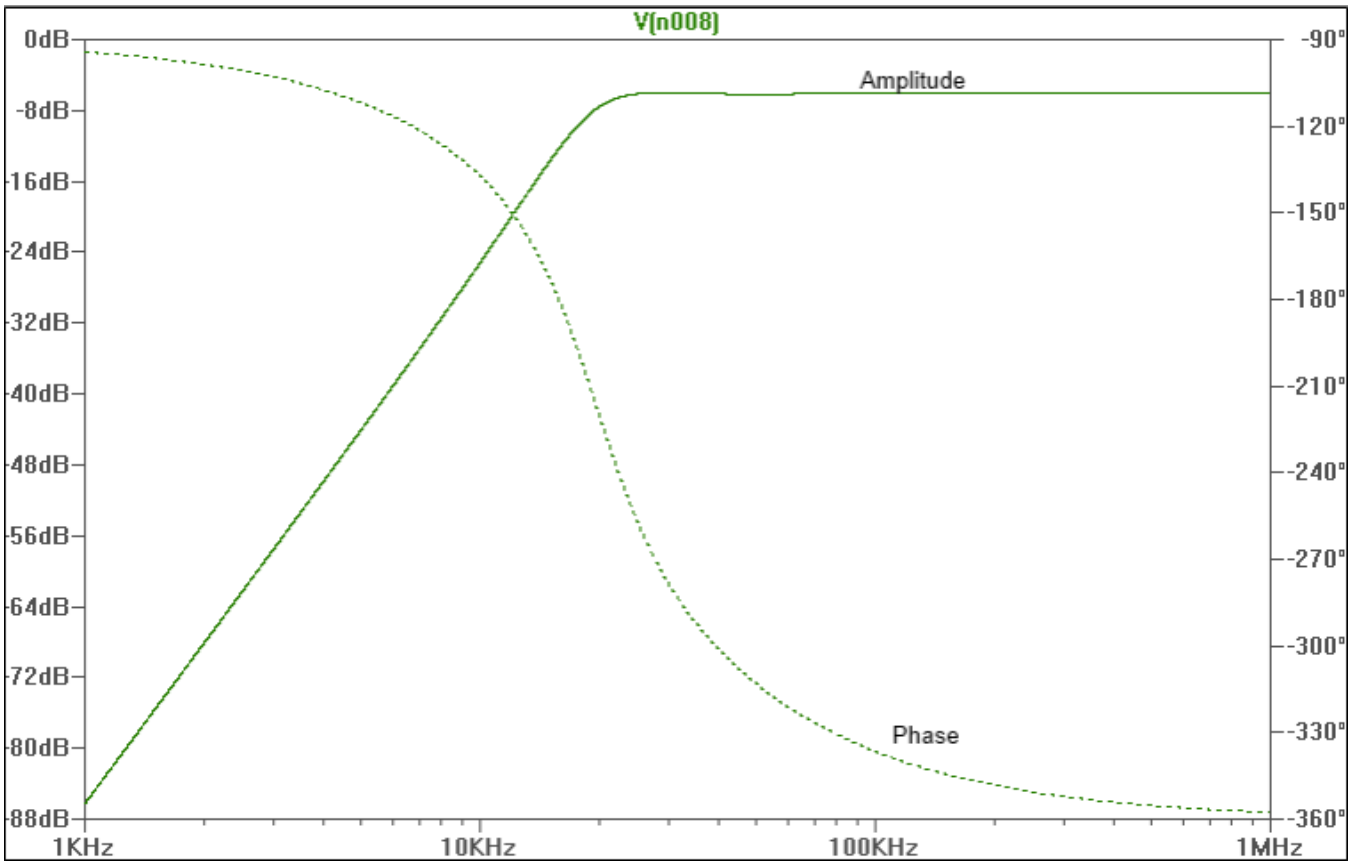


Figure 12. High-pass filter transfer function

5.2 Programmable gain amplifier

As the input signal received from the power line has a dynamic range wider than the microcontroller ADC can overcome, we need to adopt a Programmable Gain Amplifier (PGA) to tailor the signal to a level suitable for the microcontroller ADC input range. The expected dynamic range of the input signal is something like 110 dB, so two stages of PGA are present. The first PGA stage has gain steps 0, 9.5, 19, and 31.5 dB, while the second stage has only two gain steps, 0 and 32 dB.

Table 6 shows the signal levels at various points of the receiver circuit. The maximal received voltage is chosen by the CENELEC signalling limit for a narrowband signal – 134 uVp, the first column in the table. Line attenuation, the second column in the table, varies from 0 to 110 dB. The high-pass filter attenuates the signal by 6 dB. The signal is consecutively amplified by the chosen gain on the first and second stages of the PGA. At the last stage, which is a low-pass filter, the signal is attenuated by 6 dB.

For line attenuation greater than 80 dB, the signal is smaller than 104.5 dBuV so that the ADC input signal is 1/17 FS. From this point, the receive signal decoding will start to lose accuracy.

Table 6. Received signal – levels at various testing points

Tx Signal [dBuVp]	Line Attenuation [dB]	Line input [dBuVp]	High-pass filter -6dB [dbuVp]	PGA1 gain [dB]	PGA1 [dBuVp]	PGA2 gain [dB]	PGA2 [dBuVp]	Low-pass filter -6dB [dBuVp] ADC level
134	0	134	128	0	128	0	128	122

Table continues on the next page...

Table 6. Received signal – levels at various testing points (continued)

Tx Signal [dBuVp]	Line Attenuation [dB]	Line input [dBuVp]	High-pass filter -6dB [dbuVp]	PGA1 gain [dB]	PGA1 [dBuVp]	PGA2 gain [dB]	PGA2 [dBuVp]	Low-pass filter -6dB [dBuVp] ADC level
134	5	129	123	0	123	0	123	117
134	10	124	118	9.7	127.7	0	127.7	121.7
134	15	119	113	9.7	122.7	0	122.7	116.7
134	20	114	108	19	127.12	0	127.12	121.12
134	25	109	103	19.12	122.12	0	122.12	116.12
134	30	104	98	19.12	117.12	0	117.12	111.12
134	35	99	93	0	93	30.1	123.1	117.1
134	40	94	88	9.7	97.7	30.1	127.8	121.8
134	45	89	83	9.7	92.7	30.1	122.8	116.8
134	50	84	78	19.12	97.12	30.1	127.22	121.22
134	55	79	73	19.12	92.12	30.1	122.22	116.22
134	60	74	68	19.12	87.12	30.1	117.22	111.22
134	65	69	63	32.4	95.4	30.1	125.5	119.5
134	70	64	58	32.4	90.4	30.1	120.5	114.5
134	75	59	53	32.4	85.4	30.1	115.5	109.5
134	80	54	48	32.4	80.4	30.1	110.5	104.5
134	85	49	43	32.4	75.4	30.1	105.5	99.5
134	90	44	38	32.4	70.4	30.1	100.5	94.5
134	95	39	33	32.4	65.4	30.1	95.5	89.5
134	100	34	28	32.4	60.4	30.1	90.5	84.5
134	105	29	23	32.4	55.4	30.1	85.5	79.5
134	110	24	18	32.4	50.4	30.1	80.5	74.5

NOTE

It is important to avoid saturating the PGA2 input by selecting an improper gain on the first stage of PGA1.

5.3 Low-pass filter

The last stage of the receiver circuit is a third-order low-pass filter with a corner frequency of 125 kHz, filtering out all the higher frequency noise to fulfill the Nyquist criteria for an ADC converter input. The filter introduces 6 dB of signal attenuation and also shifts the DC voltage level to the 1.5 V level, which is the center of the ADC converter input range, provided that it has a 3 V reference voltage.

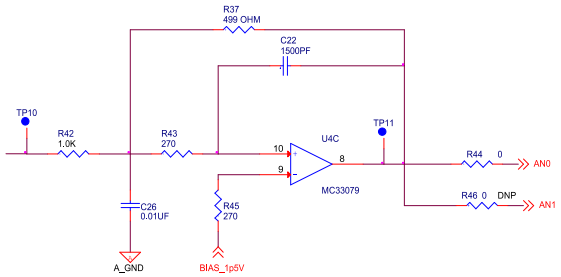


Figure 13. Receiver third-order low-pass filter schematic

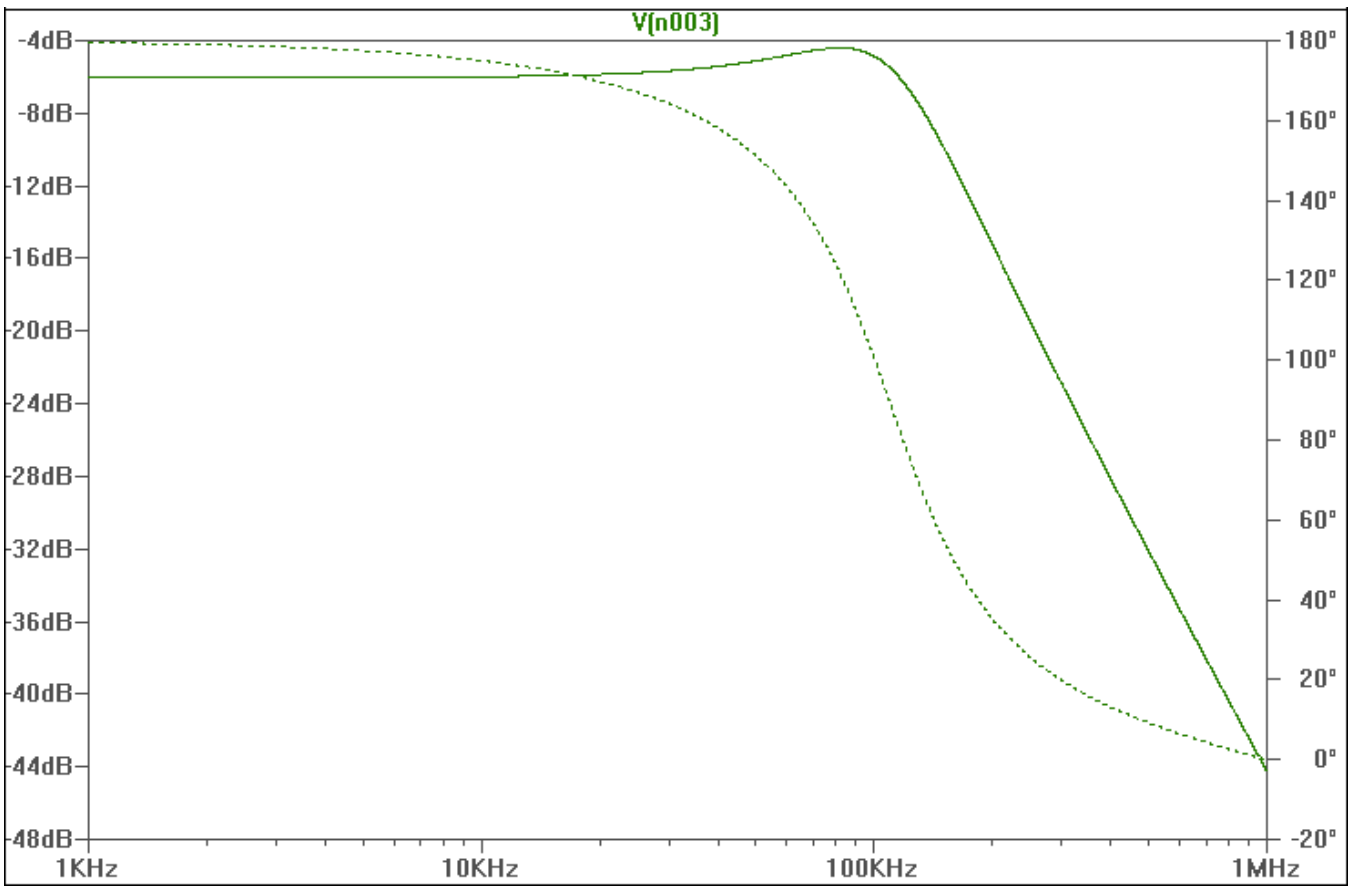


Figure 14. High-pass filter frequency response

Output from the low-pass filter feeds the microprocessor single-ended ADC input. Choose the AN0 or AN1 tower system bus by populating either the R44 or R46 resistors.

Figure 15 shows the full receiver path transfer function for all the gains. The input signal is generated by signal generator AFG3022B connected to the J8 connector. The signal level is 8 mV_{PP}. Green lines correspond to PGA1 gains 0, 9.5, 19, 31 dB and PGA2 0 dB, while blue lines apply to PGA2 32 dB.

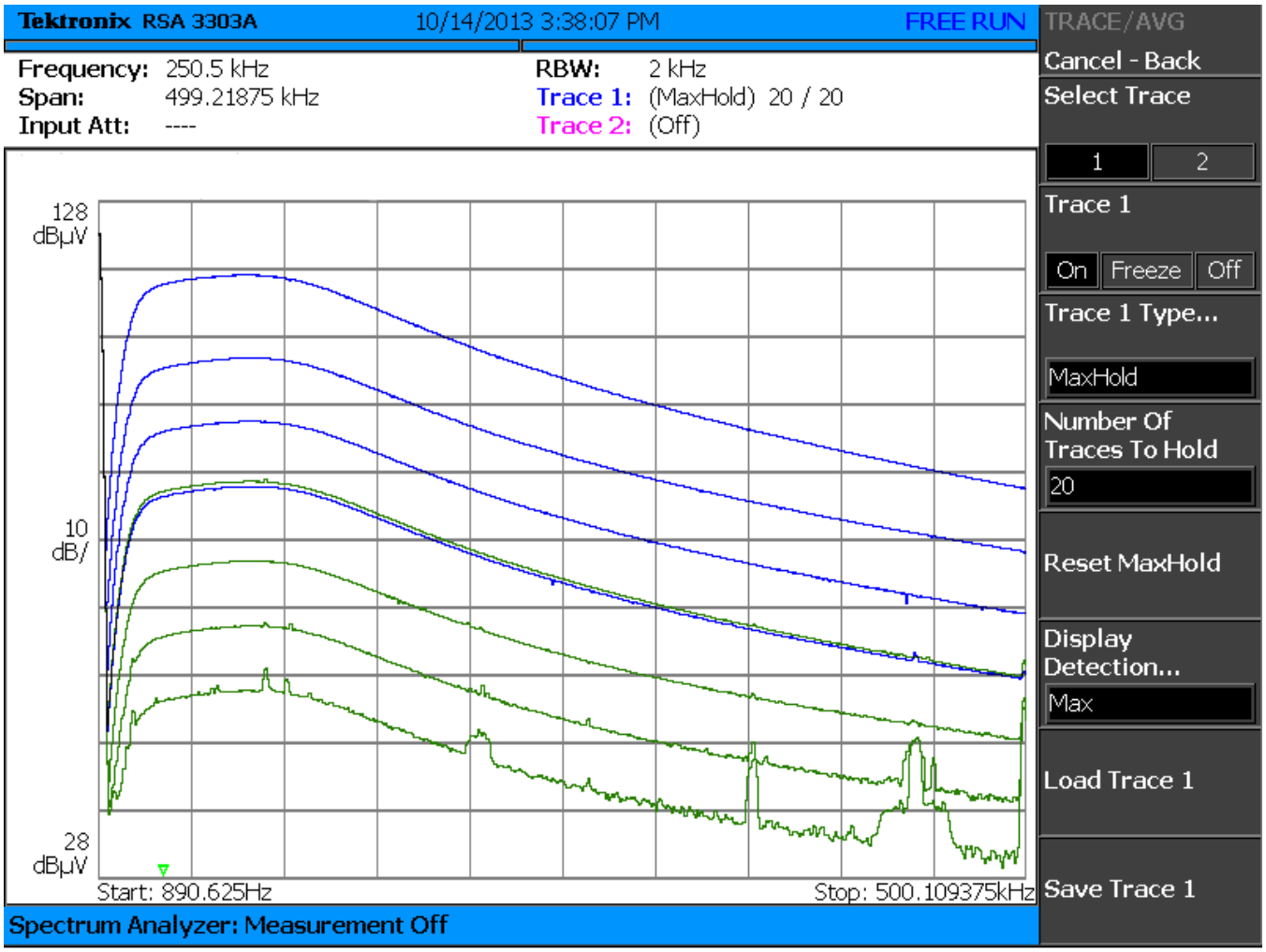


Figure 15. Receiver transfer function

5.4 Receiver harmonic distortion

The following two pictures show the spectral parameters of the receiver. The input signal is generated by the arbitrary function generator AFG3022B and injected into the mains connector J8. The spectral chart is measured at resistor R44, in fact, the input point to the ADC. There are two situations, where the lowest possible or the highest possible signal is injected into the input. The green line represents background noise, while the blue is that captured when the input signal is present.

Figure 16. Receiver harmonic distortion measurement topology

In the next figure, the blue line is measured while the input signal is applied. The green line is background noise.

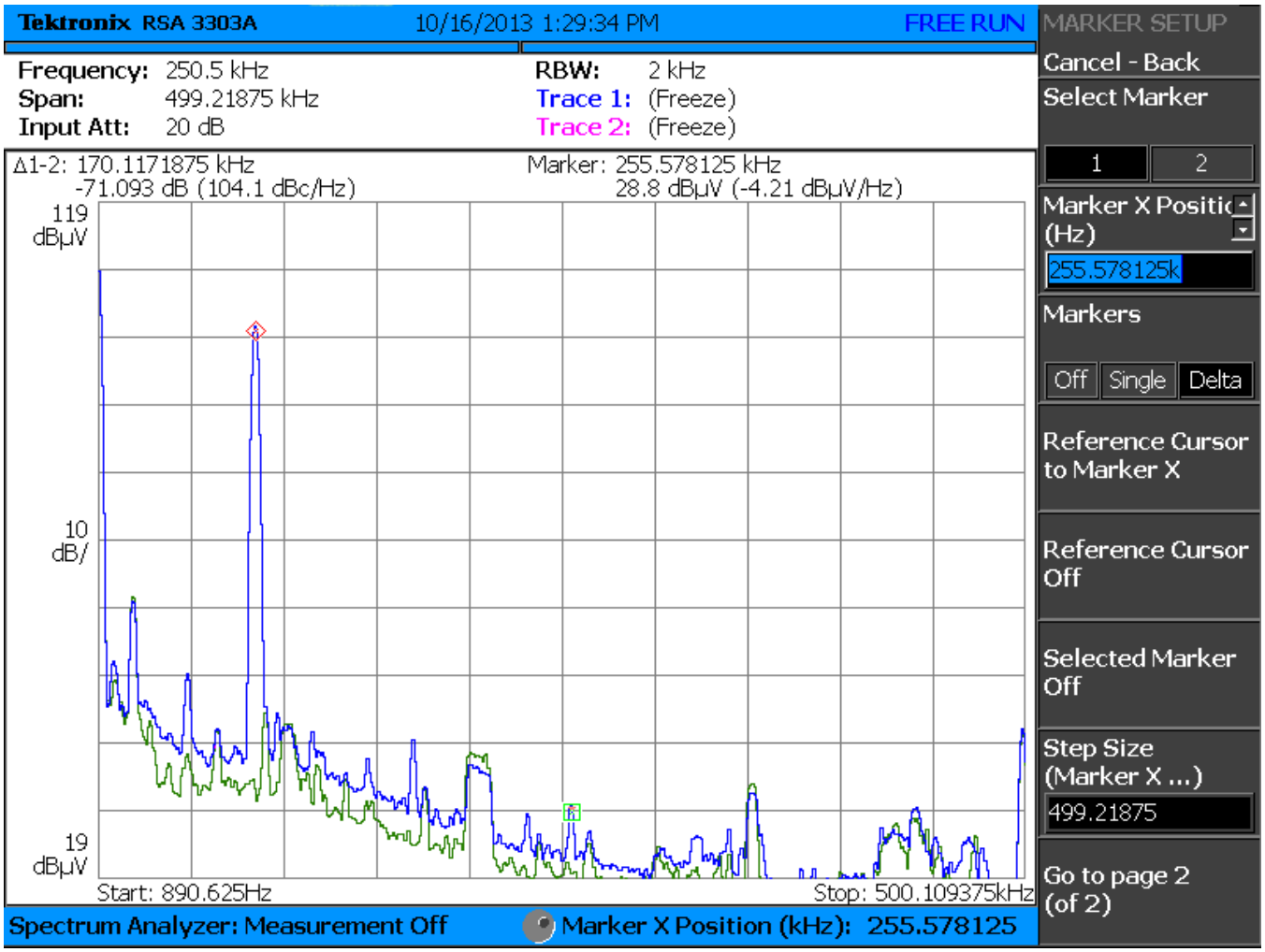


Figure 17. Input signal: 8 mV^{PP} PGA1 31.5 dB, PGA2 32 dB

In the next figure, the blue line is the input signal. The green line is background noise.

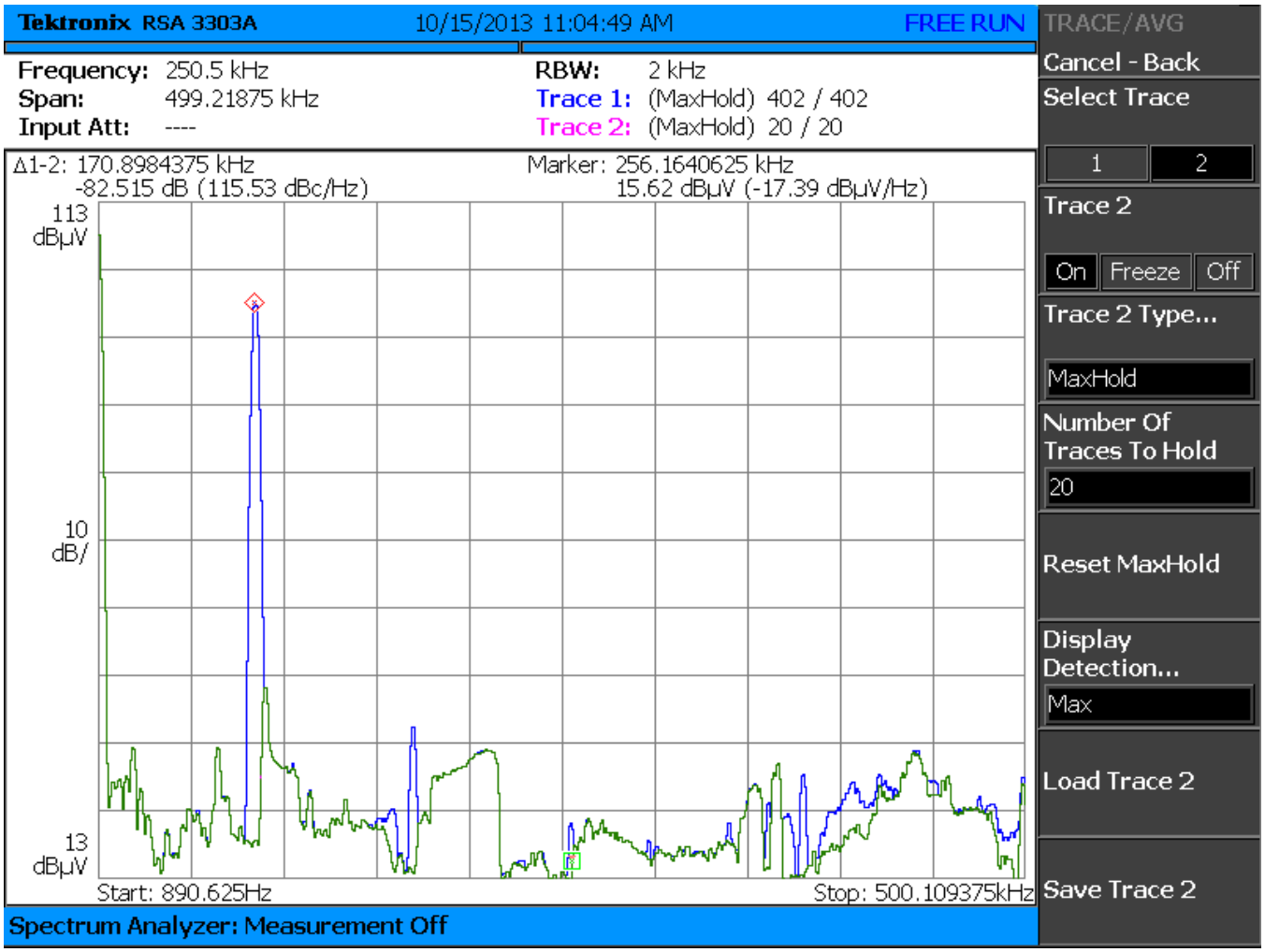


Figure 18. Input signal 10 V^{PP}, PGA1 0 dB, PGA2 0 dB

5.5 Receiver PGA gain control

The receiver uses six digital signals to control the gains of both PGA stages. The following tables show the gain control signal settings and corresponding gains.

Table 7. PGA1 control signal states and corresponding gains

PLC signal name	Tower system name	Tower edge conn. J2	State			
PLC_RXG0	SPI1_CLK	J2[B7]	1	0	0	0
PLC_RXG1	SPI1_CS0_B	J2[B9]	0	1	0	0
PLC_RXG2	SPI1_MOSI	J2[B10]	0	0	1	0
PLC_RXG3	SPI1_MISO	J2[B11]	0	0	0	1
Gain		dB	0	9.5	19	31.5

Table 8. PGA2 control signal states and corresponding gains

PLC signal name	Tower system name	Tower edge conn. J2	State	
PLC_RXG4	SPI1_TMR1	J2[A33]	1	0
PLC_RXG5	SPI1_TMR0	J2[A34]	0	1
Gain		dB	0	32

Table 9. PGAx control signal voltage levels

Digital VCC3V3 = 3.3V	Input Low max [V]	Input High min [V]
PLC_RXGx	1	2.5

Gain settling times for both PGA1 and PGA2 are fast, in the range of microseconds. The following pictures show the gain settlings for PGA1 and PGA2.

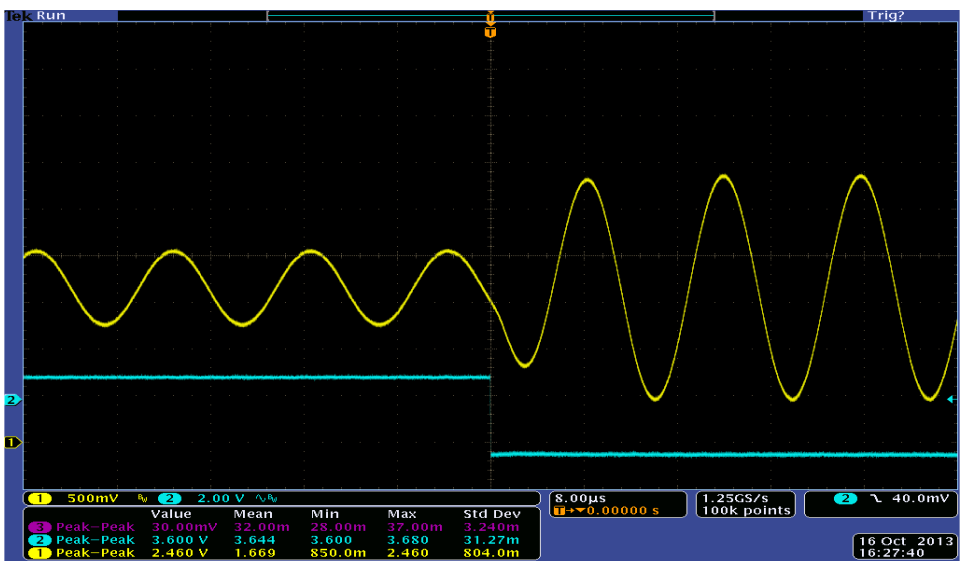


Figure 19. Rx PGA1 gain settling time (yellow trace measured on TP11) 0 dB to 9.5 dB

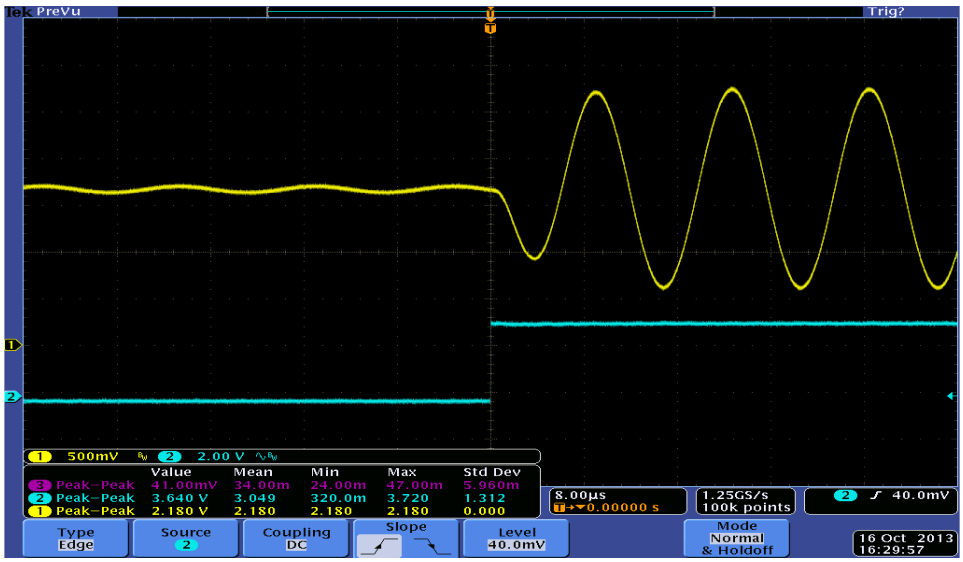


Figure 20. Rx PGA2 gain settling time (yellow trace measured on TP11) 0 dB to 32 dB

6 Zero-crossing detection

Some power line communication protocols use the mains zero-crossing event for synchronization. The MCR2 AFE offers a zero-crossing signal. The signal is opto-isolated and offers a rectangular analogue output. This signal is connected to J2[A72] and should be detected by the microcontroller internal analogue comparator.

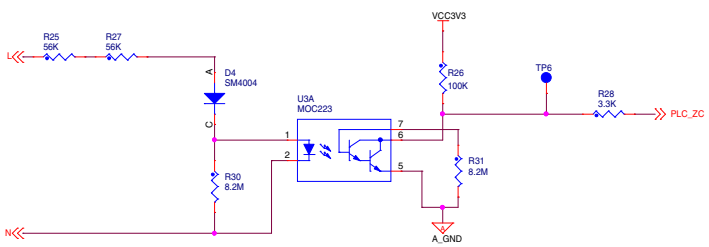


Figure 21. The mains zero-crossing detector

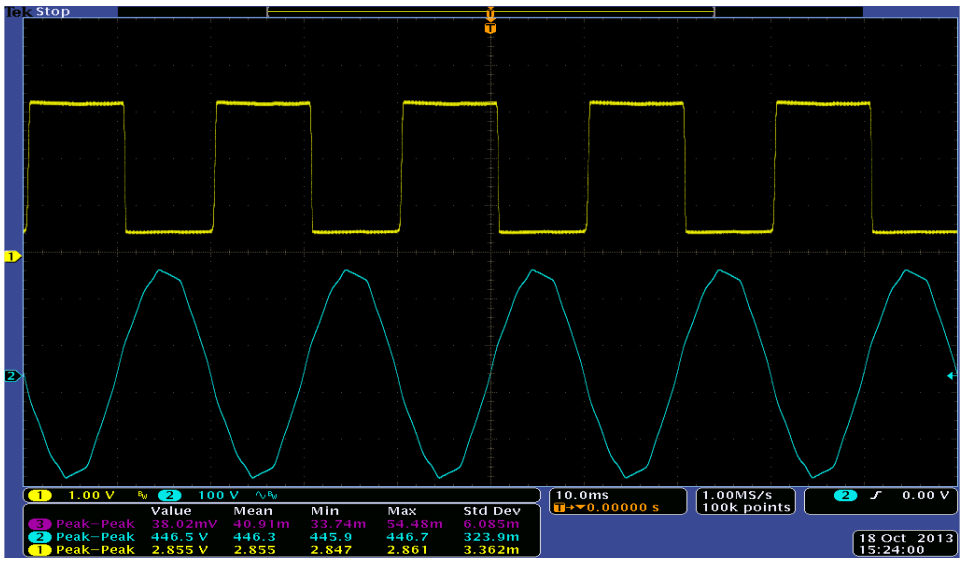


Figure 22. The zero-crossing detector output signal

7 Coupling

The coupling circuit connects the transmitter/receiver to the mains. The main purpose of the circuit is to remove the 120/230V 50Hz AC voltage to protect the low-voltage circuits of the MCR2 AFE. The C51 capacitor forms a high-pass filter and attenuates the 50Hz mains voltage. The R79 varistor protects the coupling circuit from overvoltage.

The R39 resistor is a placeholder only, for the case of narrowband modulation. In this case, there may be an inductor assembled to form a resonating circuit with C51.

The T1 transformer provides galvanic isolation of the MCR2 AFE from the mains.

The C50 capacitor removes the transmitter signal DC voltage, which would be short-cut on the transformer.

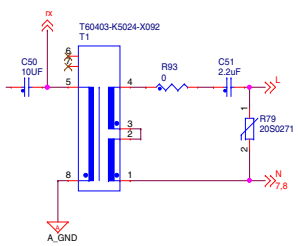


Figure 23. Coupling circuit

An impedance of the coupling and protection circuit limits the maximal current injected into the mains, provided that the maximal output voltage swing is 12V. The C50 and C51 capacitors have impedances 0.32Ohm @50kHz signal and 1.44Ohm @50kHz signal. Together with the protection circuit impedance of 0.66Ohms, the coupling path has an impedance of roughly 2.5 Ohm.

8 Communication

As mentioned at the start, the MCR2 AFE board may not be used in the tower system; it only adopts the microcontroller board, and therefore may not be connected with the tower serial board to enable communication. For communication purposes, the MCR2 AFE provides the connectivity.

The MCR2 AFE provides three communication interfaces: UART, I^2C, and SPI. In the figure below, there is a schematic of the communication connectors.

The J5 connectors are for UART1 and I^2C, and the J6 connector is for the SPI interface. The signals on those connectors are at the logic level 0 V/3.3 V.

The J4 connector provides the UART0 interface. The J4 connector is a standard Cannon type connector and the signals are RS232 level, –12/12 V compliant.

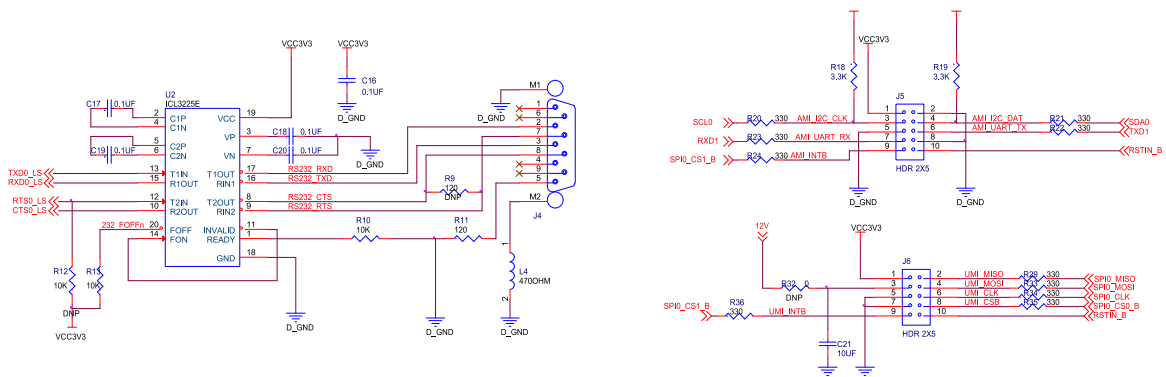


Figure 24. The communication interfaces

9 Conclusion

The MCR2 analog front end serves as a suitable development platform for power line communication. The board may be connected to an arbitrary microprocessor tower card (see www.freescale.com/tower). This gives the user freedom in selecting the microcontroller.

The MCR2 AFE is suitable for alternating high-voltage power lines (220 V AC), as well as lower voltage levels or DC power lines.

The MCR2 AFE may be used for narrow or broadband signals from 0 Hz to 500 kHz, with only a few hardware changes.

The MCR2 AFE provides transmitter/receiver amplifiers with many gain steps and filters. For alternating power buses, it provides a zero-crossing event signal. There is a 12 V to 3.3 V step-down converter which may feed the microcontroller tower card.

The MCR2 AFE allows connection of several communication interfaces – SPI, UART, and I^2C on a 3.3 V level and ±12 V UART.

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