NXP Semiconductors
Application Note

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QorIQ LS1043A Design Checklist

1 About this document

This document provides recommendations for new designs based on the LS1043A/LS1023A processor, which is a cost-effective, power-efficient, and highly integrated system-on-chip (SoC) design that extends the reach of the NXP Value Performance line of QorIQ communications processors.

This document can also be used to debug newly-designed systems by highlighting those aspects of a design that merit special attention during initial system start-up.

NOTE

This document applies to the LS1043A and LS1023A devices. For a list of functionality differences, see the appendices in *QorIQ LS1043A Reference Manual* (document LS1043ARM).

Contents

2 Before you begin

Ensure you are familiar with the following NXP collateral before proceeding:

- *QorIQ LS1043A, LS1023A Data Sheet* (document LS1043A)
- *QorIQ LS1043A Reference Manual* (document LS1043ARM)

3 Simplifying the first phase of design

Before designing a system with the chip, it is recommended that you familiarize yourself with the available documentation, software, models, and tools.

This figure shows the major functional units within the LS1043A chip.

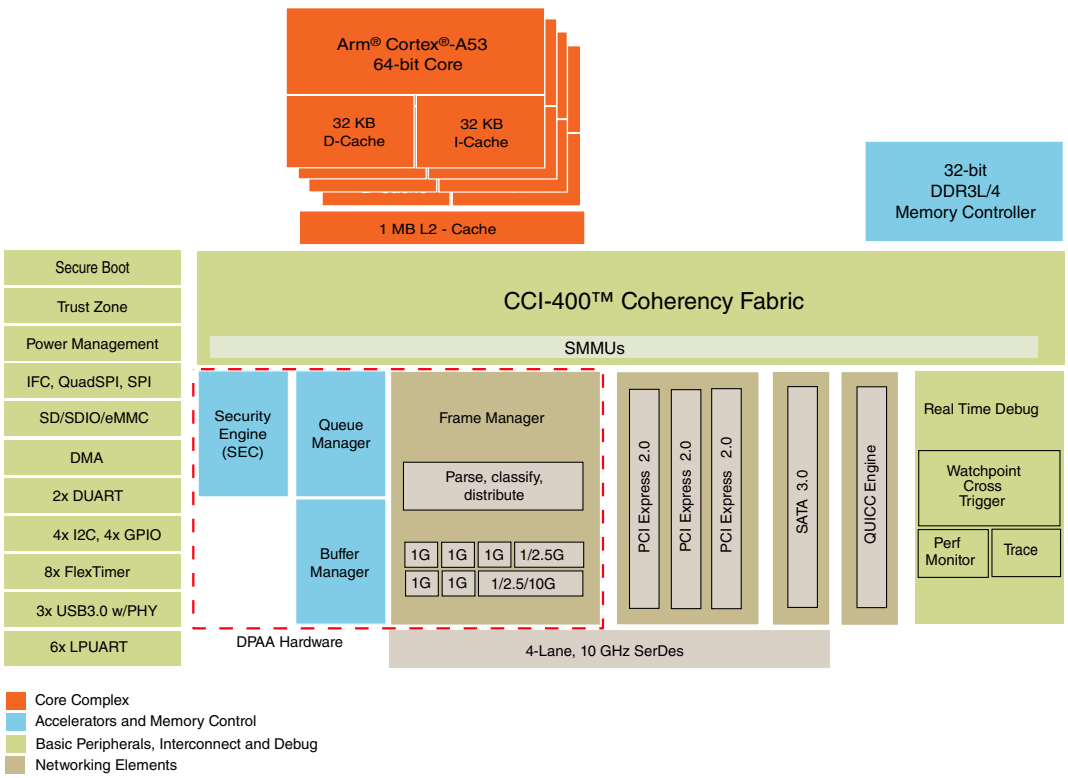


Figure 1. LS1043A block diagram

This figure shows the major functional units within the LS1023A chip.

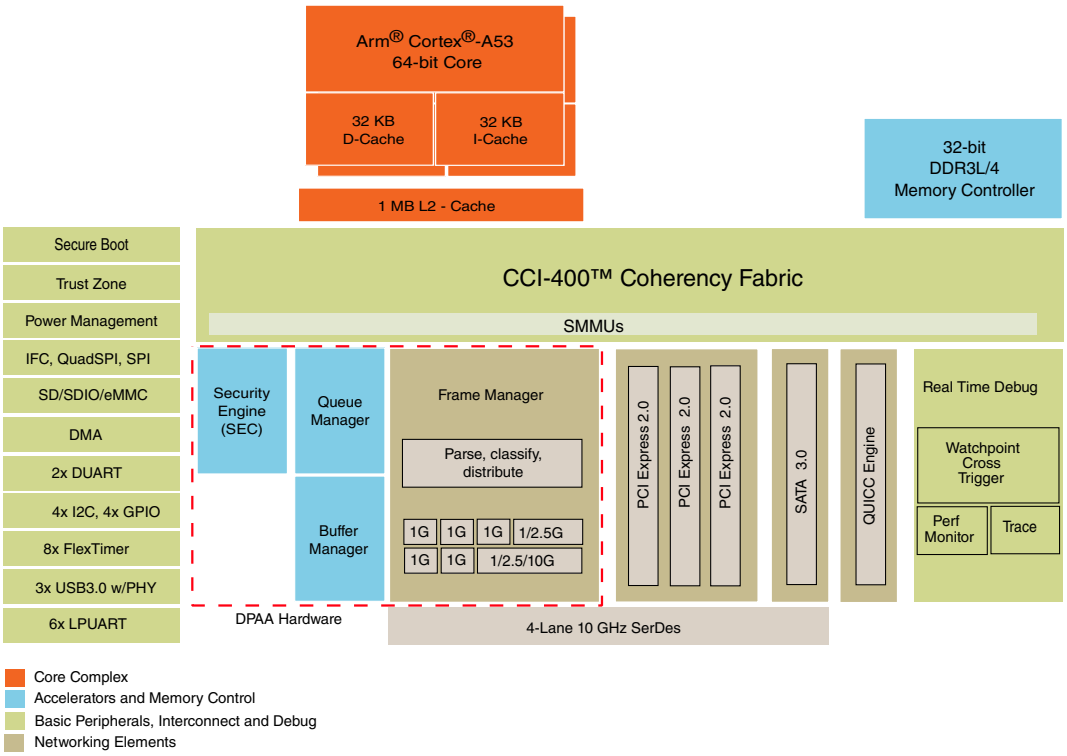


Figure 2. LS1023A block diagram

3.1 Recommended resources

This table lists helpful tools, training resources, and documentation, some of which may be available only under a non-disclosure agreement (NDA). Contact your local field applications engineer or sales representative to obtain a copy.

Table 1. Helpful tools and references

ID	Name	Location
	Related collateral	
LS1043ACE	LS1043A Chip Errata **NOTE:** This document describes the latest fixes and workarounds for the chip. It is strongly recommended that this document be thoroughly researched prior to starting a design with the chip.	Contact your NXP representative
LS1043A	*QorIQ LS1043A, LS1023A Data Sheet*	www.nxp.com
LS1043AFS	*QorIQ LS1043A and LS1023A Communication Processors - Fact Sheet*	www.nxp.com
LS1043ARM	*QorIQ LS1043A Reference Manual*	www.nxp.com
LS1043APB	*QorIQ LS1043A Product Brief*	www.nxp.com
AN5125	*Introduction to Device Trees - Application note*	
	Arm® Cortex®-A53 MPCore Processor Technical - Reference Manual Revision: r0p4	Attached with LS1043ARM
AN4871	*Assembly Handling and Thermal Solutions for Lidless Flip Chip Ball Grid Array Packages*	www.nxp.com

Table continues on the next page...

Table 1. Helpful tools and references (continued)

ID	Name	Location
AN5080	*QorIQ P1xxx series to LS1043A Migration Guide - Application Note*	Contact your NXP reprentative
AN5097	*Hardware and Layout Design Considerations for DDR4 SDRAM Memory Interfaces - Application Note*	www.nxp.com
AN4311	*SerDes Reference Clock Interfacing and HSSI Measurements Recommendations*	www.nxp.com
AN3940	*Hardware and Layout Design Considerations for DDR3 SDRAM Memory Interfaces*	www.nxp.com
Software tools		
	CodeWarrior Development Software for ARM® v8 64-bit based QorIQ LS-Series Processors	www.nxp.com
	Software Development Kit for LS1043A	www.nxp.com
Hardware tools		
	CodeWarrior TAP	www.nxp.com
	QorIQ LS Processor Probe Tips for CodeWarrior TAP	www.nxp.com
	QorIQ LS1043A reference design board	www.nxp.com
Models		
IBIS	To ensure first path success, NXP strongly recommends using the IBIS models for board-level simulations, especially for SerDes and DDR characteristics.	Contact your NXP representative
BSDL	Use the BSDL files in board verification.	Contact your NXP representative
Flotherm	Use the Flotherm model for thermal simulation. Especially without forced cooling or constant airflow, a thermal simulation should not be skipped.	Contact your NXP representative
Available training		
-	Our third-party partners are part of an extensive alliance network. More information can be found at www.NXP.com/alliances.	www.nxp.com/alliances
-	Training materials from past Smart Network Developer's Forums and NXP Technology Forums (FTF) are also available at our website. These training modules are a valuable resource for understanding the chip.	www.nxp.com/alliances

NOTE

Design requirements in the device datasheet supersede requirements mentioned in design checklist and design requirements mentioned in design checklist supersede the design/ implementation of the NXP reference design (RDB) system.

3.2 Product revisions

This table lists the System Version Register (SVR) and Arm Core main ID register (TRCIDR1) values for the various chip silicon derivatives.

Table 2. Chip product revisions (21x21 package)

Part (21x21 package)	Arm® Cortex®-A53 MPCore Processor Revision	Arm Core Main ID Register	System Version Register Value		Note
			Silicon Rev 1.0	Silicon Rev 1.1	
LS1043A	r0p4	0x4100_0404h	0x8792_0110h	0x8792_0111h	Without Security
LS1043AE	r0p4	0x4100_0404h	0x8792_0010h	0x8792_0011h	With Security
LS1023A	r0p4	0x4100_0404h	0x8792_0910hh	0x8792_0911h	Without Security
LS1023AE	r0p4	0x4100_0404h	0x8792_0810h	0x8792_0811h	With Security

Table 3. Chip product revisions (23x23 package)

Part (23x23 package)	Arm® Cortex®-A53 MPCore Processor Revision	Arm Core Main ID Register	System Version Register Value		Note
			Silicon Rev 1.0	Silicon Rev 1.1	
LS1043A	r0p4	0x4100_0404h	0x8792_0310h	0x8792_0311h	Without Security
LS1043AE	r0p4	0x4100_0404h	0x8792_0210h	0x8792_0211h	With Security
LS1023A	r0p4	0x4100_0404h	0x8792_0B10h	0x8792_0B11h	Without Security
LS1023AE	r0p4	0x4100_0404h	0x8792_0A10h	0x8792_0A11h	With Security

4 Power design recommendations

4.1 Power pin recommendations

Table 4. Power and ground pin termination checklist

Signal name	Used		Not used	Completed
AV_{DD}_CGA1	Power supply for cluster group A PLL 1 supply	1.8 V (through a filter)	Must remain powered	
AV_{DD}_CGA2	Power supply for cluster group A PLL 2 supply	1.8 V (through a filter)	Must remain powered	
AV_{DD}_D1	Power supply for DDR1 PLL	1.8 V (through a filter)	Must remain powered	
AV_{DD}_PLAT	Power supply for Platform PLL	1.8 V (through a filter)	Must remain powered	
AV_{DD}_SD1_PLL1	Power supply for SerDes1 PLL 1	1.35 V (SerDes, filtered from X1VDD)	Must remain powered (no need to filter from X1VDD)	

Table continues on the next page...

Table 4. Power and ground pin termination checklist (continued)

Signal name	Used		Not used	Completed
AV_{DD}_SD1_PLL2	Power supply for SerDes1 PLL 2	1.35 V (SerDes, filtered from X1VDD)	Must remain powered (no need to filter from X1VDD)	
V_{DD}	Core and platform supply voltage	0.9/1.0 V	Must remain powered	
$S1V_{DD}$	Core power supply for the SerDes logic transceiver	0.9/1.0 V	Must remain powered	
EV_{DD}	eSDHC[0-3]/CLK/CMD, GPIO2,LPUART2_CTS_B,LPUART2_RTS_B, LPUART3,LPUART5, LPUART6, FTM4_CH6/7,FTM4_EXTCLK/FAULT/ QD_PHA/QD_PHB	1.8/3.3 V	Must remain powered	
DV_{DD}	DUART1/2, I2C, DMA, QE, LPUART1,LPUART2_SOUT/SIN, LPUART4, GPIO1, GPIO4,GIC (IRQ 3/4/5/6/7/8/9/10), FTM 3/8, USB Control(DRVVBUS, PWRFAULT), FTM4_CH0/1/2/3/4/5	1.8/3.3 V	Must remain powered	
$G1V_{DD}$	Power supply for the DDR3L/DDR4	1.35 V for DDR3L 1.2 V for DDR4	Must remain powered	
TV_{DD}	Ethernet management interface 2 (EMI2)	1.2/1.8/2.5 V	Must remain powered	
LV_{DD}	Ethernet Interface 1/2, Ethernet management interface 1 (EMI1), TSEC_1588, GPIO1, GPIO3,FTM1/2, GIC (IRQ11)	1.8/2.5 V	Must remain powered	
OV_{DD}	IFC, SPI, GIC (IRQ 0/1/2), Temper_Detect, System control and power management, SYSCLK,DDR_CLK, DIFF_SYSCLK, GPIO2, GPIO1,eSDHC[4-7]/VS/ DAT123_DIR/ DAT0_DIR/CMD_DIR/ SYNC), Debug, SYSCLK, JTAG, RTC, FTM5/6/7,POR signals	1.8 V	Must remain powered	
X1VDD	Pad power supply for the SerDes transceiver	1.35 V	Must remain powered	

Table continues on the next page...

Table 4. Power and ground pin termination checklist (continued)

Signal name	Used		Not used	Completed
TA_PROG_SFP	SFP fuse programming override supply	Should only be supplied 1.8V during secure boot programming. For normal operation, this pin needs to be tied to GND through a 330 Ω resistor.		
PROG_MTR	This pin must be pulled to GND through a 330 Ω resistor.			
FA_VL	This pin must be pulled to GND through a 330 Ω resistor.			
TA_BB_VDD	Battery backed security monitor supply	0.9V/1.0 V	This signal should be connected to 0.9V/1.0V V_{DD} supply.	
TH_V_{DD}	Thermal monitor unit supply	1.8 V	Must remain powered	
USB_HV_{DD}[2]	USB PHY Transceiver supply	3.3 V	Tie to GND	
USB_SDV_{DD}[2]	Analog and Digital HS supply for USBPHY	0.9/1.0 V	Tie to GND	
USB_SV_{DD}[2]	Analog and Digital SS supply for USBPHY	0.9/1.0 V	Tie to GND	
SENSEVDD	V_{DD} sense pin	Connect to regulator feedback.		
GND	Core, platform and PLL ground	GND	Tie to GND	
SENSEGND	GND sense pin	Connect to regulator feedback.		
SD_GND	GND pin for SerDes and PLL supplies	GND	Tie to GND	

NOTE

1. For supported voltage/frequency options, refer to orderable part list of QorIQ LS1043A and LS1023A Multicore Communications Processors at www.nxp.com
2. If all USB power supplies are connected to GND when USB is not used, the JTAG IEEE Std 1149.1-2001 Boundary Scan Register (BSR) will not shift contents between TDI and TDO. USB_SVDD must be powered in order for the USB BSR cells to shift. In this case, the USB boundary cells cannot observe or control USB pins. This affects the USB BSR cells during EXTEST, EXTEST_PULSE, EXTEST_TRAIN, CLAMP and SAMPLE. The only fails are related to USB IO's when USB_SVDD is powered on, and USB_SDVDD and USB_HVDD are powered off. If all USB power supplies are connected to GND, the other 1149.1 JTAG or DAP debug instructions will still operate.

4.2 Power system-level recommendations

Table 5. Power design system-level checklist

Item	Completed
General	
Ensure to meet all of the requirements in the data sheet, including power sequencing, power down requirements, THERMAL and MAXIMUM power dissipation, I/O power dissipation, and power on ramp rate.	

Table continues on the next page...

Table 5. Power design system-level checklist (continued)

Item	Completed
Ensure the PLL filter circuit is applied to AV_{DD}_PLAT, AV_{DD}_CGA1, AV_{DD}_CGA2, AV_{DD}_D1. See the "PLL power supply filtering" section of this table.	
If SerDes is enabled, ensure the PLL filter circuit is applied to the respective AV_{DD}_SD1_PLL1, AV_{DD}_SD1_PLL2 pins. Otherwise, a filter is not required. Even if an entire SerDes module is not used, the power is still needed to the AV_{DD} pins. However, instead of using a filter, it needs to be connected to the XV_{DD} rail through a 0 Ω resistor. See the "PLL power supply filtering" section of this table.	
Ensure the PLL filter circuits are placed as close to the respective AV_{DD}_SD1_PLL1, AV_{DD}_SD1_PLL2 pin as possible. If possible, a small cap for the filter should be placed directly at the pin. If no small cap for the filter is available, consider at least a standard decoupling cap, such as 0.1 µF.	
General Power supply decoupling	
Because of large address and data buses and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the system, and the device itself, so this requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, TA_BB_V_{DD}, OV_{DD}, TV_{DD}, EV_{DD}, DV_{DD}, LV_{DD}, $G1V_{DD}$, $S1V_{DD}$, $X1V_{DD}$ pin of the device. These decoupling capacitors should receive their power from separate V_{DD}, TA_BB_V_{DD}, OV_{DD}, TV_{DD}, EV_{DD}, DV_{DD}, LV_{DD}, $G1V_{DD}$, $S1V_{DD}$, $X1V_{DD}$ and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part. These capacitors typically should have a value of approximately 0.1 µF. However, larger values available in the given package, such as 10 µF for 0402 (supports 1.0 mm pitched parts) or 4.7 µF for 0201 (supports 0.8 mm pitched parts), may be used to provide both decoupling and intermediate capacitance for the power supply design. For example, a system may have 0.1 µF at the pin, but also needs 22 µF intermediate capacitance outside the package. Given routing escape density, it may be more beneficial to remove the 22 µF caps and replace the 0.1 µF with 4.7 µF to 10 µF 0201/0402. Thus, it allows more room for routing to escape as an option. It is best to have one decoupling capacitor at each pin location. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes for 1 mm pitched parts and 0201 for 0.8 mm pitched parts. As presented in the "Core and platform supply voltage filtering" section of this table, it is recommended that there be several medium and large sized bulk storage capacitors distributed around the PCB, feeding the V_{DD} and other planes (for example, TV_{DD}, EV_{DD}, DV_{DD}, LV_{DD}, $G1V_{DD}$, and so on), to enable quick recharging of the smaller chip capacitors.	
Provide sufficiently-sized power planes for the respective power rail. Use separate planes if possible; split (shared) planes if necessary. If split planes are used, ensure that signals on adjacent layers do not cross splits. Avoid splitting ground planes at all costs.	
Ensure the bulk capacitors have a low ESR rating to ensure the quick response time necessary.	
Ensure the bulk capacitors are connected to the power and ground planes through two vias, as necessary, to minimize inductance.	
Ensure you work directly with your power regulator vendor for best values and types of bulk capacitors. The capacitors need to be selected to work well with the power supply to be able to handle the chip's power requirements. Most regulators perform best with a mix of ceramic and other low ESR types, such as OSCON, POS, and other types of capacitor technologies.	
Core and platform supply voltage filtering	
The V_{DD} supply is normally derived from a high current switching power supply, which can regulate its output voltage very accurately despite changes in current demand from the chip within the regulator's relatively low bandwidth. Several bulk capacitors must be distributed around the PCB to supply transient current demand above the bandwidth of the voltage regulator. Bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the necessary response time. They should also be connected to the power and ground planes through two vias at each side, if necessary, to minimize inductance. However, customers should work directly with their power	

Table continues on the next page...

Table 5. Power design system-level checklist (continued)

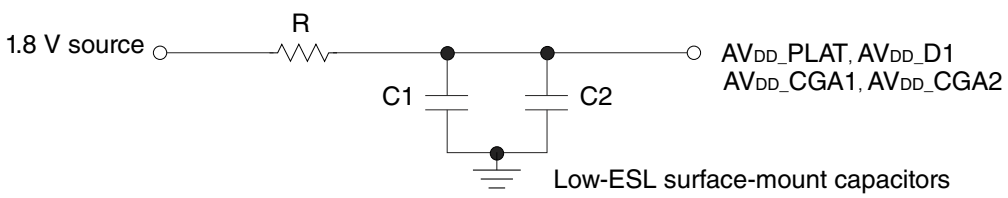
Item	Completed
regulator vendor for best values and types of bulk capacitors. Most power supply designs work well with small ceramic caps at each pin, as discussed in the "General power supply decoupling" section of this table. But also nearby the SoC should be intermediate caps, such as 22 µF ceramic and larger 330 to 560 µF POS type caps, as an example. As a guideline for customers and their power regulator vendors, NXP recommends that these bulk capacitors should be chosen to maintain the positive transient power surges to less than V_{DD} + 50 mV (negative transient undershoot should comply with specification of VDD - 30 mV) for current steps of up to 50% to 100% rise and 100% to 50% of max current (based on maximum power in the datasheet) with a slew rate of 7 A/us. These bulk decoupling capacitors will ideally supply a stable voltage for current transients into the MHz range. See the "General power supply decoupling" section of this table for further decoupling recommendations.	
PLL supply filtering (core, platform, DDR, filtered from 1.8 V source)	
All PLLs are provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CGA1/2, and AV_{DD}_D1 voltages must be derived directly from a 1.8 V voltage source, such as OV_{DD}, through a low frequency filter. The recommended solution for this type of PLL filtering is to provide independent filter circuits per PLL power supply, one for each of the AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced. This circuit is intended to filter noise in the PLL's resonant frequency range from a 500 kHz to 10 MHz range. Provide independent filter circuits per PLL power supply, as illustrated in the following figure. Where • R = 5 Ω ± 5% • C1 = 10 µF ± 10%, 0603 or smaller, X5R or better (X7R or C0G are fine), with ESL ≤ 0.5 nH • C2 = 1.0 µF ± 10%, 0402 or 0201, X5R, with ESL ≤ 0.5 nH • Low-ESL surface-mount capacitors  Note the following: • Each AV_{DD} pin must have its own independent filter circuit. • Voltage for AV_{DD} is defined at the input of the PLL supply filter and not the pin of AV_{DD}. • If done properly, it is possible to route directly from the capacitors to the AV_{DD} pins, without the added inductance of vias. • It is recommended that an area fill or power plane split be provided for a low-impedance profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. • Placement should be such that the smaller capacitors are nearest to the AV_{DD} pin. If routing permits, the smallest cap would be best located at the pin of AV_{DD}. • **Caution:** These filters are a necessary extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the user's risk.	
PLL supply filtering (SerDes, filtered from X1V_{DD})	
The AV_{DD}_SD1_PLL1/2 signals provide power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, ensure the power supplied to the PLL is filtered using a circuit similar to the one shown in the following figure. The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, one for each side of the AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced.	

Table continues on the next page...

Table 5. Power design system-level checklist (continued)

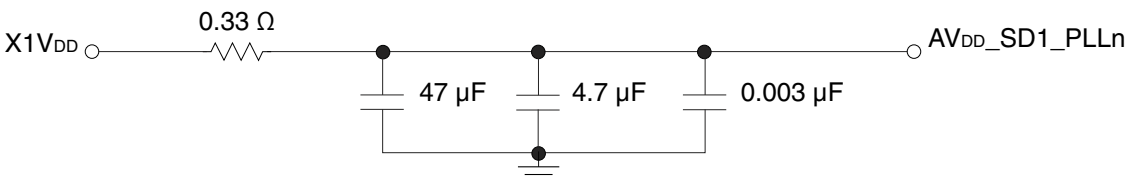
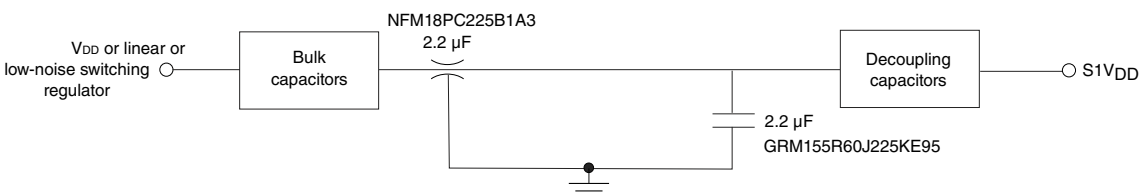
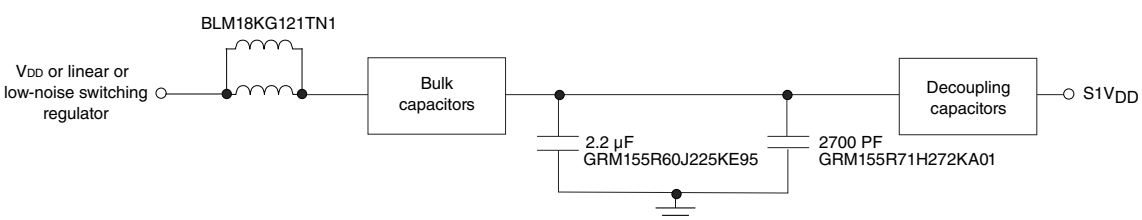
Item	Completed
Note the following: • Each AV_{DD} must have its own independent filter circuit. • AV_{DD}_SD1_PLL*n* should be a filtered version of $X1V_{DD}$. • Voltage for AV_{DD} is defined at the pin of AV_{DD}. This is in contrast to the requirement, for example for the core PLL filter such as AV_{DD}_CGA*n*, which is measured at the input of the filter. • Placement should be such that the smaller capacitors are nearest to the AV_{DD} pin. If routing permits, the smallest cap would be best located at the pin of AV_{DD}. • It is recommended that an area fill or power plane split be provided for a low-impedance profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • A 47 µF 0805 XR5 or XR7, 4.7 µF 0603 or smaller, and 0.0033 µF 0402 or 0.0033 µF 0201 capacitor are recommended. The size and material type are important. A 0.33 Ω ± 1% resistor is recommended. • **Caution**: These filters are a necessary extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the user's risk. 	
SerDes power supply filtering	
The ferrite beads should be placed in parallel to reduce voltage droop. For the linear or low-noise switching regulator, 10 mVp-p, 50 kHz to 500 MHz is the noise goal. All traces should be kept short, wide, and direct. Use small area fill, if possible. The goal is to lower the impedance of this net, thus lowering the noise. $S1V_{DD}$ may be supplied by linear or low noise switching regulator or sourced by a filtered V_{DD}. Two example solutions for $S1V_{DD}$ filtering, where $S1V_{DD}$ is sourced from V_{DD}, linear or low noise switching regulator, are illustrated in Figure 3 and Figure 4. Users can choose either one as they see best fit their needs, but the primary NFM type filter has two advantages: lower DC droop and easier layout than the ferrite bead solution.  **Figure 3. Primary $S1V_{DD}$ power supply filter circuit**  **Figure 4. Alternate $S1V_{DD}$ power supply filter circuit**	

Table continues on the next page...

Table 5. Power design system-level checklist (continued)

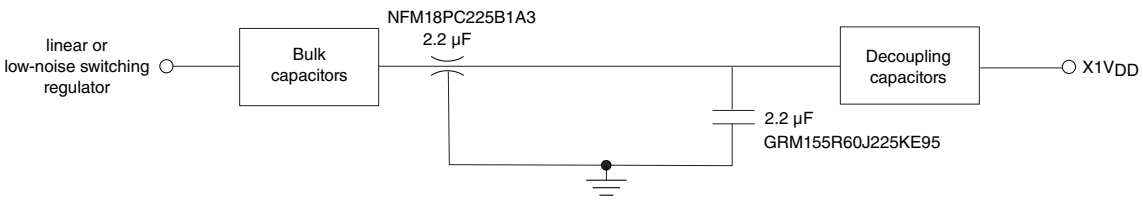
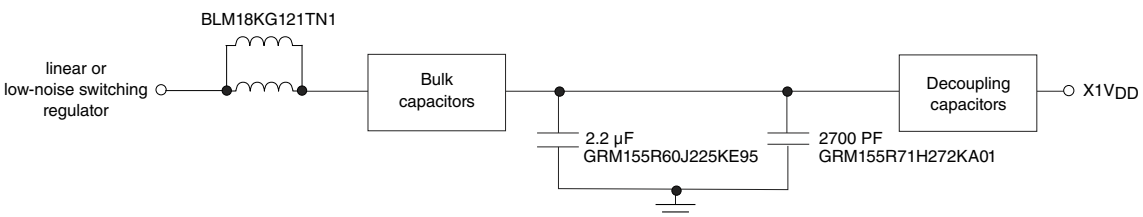
Item	Completed
Note the following: • See "Power-on ramp rate," in the data sheet for maximum $S1V_{DD}$ power-up ramp rate. • It is recommended that an area fill or power plane split be provided for a low-impedence profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific set of pins being supplied to minimize noise coupled from nearby circuits. • Located at each pin should have a decouple capacitor, such as 0.1 µF.	
$X1V_{DD}$ may be supplied by a linear or low noise switching regulator or sourced by a filtered $G1V_{DD}$. Two example solutions for $X1V_{DD}$ filtering, where $X1V_{DD}$ is sourced from a linear or low noise switching regulator, are illustrated in Figure 5 and Figure 6. Users can choose either one as they see best fit their needs, but the primary NFM type filter has two advantages: lower DC droop and easier layout than the ferrite bead solution  **Figure 5. Primary $X1V_{DD}$ power supply filter circuit**  **Figure 6. Alternte $X1V_{DD}$ power supply filter circuit** Note the following: • See "Power-on ramp rate," in the data sheet for maximum $X1V_{DD}$ power-up ramp rate. • It is recommended that an area fill or power plane split be provided for a low-impedance profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific set of pins being supplied to minimize noise coupled from nearby circuits. • Located at each pin should have a decouple capacitor, such as 0.1 µF.	
USB_HV_{DD} may be supplied by a linear or low noise switching regulator, which may be the system-wide 3.3 V power supply. Two example solutions for USB_HV_{DD} filtering, where USB_HV_{DD} is sourced from a linear or low noise switching regulator, are illustrated in Figure 7 and Figure 8. Users can choose either one as they see best fit their needs, but the primary NFM type filter has two advantages: lower DC droop and easier layout than the ferrite bead solution.	

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Table 5. Power design system-level checklist (continued)

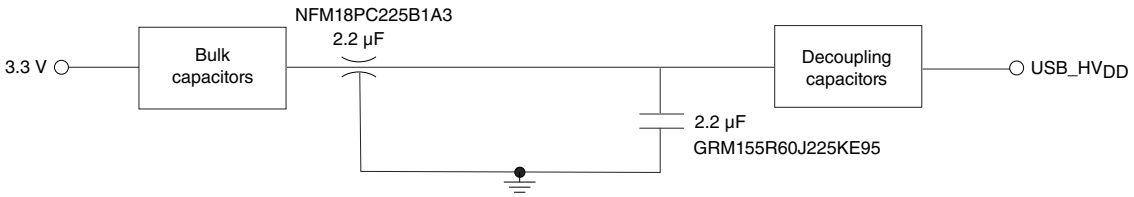
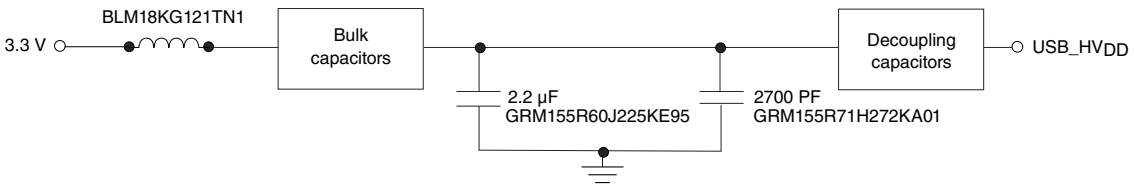
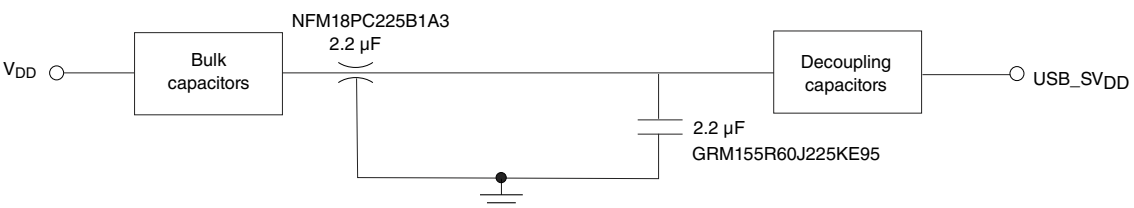
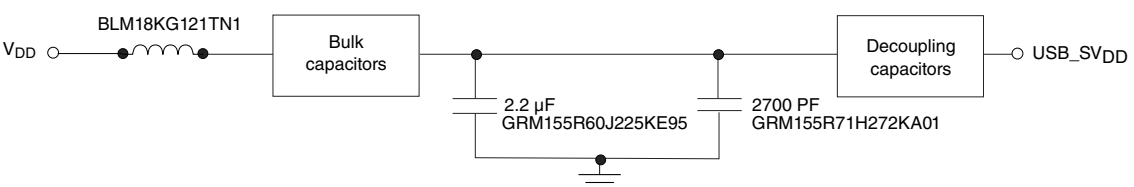
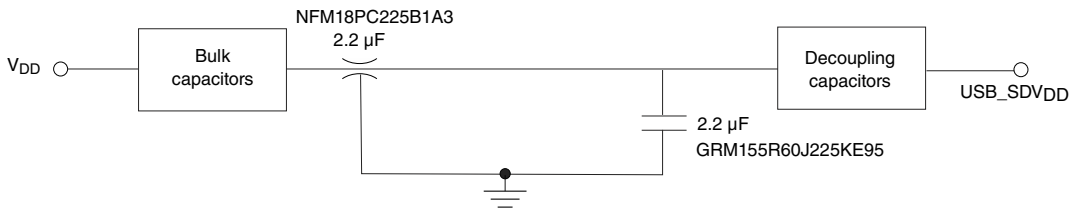
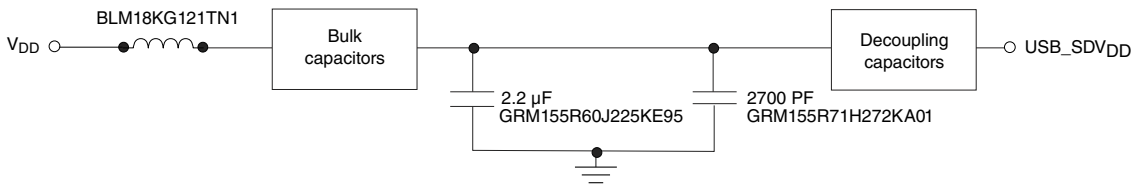
Item	Completed
 **Figure 7. Primary USB_HV$_{DD}$ power supply filter circuit**  **Figure 8. Alternate USB_HV$_{DD}$ power supply filter circuit** Note the following: • It is recommended that an area fill or power plane split be provided for a low-impedence profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific set of pins being supplied to minimize noise coupled from nearby circuits. • Located at each pin should have a decouple capacitor, such as 0.1 µF.	
USB_SV$_{DD}$ and USB_SDV$_{DD}$ are to be filtered from the V$_{DD}$ power supply. Two example solutions for USB_SV$_{DD}$ and USB_SDV$_{DD}$ filtering, where USB_SV$_{DD}$ and USB_SDV$_{DD}$ are sourced from a filtered version of V$_{DD}$, are illustrated in Figure 9, Figure 10, Figure 11 and Figure 12. Users can choose either one as they see best fit their needs, but the primary NFM type filter has two advantages: lower DC droop and easier layout than the ferrite bead solution.  **Figure 9. Primary USB_SV$_{DD}$ power supply filter circuit**  **Figure 10. Alternate USB_SV$_{DD}$ power supply filter circuit**	

Table 5. Power design system-level checklist

Item	Completed
 **Figure 11. Primary USB_SDV_{DD} power supply filter circuit**  **Figure 12. Alternate USB_SDV_{DD} power supply filter circuit** Note the following: • It is recommended that an area fill or power plane split be provided for a low-impedence profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific set of pins being supplied to minimize noise coupled from nearby circuits. • Located at each pin should have a decouple capacitor, such as 0.1 µF.	

4.3 Power-on reset recommendations

Various chip functions are initialized by sampling certain signals during the assertion of PORESET_B. These power-on reset (POR) inputs are pulled either high or low during this period. While these pins are generally output pins during normal operation, they are treated as inputs while PORESET_B is asserted. When PORESET_B de-asserts, the configuration pins are sampled and latched into registers, and the pins then take on their normal output circuit characteristics.

Table 6. Power-on reset system-level checklist

Item	Completed
Ensure PORESET_B is asserted for a minimum of 1 ms after V_{DD} ramps up.	
Ensure HRESET_B is asserted for a minimum of 32 SYSCLK cycles.	
In cases where a configuration pin has no default, use a 4.7 kΩ pull-up or pull-down resistor for appropriate configuration of the pin.	
Optional: An alternative to using pull-up and pull-down resistors to configure the POR pins is to use a PLD or similar device that drives the configuration signals to the chip when PORESET_B is asserted. The PLD must begin to drive these signals at least four SYSCLK cycles prior to the de-assertion of PORESET_B (other than cfg_eng_use0), hold their values for at least two SYSCLK cycles after the de-assertion of PORESET_B, and then release the pins to high impedance afterward for normal device operation **NOTE:** See the applicable chip data sheet for details about reset initialization timing specifications.	

Table continues on the next page...

Table 6. Power-on reset system-level checklist (continued)

Item	Completed
Configuration settings	
Ensure the settings in Configuration signals sampled at reset are selected properly. **NOTE:** See the applicable chip reference manual for a more detailed description of each configuration option.	
Power sequencing	
The chip requires that its power rails be applied in a specific sequence in order to ensure proper device operation. For details, see *QorIQ LS1043A, LS1023A Data Sheet*" (document LS1043A).	

4.3.1 Configuration signals sampled at reset

The signals that serve alternate functions as configuration input signals during system reset are summarized in this table.

Reset configuration signals are sampled at the negation of PORESET_B. However, there is a setup and hold time for these signals relative to the rising edge of PORESET_B, as described in the QorlQ LS1043A Data Sheet (document LS1043A).

The reset configuration signals are multiplexed with other functional signals. The values on these signals during reset are interpreted to be logic one or zero, regardless of whether the functional signal name is defined as active-low. The reset configuration signals have internal pull-up resistors so that if the signals are not driven, the default value is high (a one), as shown in the table below. Some signals must be driven high or low during the reset period. For details about all the signals that require external pull-up resistors, see the applicable device data sheet.

Table 7. LS1043A reset configuration signals

Configuration Type	Functional Pins	Comments
Reset configuration word (RCW) source inputs cfg_rcw_src[0:8]	IFC_AD[8:15] IFC_CLE	They must be set to one of the valid RCW source input option. The 512-bit RCW word has all the necessary configuration information for the chip. If there is no valid RCW in the external memory, it can be programmed using the Code Warrior or other programmer. The JTAG configuration files (path: CWInstallDir \CW4NET_v2019.01\CW_ARMv8\Config \boards) can be used in the following situations: • target boards that do not have RCW already programmed • new board bring up • recovering boards with blank or damaged flash
IFC external transceiver enable polarity select (cfg_ifc_te)	IFC_TE	Default is "1"
DRAM type select (cfg_dram_type)	IFC_A[21]	Default is DDR3L. This reset configutation pin selects the proper I/O voltage: • 0=DDR3L 1.35 V • 1=DDR4 1.2 V Ensure the selection value that matches the DDR type used on board.

Table continues on the next page...

Table 7. LS1043A reset configuration signals (continued)

Configuration Type	Functional Pins	Comments
General-purpose input (cfg_gpinput[0:7])	IFC_AD[0:7]	Default "1111 1111", values can be application defined
"Single Oscillator Source" clock select. This field selects between SYSCLK (Single ended) and DIFF_SYSCLK/ DIFF_SYSCLK_B (differential) inputs. (cfg_eng_use0)	IFC_WE0_B	• 0=DIFF_SYSCLK/ DIFF_SYSCLK_B(differential) • 1=SYSCLK (single ended) Default selection is single ended SYSCLK; "1"
"Single Oscillator Source" clock. This field indicates whether on-chip LVDS termination for differential clock is enabled or disabled. configuration (cfg_eng_use1)	IFC_OE_B	• 0=Disabled (MUST make sure that External termination pads of DIFF_SYSCLK/DIFF_SYSCLK_B have proper termination) • 1 = Enabled (default) Default is "1". It is recommened to keep provision for optional pull-down resistor on board.
"Single Oscillator Source" clock configuration (cfg_eng_use2)	IFC_WP0_B	Default is "1". Reserved.

4.3.2 Hard-Coded RCW

The hard-coded RCW can be used as an alternative method for initial board bring-up when there is no valid RCW in the external memory. .

If a new board is using a blank flash and flash is the source of RCW, then all 0xff value from flash for RCW will put the device in an unknown state.

There are two methods to workaround this problem:

1. Put switches on cfg_rcw_src signals to select hard-coded RCW(0x9A, 0x9E, 0x9F)[2].

2. Use CodeWarrior tool from NXP to override RCW.

NOTE

1. It is recommended to disconnect RESET_REQ_B from PORESET_B when using Hard-Coded RCW as any different board configuration may push the chip into an endless reset loop. For more information, refer to Hard-coded RCW options *QorIQ LS1043A Reference Manual* (document LS1043ARM).
2. Use 0x9A or 0x9E hard-coded RCW option when external DDR clock (DDRCLK) provides the reference clock to the DDR PLL. Use 0x9F hard-coded RCW option when using DIFF_SYSCLK/DIFF_SYSCLK_B as reference clock to the DDR PLL.
3. For bringing-up a new board when no valid RCW or bootloader is available and onboard flash is not supported in CodeWarrior then refer to AN12081.

5 Interface recommendations

This section details the pin termination guidelines for different interfaces. In general, any unused input pin should be terminated by a pull down unless recommended otherwise.

5.1 DDR controller recommendations

The LS1043A/LS1023A chip supports the DDR3L (1.35 V) and DDR4 (1.2 V) SDRAM memories.

The memory interface controls main memory accesses. The interface supports 32-bit data access.

5.1.1 DDR4 and DDR3L SDRAM interface pin termination recommendations

Table 8. DDR4 and DDR3L SDRAM interface pin termination checklist

Signal name[1]		I/O type	Used	Not used	Completed
DDR3L signal	DDR4 signal[2]				
D1_MA[0:13] D1_MA[14] D1_MA[15]	D1_MA[0:13] D1_MBG1 D1_MACT_B	O	Must be properly terminated to VTT	These pins can be left unconnected.	
D1_MBA[0:1] D1_MBA[2]	D1_MBA[0:1] D1_MBG0	O	Must be properly terminated to VTT	These pins can be left unconnected.	
D1_MCK[0:1]/D1_MCK[0:1]_B		O	These pins must be properly terminated.	All unused MCK pins should be disabled via the DCFG_CCSR_DDRCLKDR register.	
D1_MCKE[0:1]		O	Must be properly terminated to VTT These pins are actively driven during reset instead of being released to high impedance.	These pins can be left unconnected.	
D1_MCS[0:3]_B		O	Must be properly terminated to VTT	These pins can be left unconnected.	
D1_MDIC[0:1]		I/O	• These pins are used for automatic calibration of the DDR3L/DDR4 IOs. The MDIC[0:1] pins must be connected to 162 Ω precision 1% resistors. • MDIC[0] is grounded through a 162 Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through a 162 Ω precision 1% resistor.	These pins can be left unconnected.	

Table continues on the next page...

Table 8. DDR4 and DDR3L SDRAM interface pin termination checklist (continued)

Signal name[1]		I/O type	Used	Not used	Completed
DDR3L signal	DDR4 signal[2]				
			• For either full- or half-driver strength calibration of DDR IOs, use the same MDIC resistor value of 162 Ω. • The memory controller register setting can be used to determine if automatic calibration is done to full- or half-drive strength.		
D1_MDM[0:3], D1_MDM[8]		O	-	These pins can be left unconnected.	
D1_MDQ[0:32][3]		I/O	-	These pins can be left unconnected.	
D1_MDQS[0:3]/D1_MDQS[0:3]_B, D1_MDQS[8]/D1_MDQS[8]_B		I/O	-	These pins can be left unconnected.	
D1_MECC[0:3]		I/O	-	These pins can be left unconnected.	
D1_MAPAR_ERR_B	D1_MALERT_B	I	Recommend that a weak pull-up resistor (2-10 kΩ) for SDRAM DDR4/DDR3L to $G1V_{DD}$. When using discrete DRAM, the MALERT_B pin needs a strong pull-up resistor (50-100 Ω) to $G1V_{DD}$.	This pin should be pulled up to $G1V_{DD}$.	
D1_MAPAR_OUT		O	-	This pin can be left unconnected.	
D1_MODT[0:1]		O	Ensure the MODT signals are connected correctly. Two dual ranked DIMMs topology is not supported on LS1043A. For a single, dual-ranked DIMM, consider the following connections • MODT(0), MCS(0), MCKE(0) • MODT(1), MCS(1), MCKE(1) For quad-ranked DIMMS, it is recommended to obtain a data sheet from the memory supplier to confirm required signals. But in general, each controller needs MCS(0:3), MODT(0:1), and MCKE(0:1) connected to the one quad-ranked DIMM.	These pins can be left unconnected.	

Table continues on the next page...

Table 8. DDR4 and DDR3L SDRAM interface pin termination checklist (continued)

Signal name[1]		I/O type	Used	Not used	Completed
DDR3L signal	DDR4 signal[2]				
			These pins are actively driven during reset instead of being released to high impedance.		
D1_MRAS_B		O	Must be properly terminated to VTT	This pin can be left unconnected.	
D1_MCAS_B		O	Must be properly terminated to VTT	This pin can be left unconnected.	
D1_MWE_B		O	Must be properly terminated to VTT	This pin can be left unconnected.	
D1_MVREF	DDR4 Vref is provided internally, the external vref signal needs to be grounded when using DDR4 SDRAM	IO	DDR reference voltage: 0.49 x $G1V_{DD}$ to 0.51 x $G1V_{DD}$. • D1_MVREF can be generated using a divider from $G1V_{DD}$ as MVREF. • Another option is to use supplies that generate $G1V_{DD}$, VTT, and D1_MVREF voltage. These methods help to reduce differences between $G1V_{DD}$ and MVREF. D1_MVREF generated from a separate regulator is not recommended, because D1_MVREF does not track $G1V_{DD}$ as closely.	This pin must be connected to GND.	

NOTE

1. DDR3L signals are muxed with DDR4 signals.
2. For DDR4, bit and byte swapping rules and layout guidelines, see the application note *Hardware and Layout Design Considerations for DDR4 SDRAM Memory Interfaces* (document AN5097).
3. When DDR4 Discrete DRAM is soldered on the board, and two chip selects are used, and the second chip select is bit swizzling (meaning bits mapping from CS0 is additionally swapped in CS1 by swapping DQ0 with DQ1, DQ2 with DQ3, DQ4 with DQ5, and DQ6 with DQ7). Then bit map orders of 0x10 (2 1 3 0) and 0x30 (6 5 7 4) are not allowed.

5.1.2 DDR system-level recommendations

Table 9. DDR system-level checklist

Item	Completed
General	

Table continues on the next page...

Table 9. DDR system-level checklist (continued)

Item	Completed
DDR3L /DDR4 mode selection is through por-config signal cfg_dram_type. Ensure that the pin is configured correctly as per the DDR mode. Setting DDR4 mode while applying GVdd=1.35 V can lead to damage of IO's.	
Data Bus inversion (DBI) signals are muxed on Data Mask (D1_MDM) signals and are optional function for DDR4. Only one function can be used at a time.	
PORESET_B assertion should also reset SDRAM Memory.	
CKE termination requirment during self refresh - In order to keep DRAM memory in a self-refresh mode, the CKE signal must be driven low. For applications requiring LS1043A to be powered off and SDRAM memory in self refresh, the CKE signal must be driven/pulled low during power ramp up, external to the SoC by hardware on the board. Refer *Achieving Persistent DRAM on PowerQUICC III and QorIQ Processors* (document AN4531).	

NOTE

1. Stacked memory for DDR4 are not supported
2. DDR3L and DDR4 RDIMMs are not supported.
3. For devices with four ECC pins, ensure to connect one of the ECC pins to the Prime DQ of ECC DRAM.

5.2 IFC pin termination recommendations

Table 10. IFC pin termination checklist

Signal name	I/O type	Used	Not used	Completed
IFC_A[16:20]	O	These pins must not be pulled down during power-on reset. It may be pulled up, driven high, or if there are no externally connected devices, left in tristate. If these pins are connected to a device that pulls down during reset, an external pull-up is required to drive these pins to a safe state during reset.		
IFC_A[21]	O	This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. The pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_A[22:27]	I/O	Connect as needed.	These pins can be left unconnected.	
IFC_AD[0:15]	I/O	These pins are reset configuration pins. They have a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. These pull-ups are designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_PAR[0:1]	I/O	Connect as needed.	These pins can be left unconnected.	
IFC_CS[0:3]_B	O	Recommend weak pull-up resistors (2–10 kΩ) be placed	These pins can be left unconnected.	

Table continues on the next page...

Table 10. IFC pin termination checklist (continued)

Signal name	I/O type	Used	Not used	Completed
		on these pins to OV_{DD}.		
IFC_WE[0]_B	O	These pins are reset configuration pins, they have a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. The internal pull-ups are designed such that it can be overpowered by an external 4.7 kΩ resistor. However, It is recommended to keep a provision for optional pull-up and pull-down resistor on board.		
IFC_OE_B	O			
IFC_WP[0]_B	O			
IFC_PERR_B	I	Connect as needed.	This pin should be pulled high through a 2-10 kΩ resistor to OV_{DD} or can be left floating if configured as GPIO output	
IFC_BCTL	O	Connect as needed.	This pin can be left unconnected.	
IFC_TE	O	This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_NDDQS	I/O	Connect as needed.	This pin can be left unconnected.	
IFC_AVD	O	This pin must not be pulled down during power-on reset. It may be pulled up, driven high, or if there are no externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.		
IFC_CLE	O	This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_RB[0:3]_B	I	These pins should be pulled high through a 1 kΩ resistor to OV_{DD}.	These pins should be pulled high through a 1 kΩ resistor.	
IFC_CLK[0:1]	O	Connect as needed.	This pin can be left unconnected.	
IFC_NDDDR_CLK	O	Connect as needed	This pin can be left unconnected.	

NOTE

The IFC interface is on OVDD power domain which is 1.8 V only.

For functional connection diagram, see the chip reference manual.

5.3 DUART pin termination recommendations

Table 11. DUART pin termination checklist

Signal name	I/O type	Used	Not used	Completed
UART1_SOUT	O	The functionality of these pins is determined by the UART_BASE and UART_EXT fields in the reset configuration word (RCW[UART_BASE], RCW[UART_EXT]).	These pins can be left unconnected.	
UART1_RTS_B	O			
UART1_SIN	I		These pins should be pulled high through a 2-10 kΩ resistor to DV_{DD} or else programmed as GPIO and output.	
UART1_CTS_B	I			
UART2_SOUT	O		These pins can be left unconnected.	
UART2_RTS_B	O			
UART2_SIN	I		These pins should be pulled high through a 2-10 kΩ resistor to DV_{DD} or else programmed as GPIO and output.	
UART2_CTS_B	I			
UART3_SOUT	O		This pin can be left unconnected.	
UART3_SIN	I		This pin should be pulled high through a 2-10 kΩ resistor to DV_{DD} or else programmed as GPIO and output.	
UART4_SOUT	O		This pin can be left unconnected.	
UART4_SIN	I		This pin should be pulled high through a 2-10 kΩ resistor to DV_{DD} or else programmed as GPIO and output.	

5.4 LPUART pin termination recommendations

Table 12. LPUART pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
LPUART1_CTS_B	I	The functionality of LPUART1_CTS_B is determined by the UART_EXT field in the reset configuration word (RCW[UART_EXT]).	This pin should be pulled high through a 2-10 kΩ resistor to DV_{DD} or else programmed as GPIO and output.	
LPUART[2:3]_CTS_B	I	The functionality of LPUART[2:3]_CTS_B is determined by the SDHC_EXT field in the reset configuration word (RCW[SDHC_EXT]).	These pins should be pulled high through a 2-10 kΩ resistor to EV_{DD} or else programmed as GPIOs and outputs.	
LPUART1_RTS_B	O	The functionality of LPUART1_RTS_B is determined by the UART_EXT field in the reset configuration word (RCW[UART_EXT]).	These pins can be left unconnected or else programmed as GPIOs and outputs.	

Table continues on the next page...

Table 12. LPUART pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
LPUART[2:3]_RTS_B	O	The functionality of LPUART[2:3]_RTS_B is determined by the SDHC_EXT field in the reset configuration word (RCW[SDHC_EXT]).		
LPUART[1:2]_SIN, LPUART[4]_SIN	I	The functionality of LPUART[1:2]_SIN and LPUART[4]_SIN is determined by the UART_EXT field in the reset configuration word (RCW[UART_EXT]).	These pins should be pulled high through a 2-10 kΩ resistor to DV_{DD} or else programmed as GPIOs and outputs.	
LPUART[3]_SIN, LPUART[5:6]_SIN	I	The functionality of LPUART[3]_SIN and LPUART[5:6]_SIN is determined by the SDHC_EXT field in the reset configuration word (RCW[SDHC_EXT]).	These pins should be pulled high through a 2-10 kΩ resistor to EV_{DD} or else programmed as GPIOs and outputs.	
LPUART[1:2]_SOUT, LPUART[4]_SOUT	O	The functionality of LPUART[1:2]_SOUT and LPUART[4]_SOUT is determined by the UART_EXT fields in the reset configuration word (RCW[UART_EXT]).	These pins can be left unconnected or else programmed as GPIOs and outputs.	
LPUART[3]_SOUT, LPUART[5:6]_SOUT	O	The functionality of LPUART[3]_SOUT and LPUART[5:6]_SOUT is determined by the SDHC_EXT fields in the reset configuration word (RCW[SDHC_EXT]).		

5.5 I2C pin termination recommendations

Table 13. I2C pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
IIC1_SDA	I/O	Tie these open-drain signals high through a nominal 1 kΩ resistor to DV_{DD}. Optimum pull-up value depends on the capacitive loading of external devices and required operating speed.	These pins should be pulled high through a 2-10 kΩ resistor to DV_{DD}.	
IIC1_SCL	I/O			
IIC2_SDA	I/O	The functionality of these signals are determined by the IIC2_EXT field in the reset configuration word (RCW[IIC2_EXT]). Recommend that a weak pull-up resistor (1 kΩ) to be placed on these pins to theirs respective power supply. These pins are an open-drain signal.	When IIC2_EXT field is programmed for IIC2, unused pins should be pulled high through a 2-10 kΩ resistor. Alternately, these pins can be programmed as GPIOs and outputs.	
IIC2_SCL	I/O			

Table continues on the next page...

Table 13. I2C pin termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
IIC3_SDA	I/O	The functionality of these signals are determined by the SCFG_RCWPMUXCR0 register. Recommend that a weak pull-up resistor (1 kΩ) to be placed on these pins to theirs respective power supply. These pins are an open-drain signal.	When SCFG_RCWPMUXCR0 register is programmed for IIC, unused pins should be pulled high through a 2-10 kΩ resistor. Alternately, these pins can be programmed as GPIOs and outputs.	
IIC3_SCL	I/O			
IIC4_SDA	I/O			
IIC4_SCL	I/O			

5.6 eSDHC recommendations

The LS1043A/LS1023A eSDHC interface supports a large variety of devices, as the following list shows:

- SDXC cards upto 2 TB space with UHS-I speed grade are supported
- UHS-I (Ultra high speed grade) SDR12, SDR25, SDR50, SDR104, and DDR50 are supported
- UHS-I cards work on 1.8 V power signaling
- On board dual voltage regulators are needed to support UHS-I cards because card initialization happens at 3.3 V and regular operations happen at 1.8 V. The SD controller provides a signal to control the voltage regulator, controlled via SDHC_VS bit
- eMMC 4.5 is supported (HS200, DDR)

Table 14. Supported SD card Modes

Mode	1-bit support		4-bit support		8-bit support
	LS1043A/ LS1023A	SD (3.0)	LS1043A/ LS1023A	SD (3.0)	
DS (Default Speed)	Yes	Yes	Yes	Yes	Neither supported by the SD standards nor by the LS1043A/ LS1023A device.
HS (High Speed)	Yes	Yes	Yes	Yes	
SDR12	No	No	Yes	Yes	
SDR25	No	No	Yes	Yes	
SDR50	No	No	Yes	Yes	
SDR104	No	No	Yes	Yes	
DDR50	No	No	Yes	Yes	

Table 15. Supported MMC/eMMC Modes

Mode	1-bit support		4-bit support		8-bit support	
	LS1043A/ LS1023A	eMMC (4.5)	LS1043A/ LS1023A	eMMC (4.5)	LS1043A/ LS1023A	eMMC (4.5)
DS (Default Speed)	Yes	Yes	Yes	Yes	Yes	Yes
HS(High Speed)	Yes	Yes	Yes	Yes	Yes	Yes
HS200	No	No	Yes	Yes	Yes	Yes
DDR	No	No	Yes	Yes	No	Yes

5.6.1 eSDHC pin termination recommendations

Table 16. eSDHC pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
SDHC_CMD	I/O	This pin should be pulled high through a 10-100 kΩ resistor to EV_{DD}. The functionality is determined by the SDHC_BASE and SDHC_EXT fields in the reset configuration word (RCW[SDHC_BASE], RCW[SDHC_EXT]).	Program as GPIO and output.	
SDHC_CLK	O	The functionality is determined by the SDHC_BASE and SDHC_EXT fields in the reset configuration word (RCW[SDHC_BASE], RCW[SDHC_EXT]).		
SDHC_DATA[0:3]	I/O	These pins should be pulled high through a 10-100 kΩ resistor to EV_{DD}. The functionality is determined by the SDHC_BASE and SDHC_EXT fields in the reset configuration word (RCW[SDHC_BASE], RCW[SDHC_EXT]).	When SDHC_BASE and SDHC_EXT fields are programmed for SDHC, unused pins should be pulled high through a 10-100 kΩ resistor to EV_{DD}. Alternately, these pins can be programmed as GPIOs and outputs.	
SDHC_DATA[4:7]	I/O	These pins should be pulled high through 10-100 kΩ resistors to OV_{DD}. The functionality is determined by the SPI_BASE and SPI_EXT fields in the reset configuration word (RCW[SPI_BASE], RCW[SPI_EXT]).	Program as GPIOs and outputs.	
SDHC_CD_B	I	These pins should be pulled high through 10-100 kΩ resistors to DV_{DD}. The functionality is determined by the SDHC field in the reset configuration word (RCW[IIC2_EXT]).	This pin should be pulled high through a 10-100 kΩ resistor to DV_{DD} or else programmed as GPIO and output.	
SDHC_WP	I		This pin should be pulled low through a 10-100 kΩ resistor to GND or else programmed as GPIO and output.	
SDHC_CMD_DIR	O	These pins should be pulled high through 10-100 kΩ resistors to OV_{DD}. The functionality is determined by the SPI_BASE and SPI_EXT fields in the reset configuration word (RCW[SPI_BASE], RCW[SPI_EXT]). **NOTE:** DIR signals are used as direction controls of external voltage translator	These pins can be left unconnected or programmed for other functions or else programmed as GPIOs and outputs.	
SDHC_DAT0_DIR	O			
SDHC_DAT123_DIR	O			
SDHC_VS	O	This pin should be pulled high through 10-100 kΩ resistor to OV_{DD}. The functionality is determined by the SPI_EXT field in the reset configuration word (RCW[SPI_EXT]).	This pin can be left unconnected or programmed for other function or else programmed as GPIO and output.	

Table continues on the next page...

Table 16. eSDHC pin termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
		NOTE: External voltage select, to change voltage of external regulator.		
SDHC_CLK_SYNC_IN	I	The functionality is determined by the SPI_EXT field in the reset configuration word (RCW[SPI_EXT]).	This pin should be pulled low through a weak resistor or else programmed for other function.	
SDHC_CLK_SYNC_OUT	O		This pin can be left unconnected or programmed for other function.	

NOTE

1. Separate DIR signals are implemented to support card interrupt on DAT1 in single bit mode.
2. SDHC_CLK_SYNC_OUT to SDHC_CLK_SYNC_IN connection is required in SDR50 and DDR50 mode only.
3. In SDR50 and DDR50 mode, all the input signals are sampled with respect to SDHC_CLK_SYNC_IN.
4. SDHC_CLK_SYNC_OUT and SDHC_CLK_SYNC_IN should be routed as close as possible to the card, with minimum skew with respect to SD_CLK.
5. When using 8-bit MMC/eMMC configuration, EV_{DD} and OV_{DD} should be set at same voltage.
6. As per the SD specification, a power cycle is required to reset the SD card working on UHS-I speed mode. Board design needs to provide some mechanism to power cycle the SD card during every reset.
7. Refer erratum GEN A-010539, which states that SDHC_CLK_SYNC_OUT, SDHC_CLK_SYNC_IN, SDHC_VS, SDHC_DAT[4:7], SDHC_DAT0_DIR, SDHC_DAT123_DIR, SDHC_CMD_DIR, GPIO2_[0:3] are not available when booting from QSPI. Once the workaround is applied HRESET_B can no longer be used. Workaround is not needed in following cases:
   - When SDHC interface is not used at all.
   - SDHC full speed and high speed modes when SDHC_CLK_SYNC_IN and SDHC_CLK_SYNC_OUT are not used.
   - eMMC full speed and high speed in 4 bit mode at 1.8V or 3.3V.
   - eMMC HS200 in 4 bit mode and 1.8V.

5.6.2 eSDHC system-level recommendations

Table 17. eSDHC system-level checklist

Item	Completed
SD Card interfacing (8-bit is not supported)	
SD Card Connections (DS and HS mode)	
EVDD configured for 3.3 V	

Table continues on the next page...

Table 17. eSDHC system-level checklist (continued)

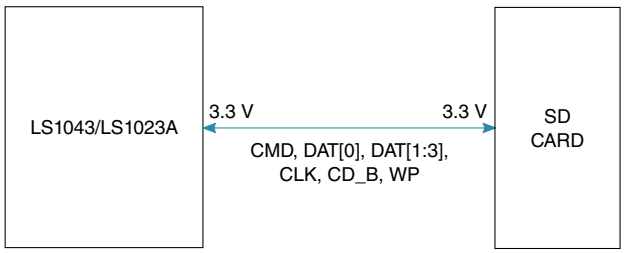
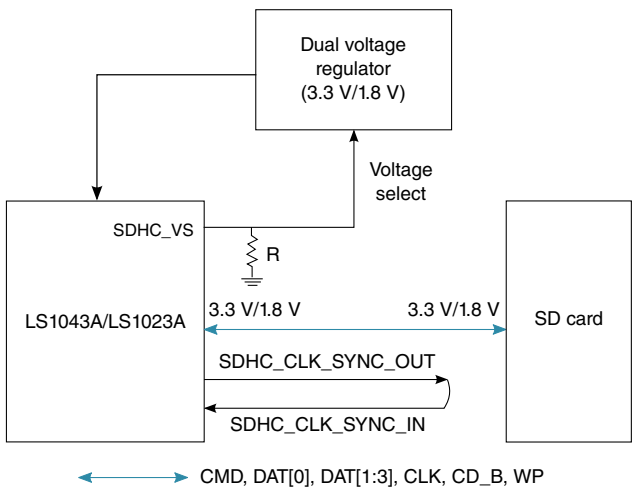
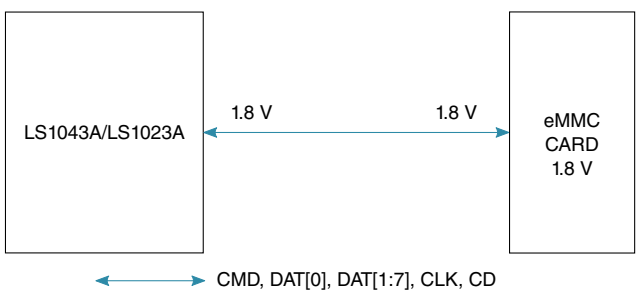
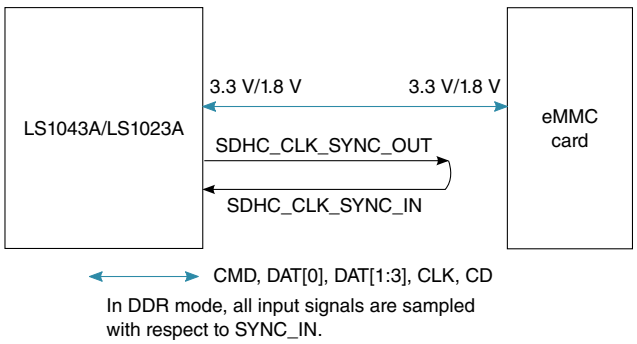
Item	Completed
 **Figure 13. DS and HS modes**	
SD Card Connections (SDR12, 25, 50, 104, and DDR50 modes) UHS-I modes, work on 1.8 V signalling. The SYNC_OUT, SYNC_IN connections are required in SDR50 and DDR50 modes only. **NOTE:** Resistor R=10 K is needed when RCW loading is required to be done from SD card.  **Figure 14. SDR12, 25, 50, 104, and DDR50 modes**	
eMMC Interfacing	
eMMC Card Connections (DS, HS, HS200 Modes) at 1.8 V card The 8-bit eMMC interface requires EVDD and OVDD configured at 1.8 V.  **Figure 15. DS, HS, and HS200 modes for eMMC (1.8 V)**	

Table continues on the next page...

Table 17. eSDHC system-level checklist (continued)

Item	Completed
NOTE: • HS200 mode is 1.8 V only mode as per eMMC 4.5 specification	
eMMC Card Connection in DDR mode The 8-bit operation cannot be supported due to RCW selection constraints. The DDR mode supports both 3.3 V and 1.8 V operation as per eMMC 4.4 specification.  **Figure 16. DDR mode**	

5.7 Global Interrupt Controller (GIC) recommendations

Note that the GIC pins in LS1043/LS1023A are distributed over several voltage domains.

5.7.1 GIC pin termination recommendations

Table 18. GIC pin termination checklist

Signal name	I/O type	Used	Not used	Completed
IRQ[0:2]	I	Ensure these pins are driven in the non-asserted state.	These pins should be tied to non-asserted state through a 2-10 kΩ resistor. • When non-asserted state is high, tied to OV_{DD} • When non-asserted state is low, tied to GND	
IRQ[3:10]	I	Ensure these pins are driven in the non-asserted state. The functionality is determined by the IRQ_BASE and IRQ_EXT fields in the reset configuration word (RCW[IRQ_BASE], RCW[IRQ_EXT]).	These pins should be tied to non-asserted state through a 2-10 kΩ resistor. • When non-asserted state is high, tied to DV_{DD} • When non-asserted state is low, tied to GND or else programmed as GPIOs and ouputs.	

Table continues on the next page...

Table 18. GIC pin termination checklist (continued)

Signal name	I/O type	Used	Not used	Completed
IRQ[11]	I		This pin should be tied to non-asserted state through a 2-10 kΩ resistor. • When non-asserted state is high, tied to LV_{DD} • When non-asserted state is low, tied to GND or else programmed as GPIOs and ouputs.	

NOTE

1. Interrupt polarity can be programmed through Interrupt Polarity Register (SCFG_INTPCR). Default polarity for the IRQs is active high.

5.8 Trust pin termination recommendations

Table 19. Trust pin termination checklist

Signal name	IO type	Used	Not used	Completed
TA_BB_RTC	I	Reserved. Pull to GND through a 2-10 kΩ resistor.		
TA_BB_TMP_DETECT_B	I	If a tamper sensor is used, it must maintain the signal at the specified voltage (1.0 V) until a tamper is detected. A 1 kΩ pull-down resistor is strongly recommended.	This pin should be pulled high through a 2-10 kΩ resistor to V_{DD} (1.0 V).	
TA_TMP_DETECT_B	I	If a tamper sensor is used, it must maintain the signal at the specified voltage (OV_{DD}) until a tamper is detected. A 1 kΩ pull-down resistor is strongly recommended.	This pin should be pulled high through a 2-10 kΩ resistor to OV_{DD}.	

5.9 Power Management pin termination recommendations

Table 20. Power Management pin termination checklist

Signal name	IO type	Used	Not used	Completed
ASLEEP	O	The functionality of this signal is determined by the ASLEEP field in the reset configuration word (RCW[ASLEEP]).	This pin can be left unconnected or else programmed as GPIO and output.	

5.10 Debug and reserved pin recommendations

5.10.1 Debug and reserved pin termination recommendations

Table 21. Debug and test pin termination checklist

Signal name	IO type	Used	Not used	Completed
SCAN_MODE_B	I	This is a test signal for factory use only and must be pulled up (100 Ω - 1 kΩ) to OV_{DD} for normal device operation.		
TEST_SEL_B	I	This pin must be pulled to OV_{DD} through a 100 Ω to 1 kΩ resistor for a four core LS1043A device and tied to the ground for a two core LS1023A device.		
EVT[0:4]_B	IO	Debug event pins	By default EVT[0:4]_B signals are input. EVT0_B has a weak internal pull up and can be left floating and EVT[1:4]_B need to be pulled up through a 2-10 kΩ resistor to OV_{DD}. Alternately, EVT[0:4]_B can be programmed as outputs through EPU_EPEVTCR register early in boot code and left unconnected.	
EVT[5:8]_B	IO	The functionality of these signals is determined by the IIC3 and IIC4 field in the SCFG_RCWPMUXCR0 register.	These pins can be programmed as GPIO outputs through SCFG_RCWPMUXCR0 bits and left unconnected.	
EVT_B[9]	IO	This pin should be connected as required.	This pin should be pulled high through a 2-10 kΩ resistor to OV_{DD}. Alternately, EVT_B[9] can be programmed as output through EPU_EPEVTCR register early in boot code and left unconnected.	
JTAG_BSR_VSEL[1]	I	It is advised that boards are built with the ability to pull up & pull down this pin. • For normal debug operation, this pin must be pulled low to GND through 4.7 kΩ resistor. • For boundary scan operation, this pin must be pulled high to OV_{DD} through 4.7 kΩ resistor.		
TBSCAN_EN_B[2]	I	It is advised that boards are built with the ability to pull up & pull down this pin. • For normal debug operation, this pin must be pulled high to OV_{DD} through 4.7 kΩ resistor. • For boundary scan operation, this pin must be pulled low to GND through 4.7 kΩ resistor.		
CKSTP_OUT_B	O	Reserved. This pin must be pulled to OV_{DD} through a 2-10 kΩ resistor.		
Analog Signals				
D1_TPA	IO	Do not connect. These pins should be left floating.		
FA_ANALOG_G_V	-	Reserved. This pin must be pulled to ground (GND).		
FA_ANALOG_PIN	-	Reserved. This pin must be pulled to ground (GND).		
TH_TPA	-	Do not connect. This pin should be left floating.		
TD1_ANODE	-	Connect as required.	Tie to GND if not used.	
TD1_CATHODE	-	Connect as required.	Tie to GND if not used.	

NOTE

1. JTAG_BSR_VSEL is an IEEE 1149.1 JTAG Compliance Enable pin.
   - 0: normal operation.
   - 1: To be compliant to the 1149.1 specification for boundary scan functions. The JTAG compliant state is documented in the BSDL.
2. TBSCAN_EN_B is an IEEE 1149.1 JTAG Compliance Enable pin.
   - 0:To be compliant to the 1149.1 specification for boundary scan functions. The JTAG compliant state is documented in the BSDL.
   - 1: JTAG connects to DAP controller for the Arm core debug.

5.11 SerDes pin termination recommendations

Table 22. SerDes pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
SD1_IMP_CAL_RX	I	Tie to $S1V_{DD}$ through a 200 Ω 1% resistor.	If the SerDes interface is entirely unused, these pins must be left unconnected.	
SD1_IMP_CAL_TX	I	Tie to $X1V_{DD}$ through a 698 Ω 1% resistor.		
SD1_PLL1_TPA	O	Provide a test point if possible. These pins should be left floating		
SD1_PLL1_TPD	O			
SD1_PLL2_TPA	O			
SD1_PLL2_TPD	O			
SD1_REF_CLK1_P SD1_REF_CLK1_N	I	Ensure clocks are driven from an appropriate clock source, as per the protocol selected by the RCW settings.	If the PLL is unused, pull it down to SD_GND.	
SD1_REF_CLK2_N SD1_REF_CLK2_P	I			
SD1_RX[0:3]_N SD1_RX[0:3]_P	I	Ensure pins are correctly terminated for the interface type used.	If the SerDes interface is entirely or partly unused, the unused pins must be pulled down to SD_GND.	
SD1_TX[0:3]_N SD1_TX[0:3]_P	O	Ensure pins are correctly terminated for the interface type used.	If SerDes interface is entirely or partly unused, the unused pins must be left unconnected.	

NOTE

1. In the RCW configuration field SRDS_PLL_PD_S1, the respective bits for each unused PLL must be set to power it down. The SerDes module is disabled when both of its PLLs are turned off.
2. After POR, if an entire SerDes module is unused, it must be powered down by clearing the SDEN fields of its corresponding PLL1 and PLL2 reset control registers (SRDSxPLLaRSTCTL).
3. Unused lanes must be powered down by clearing the RRST_B and TRST_B fields and setting the RX_PD and TX_PD fields in the corresponding lane's general control register (SRDSxLNmGCR0).
4. A spread-spectrum reference clock is permitted for PCI Express. However, if any other high-speed interface, such as SGMII or SATA, is used concurrently on the same SerDes bank, spread-spectrum clocking is not permitted.
5. If SerDes lanes are routed to a backplane slot or a PCIe connector, SerDes pins can be left unterminated even if the link partner card is not present. If some SerDes

lanes are a no-connect, pull down their receiver pins to GND. Then, if the SerDes block is powered, refer to the RM's Unused Lanes section for directions on how to power them down. To power down a SerDes lane, configure the General Control 0 register during the PBI phase. If the whole SerDes block is already powered down, there is no need to individually power down a lane.

5.11.1 Optimal setting for the SerDes channel Rx Equalization Boost bit

Select the optimal setting for the SerDes channel Rx Equalization Boost bit suitable for a particular end product system board.

For certain high speed SerDes protocols, the Rx Equalization Boost bits for all the SerDes lanes in use are initialized with a default value of 1b by the RCW. In reality, although the default 1b setting does overlap with the 0b setting in terms of Rx Equalization boost effect, the 0b setting works better for short and normal SerDes channels, while the 1b setting works better for high loss channels.

For end product system with non-high loss SerDes channels (lanes), using the default 1b setting of the Rx Equalization Boost bit may adversely enhance the return loss due to some discontinuities possibly presented in the channel. This may further causes more reflection. Therefore, unless the channel is high loss, to ensure the channel's health and better performance, the 0b setting of Rx Equalization Boost bit should be used for all the lanes, instead of the default 1b setting.

The following high speed SerDes protocols are related to this issue. If a protocol supports more than one speed, only the speed(s) listed below is affected.

- SATA 6 Gbaud
- XFI 10.3125 Gbaud

Since the channel characteristics is board and layout dependent, NXP cannot quantify the actual channel loss introduced during board design, layout and fabrication of all end product systems for our customers. Customers should always perform board level simulation and also use other appropriate tool (for example, NXP's SerDes Validation Tool) and/or instrument to determine whether the SerDes channels (lanes) are in high loss condition and then adopt the best setting suitable for their end product and application. Instead of quantifying a SerDes channel as high or non-high loss, a more practical way is to try both the 1b and 0b settings and find out which setting yields better signal integrity for the customer's particular end product system or board.

Once determined that the channels are in non-high loss condition, the Rx Equalization Boost bit for all the lanes in use should be set to 0b during the Pre-boot Initialization (PBI) stage.

Since the Rx Equalization Boost bit is defined in different SerDes registers depending on the SerDes protocols in use, it is important to select the appropriate SerDes register with the correct offset and value as described below when implementing the register write in PBI. The SerDes registers involved are defined on a per lane basis. Therefore, PBI register write must be implemented for all the lanes utilized for the affected SerDes protocols and speeds.

- For SATA 6 Gbaud:
  - Perform a PBI write to each lane's LNaSSCR1 register with a value of 0x0050_2880, which sets this lane's Rx Equalization Boost bit, LNaSSCR1 [RXEQ_BST_1] to 0b.
- For XFI 10.3125 Gbaud:
  - Perform a PBI write to each lane's LNaRECR0 register with a value of 0x0000_045F, which sets this lane's Rx Equalization Boost bit, LNaRECR0 [RXEQ_BST] to 0b.

5.12 USB PHY pin termination recommendations

Table 23. USB 1/2/3 PHY pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
USB[1/2/3]_D_P	IO	USB PHY Data Plus	Do not connect. These pins should be left floating.	
USB[1/2/3]_D_M	IO	USB PHY Data Minus		
USB[1/2/3]_VBUS	I	USB power supply pin. A charge pump external to the USB 3.0 PHY must provide power to this pin. The nominal voltage for this pin is 5 V.	Do not connect.These pins should be left floating.	
USB[1/2/3]_ID	I	USB PHY ID Detect	Pull low through a 1kΩ resistor to GND.	
USB[1/2/3]_TX_P	O	USB PHY 3.0 Transmit Data (positive)	Do not connect.These pins should be left floating.	
USB[1/2/3]_TX_M	O	USB PHY 3.0 Transmit Data (negative)		
USB[1/2/3]_RX_P	I	USB PHY 3.0 Receive Data (positive)	Connect to ground (GND)	
USB[1/2/3]_RX_M	I	USB PHY 3.0 Receive Data (negative)		
USB[1/2/3]_RESREF	IO	Attach a 200-Ω 1% 100-ppm/^{0}C precision resistor-to-ground on the board.	Do not connect.These pins should be left floating.	
USB_DRVVBUS	O	VBUS power enable. For example, if an external hub is used, it can handle this signal. The functionality of the USB_DRVVBUS signal is determined by the RCW[USB_DRVVBUS] field in the reset configuration word. The register SCFG_USBDRVVBUS_SELCR selects which of the three controllers drives USB_DRVVBUS.	Do not connect.These pins can be left floating.	
USB_PWRFAULT	I	Indicates that a VBUS fault has occurred. For example, if an external hub is used, it can handle this signal. The functionality of the USB_PWRFAULT signal is determined by the RCW[PWRFAULT] field in the reset configuration word. USB_PWRFAULT can be shared by all the three controllers, selection is through SCFG_USBPWRFAULT_SELCR register bits.	Pull low through a 1kΩ resistor to GND.	
USB2_DRVVBUS	O	VBUS power enable. For example, if an external hub is used, it can handle this signal. The functionality of the USB2_DRVVBUS signal is determined by Extended RCW PinMux Control Register (SCFG_RCWPMUXCR0) in bitfield IIC3_SCL.	Do not connect.These pins can be left floating.	

Table continues on the next page...

Table 23. USB 1/2/3 PHY pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
USB2_PWRFAULT	I	Indicates that a VBUS fault has occurred. For example, if an external hub is used, it can handle this signal. The functionality of the USB_PWRFAULT signal is determined by by Extended RCW PinMux Control Register(SCFG_RCWPMUXCR0) in bitfield IIC3_SDA. The register SCFG_USBPWRFAULT_SELCR[USB2 _SEL] can be used to select dedicated USB2_PWRFAULT signal or to select shared USB_PWRFAULT signal for USB controller 2.	Pull low through a 1kΩ resistor to GND.	
USB3_DRVVBUS	O	VBUS power enable. For example, if an external hub is used, it can handle this signal. The functionality of the USB_DRVVBUS signal is determined by by Extended RCW PinMux Control Register(SCFG_RCWPMUXCR0) in bitfield IIC4_SCL.	Do not connect.These pins can be left floating.	
USB3_PWRFAULT	I	Indicates that a VBUS fault has occurred. For example, if an external hub is used, it can handle this signal. The functionality of the USB_PWRFAULT signal is determined by by Extended RCW PinMux Control Register(SCFG_RCWPMUXCR0) in bitfield IIC4_SDA. The register SCFG_USBPWRFAULT_SELCR[USB3 _SEL] can be used to select dedicated USB3_PWRFAULT signal or to select shared USB_PWRFAULT signal for USB controller 3.	Pull low through a 1kΩ resistor to GND.	

NOTE

USB3.0 PLLs can receive clock either from SYSCLK or DIFF_SYSCLK/ DIFF_SYSCLK_B. Ensure that clock selected has 100 MHz frequency.

5.12.1 USB1 PHY connections

This section describes the hardware connections required for the USB PHY.

This figure shows the VBUS interface for the chip.

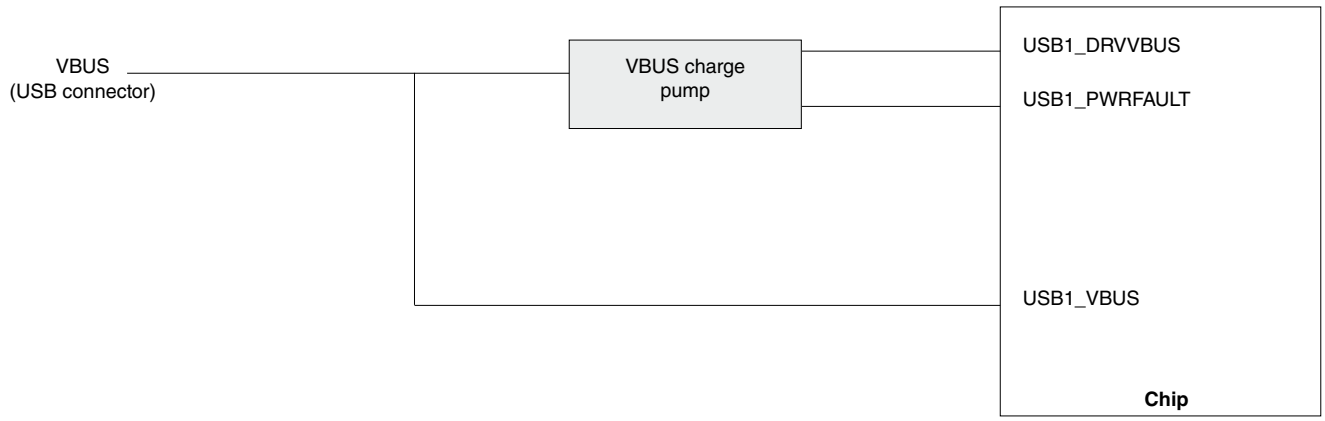


Figure 17. USB1 PHY VBUS interface

5.13 Ethernet Management Interface 1/2 pin termination recommendations

Table 24. Ethernet Management Interface (EMI1/2) pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
EMI1_MDC	O	The functionality of this signal is determined by the EM1 field in the reset configuration word (RCW[EM1]). To configure as open drain signal, write to EMI1_CMODE field in reset configuration word (RCW[EMI1_CMODE]).[3,5]	These pins should be tied low through a 2-10 kΩ resistor to ground (GND), or may be configured as a GPIOs and outputs.	
EMI1_MDIO	IO	The functionality of this signal is determined by the EM1 field in the reset configuration word (RCW[EM1]). To configure as open drain signal, write to EMI1_DMODE field in reset configuration word (RCW[EMI1_DMODE]).[3,6]		
EMI2_MDC	O	The functionality of these signals is determined by the EM1 field in the reset configuration word (RCW[EM2]). To configure as open drain signal, write to EMI1_CMODE field in reset configuration word (RCW[EMI2_CMODE]).[4,5]	These pins should be tied low through a 2-10 kΩ resistor to ground (GND), or may be configured as a GPIOs and outputs.	

Table continues on the next page...

Table 24. Ethernet Management Interface (EMI1/2) pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
EMI2_MDIO	IO	The functionality of this signal is determined by the EM1 field in the reset configuration word (RCW[EM2]). To configure as open drain signal, write to EMI1_DMODE field in reset configuration word (RCW[EMI2_DMODE]).[4,6]		

NOTE

1. Refer Ethernet A-010717: EMI -MDIO to MDC input hold time (tMDDXKH) specification violation from LS1043A Chip errata.
2. For MDC frequency greater than 2.5 MHz and less than (or equal to) 10 MHz, the load on the MDC/MDIO pads must not exceed 75pf.
3. If configured as open-drain, pull this pin to LVDD with a suitable resistor.
4. If configured as open-drain, pull this pin to TVDD with a suitable resistor.
5. In open-drain mode, the value of pull-up resistor depends on input impedance of all the peripherals connected on EMI bus. More the peripherals or more the impedance, stronger the pull-up. Typically 200Ω pull-up should suffice for 3-4 peripherals. Unless there is a requirement of MDC being an open-drain, it is advised to configure MDC in "normal functional" mode. In "normal functional" mode, the MDC will be actively driven and pull up resistors are not required.
6. In open-drain mode, the value of pull-up resistor depends on input impedance of all the peripherals connected on EMI bus. More the peripherals or more the impedance, stronger the pull-up. Typically 330Ω pull-up should suffice for 3-4 peripherals. Unless there is a requirement of MDIO being an open-drain, it is advised to configure MDIO in "normal functional" mode. In "normal functional" mode, the MDIO will be actively driven. A pull up resistors might still be required as the peripherals on EMI bus might have their MDIO pins configured as open-drain. The value of pull-up resistor depends on total input impedance of all the peripherals connected.

5.13.1 Ethernet controller pin termination recommendations

The LS1043A/LS1023A supports two Ethernet Controllers (EC) which can connect to Ethernet PHYs using RGMII protocols. Both, EC1 and EC2 operated using LVDD supply which supports 1.8 V/2.5 V operation.

Table 25. Ethernet controller pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
EC1 in RGMII mode				
EC1_TXD[0:3], EC1_TX_EN	O	The functionality of these signals is determined by the EC1 field in the reset configuration word (RCW[EC1]). FMAN-MAC3 is connected to EC1 interface when RGMII is selected through RCW[EC1] field.	Entire EC1 interface can be configured as GPIOs and outputs through RCW[EC1]	
EC1_GTX_CLK	O			
EC1_RXD[0:3]	I			
EC1_RX_DV	I			

Table continues on the next page...

Table 25. Ethernet controller pin termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
EC1_RX_CLK	I	EC1_TX_EN requires an external 1-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.		
EC1_GTX_CLK125[1]	I			
EC2 in RGMII mode				
EC2_TXD[0:3], EC2_TX_EN	O	The functionality of these signals is determined by the EC2 field in the reset configuration word (RCW[EC2]). FMAN-MAC4 is connected to EC2 interface when RGMII is selected through RCW[EC2] field. EC2_TX_EN requires an external 1-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.	Entire EC2 interface can be configured as GPIOs and outputs through RCW[EC2]	
EC2_GTX_CLK	O			
EC2_RXD[0:3]	I			
EC2_RX_DV	I			
EC2_RX_CLK	I			
EC2_GTX_CLK125[1]	I			

NOTE

1. Either of the EC1_GTX_CLK125 or EC2_GTX_CLK125 can be used to clock both the EC interfaces in RGMII mode. The selection is through SCFG_ECGTXCMCR[CLKSEL]. The unused clock pin should be pulled to GND.

5.14 QUICC Engine recommendations

The QUICC Engine block in the LS1043A/LS1023A device supports two TDM/HDLC interfaces.

The functionality of these signals is determined by the QE-TDMA and QE-TDMB fields in the reset configuration word.

The QUICC Engine supports 3.3 V and 1.8 V operation only.

5.14.1 QUICC Engine pin termination recommendations

Table 26. QUICC Engine pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
QE Clock Signals				
BRGO[1 & 4]	O	The functionality of these signals is determined by the IIC3_SDA and IIC3_SCL field in SCFG_RCWPMUXCR0 register.	Program as GPIOs and as output.	
CLK[11:12]	I			
BRGO[2:3]	O	The functionality of these signals is determined by the IIC2_EXT field in reset configuration word (RCW[IIC2_EXT]).	Program as GPIOs and as output.	
CLK[9:10]	I			

Table continues on the next page...

Table 26. QUICC Engine pin termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
		RCW[QE_CLK_OVRRIDE] field in reset configuration word provides options to select other combinations of BRGs and CLKs. For more details, see the *QorIQ LS1043A Reference Manual* (document LS1043ARM).		
UCC1 signals				
UC1_CDB_RXER	I	The functionality of these signals is determined by the RCW[IRQ_EXT] field in the reset configuration word except for UC1_CDB_RXER which is determined by the IIC4_SCL bitfield in register SCFG_RCWPMUXCR0.	If UCC1 is not used, all the pins can be programmed as GPIOs and outputs.	
UC1_CTSB_RXDV	I			
UC1_RXD7	I			
UC1_TXD7	O			
UC1_RTSB_TXEN	O			
UCC3 signals				
UC3_CDB_RXER	I	The functionality of these signals is determined by the RCW[IRQ_EXT] field in the reset configuration word except for UC3_CDB_RXER which is determined by the IIC4_SDA bitfield in register SCFG_RCWPMUXCR0.	If UCC3 is not used, all the pins can be programmed as GPIOs and outputs.	
UC3_CTSB_RXDV	I			
UC3_RXD7	I			
UC3_TXD7	O			
UC3_RTSB_TXEN	O			
TDMA signals				
TDMA_TXD	O	The functionality of these signals is determined by the RCW[IRQ_EXT] field in the reset configuration word except for TDMA_RQ which is determined by the IIC4_SCL bitfield in register SCFG_RCWPMUXCR0.	If TDMA is not used, all the pins can be programmed as GPIOs and outputs.	
TDMA_TSYNC	I			
TDMA_RQ	O			
TDMA_RSYNC	I			
TDMA_RXD	I			
TDMB signals				
TDMB_TXD	O	The functionality of these signals is determined by the RCW[IRQ_EXT] field in the reset configuration word except for TDMB_RQ which is determined by the IIC4_SDA bitfield in register SCFG_RCWPMUXCR0.	If TDMB is not used, all the pins can be programmed as GPIOs and outputs.	
TDMB_TSYNC	I			
TDMB_RQ	O			
TDMB_RSYNC	I			
TDMB_RXD	I			

5.15 QSPI pin termination recommendations

Table 27. QSPI pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
QSPI_A_SCK	O	The functionality of these signals is determined by the RCW[IFC_GRP_F_EXT] bits of reset configuration word.	These pins can be left unconnected.	
QSPI_B_SCK	O			
QSPI_A_CS[0:1][2]	O			
QSPI_B_CS[0:1][2]	O			

Table continues on the next page...

Table 27. QSPI pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
QSPI_A_DATA[0:2]	IO		If these pins are not used, they should be pulled to GND through 1 kΩ resistor.	
QSPI_A_DATA[3]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_A_EXT] bits of reset configuration word.	If these pins are not used, it should be programmed as GPIOs and output.	
QSPI_B_DATA[0:2]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_D_EXT] bits of reset configuration word.		
QSPI_B_DATA[3]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_E1_EXT] bits of reset configuration word.		

NOTE

1. QSPI signals are multiplexed with IFC signals and only select lines are available on IFC when QSPI is used.
2. To avoid glitches or noise on chip select, it is recommended to use series resistor of 22Ω to 68Ω along with a 20pf capacitor to GND. The capacitor should be placed close to the receiver.
3. If RCW[IFC_GRP_A_EXT] = 001, then IFC_A26 and IFC_A27 should be pulled to GND through 4.7 kΩ resistor. Otherwise, these pins should be configured as output GPIOs and left as unconnected.

5.16 SPI recommendations

The LS1043A/LS1023A serial peripheral interface (SPI) pins are powered from OVDD supply, which supports only 1.8 V power.

5.16.1 SPI pin termination recommendations

Table 28. SPI pin termination checklist

Signal name	I/O type	Used	Not used	Completed
SPI_MISO **(SPI_SIN)**	I	The functionality of these signals is determined by the SPI_BASE and SPI_EXT field in the reset configuration (RCW[SPI_BASE],RCW[SPI_EXT]).	These pins should be pulled high through a 2-10 kΩ resistor to OV_{DD}.	
SPI_MOSI **(SPI_SOUT)**	I/O			
SPI_CLK **(SPI_SCK)**	O		These pins can be left unconnected.	
SPI_CS[0:3]_B **(SPI_PCS[0:3])**	O			

NOTE

1. The names in above table follow the following nomenclature:

   X(**Y**) : Name in 21x21, 621 ball package (**Name in 23x23, 780 ball package**).

2. SPI_CLK is available only when RCW[SPI_EXT]=000 and RCW[SPI_BASE]=00. Master mode requires that SPI_CLK is generated by Master, therefore only RCW[SPI_EXT]=000 and RCW[SPI_BASE]=00 can be used for SPI controller on this device although some SPI signals are also available when RCW[SPI_EXT]=001/010.

5.17 General Purpose Input/Output pin termination recommendations

Table 29. General Purpose Input/Output pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
GPIO1_13	O	The functionality of this signal is determined by the RCW[ASLEEP] field in the reset configuration word.	For all GPIO1 pins: When programmed as outputs, no termination is required.	
GPIO1_14	IO	The functionality of this signal is determined by the RCW[RTC] field in the reset configuration word.		
GPIO1_[15:22]	IO	The functionality of these signals is determined by the RCW[UART_BASE] & RCW[UART_EXT] field in the reset configuration word.		
GPIO1_[23:31]	IO	The functionality of these signals is determined by the RCW[IRQ_EXT] and RCW[IRQ_BASE] fields in the reset configuration word.		
GPIO2_[0:3]	IO	The functionality of these signals is determined by the RCW[SPI_BASE] fields in the reset configuration word.	For all GPIO2 pins: When programmed as outputs, no termination is required.	
GPIO2_[4:9]	IO	The functionality of these signals is determined by the RCW[SDHC_BASE] fields in the reset configuration word.		
GPIO2_[10:12]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_E1_BASE] field in the reset configuration word.		
GPIO2_[13:15]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_D_BASE] fields in the reset configuration word.		

Table continues on the next page...

Table 29. General Purpose Input/Output pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
GPIO2_[25:27]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_A_BASE] field in the reset configuration word.		
GPIO3_[0:1]	IO	The functionality of these signals is determined by the RCW[EM1] field in the reset configuration word.	For all GPIO3 pins: When programmed as outputs, no termination is required.	
GPIO3_[2:14]	IO	The functionality of these signals is determined by the RCW[EC1] field in the reset configuration word.		
GPIO3_[15:27]	IO	The functionality of these signals is determined by the RCW[EC2] field in the reset configuration word.		
GPIO4_[0:1]	IO	The functionality of these signals is determined by the RCW[EM2] field in the reset configuration word.	For all GPIO4 pins: When programmed as outputs, no termination is required.	
GPIO4_[2:3]	IO	The functionality of these signals is determined by the RCW[IIC2_EXT] field in the reset configuration word.		
GPIO4_[10:11]	IO	The functionality of these signals is determined by the IIC3_SCL and IIC3_SDA fields in SCFG_RCWPMUXCR0 respectively.		
GPIO4_[12:13]	IO	The functionality of these signals is determined by the IIC4_SCL and IIC4_SDA fields in SCFG_RCWPMUXCR0 respectively.		
GPIO4_[29]	IO	The functionality of these signals is determined by the RCW[USB_DRVVBUS] field in the reset configuration word.		
GPIO4_[30]	IO	The functionality of these signals is determined by the RCW[USB_PWRFAULT] fields in the reset configuration word.		

5.18 FTM1 pin termination recommendations

Table 30. FTM1 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM1_CH[0:7]	IO	The functionality of these signals is determined by the EC1 field in the reset configuration (RCW[EC1]).	Program as GPIOs and outputs.	
FTM1_EXTCLK	I			
FTM1_FAULT	I			
FTM1_QD_PHA	I			
FTM1_QD_PHB	I			

5.19 FTM2 pin termination recommendations

Table 31. FTM2 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM2_CH[0:7]	IO	The functionality of these signals is determined by the EC2 field in the reset configuration (RCW[EC2]).	Program as a GPIO and as an output.	
FTM2_EXTCLK	I			
FTM2_FAULT	I			
FTM2_QD_PHA	I			
FTM2_QD_PHB	I			

5.20 FTM3 pin termination recommendations

Table 32. FTM3 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM3_CH[0:7]	IO	The functionality of these signals is determined by the IRQ_BASE and IRQ_EXT fields in the reset configuration word (RCW[IRQ_BASE], RCW[IRQ_EXT]).	Program as a GPIO and as an output.	
FTM3_EXTCLK	I	The functionality of these signals is determined by the IIC4_SDA bitfield in register SCFG_RCWPMUXCR0.		
FTM3_FAULT	I			
FTM3_QD_PHA	I	The functionality of these signals is determined by the IIC2_EXT fields in the reset configuration word (RCW[IIC2_EXT]).		
FTM3_QD_PHB	I			

5.21 FTM4 pin termination recommendations

Table 33. FTM4 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM4_CH[0:7]	IO	The functionality of FTM4_CH[0-5] signals is determined by the UART_EXT fields in the reset configuration word (RCW[UART_EXT]). The functionality of FTM4_CH6 and FTM4_CH7 signals is determined by the SDHC_EXT fields in the reset configuration word (RCW[SDHC_EXT]).	Program as a GPIO and as an output.	
FTM4_EXTCLK	I	The functionality of these signals is determined by the SDHC_EXT fields in the reset configuration word (RCW[SDHC_EXT]).		
FTM4_FAULT	I			
FTM4_QD_PHA	I			
FTM4_QD_PHB	I			

5.22 FTM5 pin termination recommendations

Table 34. FTM5 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM5_CH[0:1]	IO	The functionality of these signals is determined by the IFC_GRP_A_EXT fields in the reset configuration word (RCW[IFC_GRP_A_EXT]).	Program as a GPIO and as an output.	
FTM5_EXTCLK	I			

5.23 FTM6 pin termination recommendations

Table 35. FTM6 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM6_CH[0:1]	IO	The functionality of these signals is determined by the IFC_GRP_D_EXT fields in the reset configuration word (RCW[IFC_GRP_D_EXT]).	Program as a GPIO and as an output.	
FTM6_EXTCLK	I			

5.24 FTM7 pin termination recommendations

Table 36. FTM7 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM7_CH[0:1]	IO	The functionality of these signals is determined by the IFC_GRP_E1_EXT fields in the reset configuration word (RCW[IFC_GRP_E1_EXT]).	Program as a GPIO and as an output.	
FTM7_EXTCLK	I			

5.25 FTM8 pin termination recommendations

Table 37. FTM8 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM8_CH[0:1]	IO	The functionality of these signals is determined by the IIC3_SCL and IIC3_SDA bitfields respectively in register SCFG_RCWPMUXCR0.	Program as a GPIO and as an output.	

5.26 IEEE 1588 recommendations

5.26.1 IEEE 1588 pin termination recommendations

Table 38. IEEE 1588 pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
TSEC_1588_CLK_IN	I	Connect to external high-precisiontimer reference input. The functionality of this signal is determined by the EC2 field in the reset configuration word (RCW[EC2]).	Program as GPIOs and outputs.	
TSEC_1588_ALARM_OUT1	O	The functionality of these signals is determined by the EC2 field in the reset configuration word (RCW[EC2]).		
TSEC_1588_ALARM_OUT2	O			
TSEC_1588_CLK_OUT	O			
TSEC_1588_PULSE_OUT1	O			

Table continues on the next page...

Table 38. IEEE 1588 pin termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
TSEC_1588_PULSE_OUT2	O			
TSEC_1588_TRIG_IN1	I			
TSEC_1588_TRIG_IN2	I			

NOTE

When configured for IEEE 1588, the EC2 pins those are not available for IEEE 1588, are configured for GPIO. All IEEE 1588 pins are referenced to LV_{DD}.

5.27 System control pin termination recommendations

Table 39. System Control pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
PORESET_B	I	This pin is required to be asserted as per the applicable chip data sheet, in relation to minimum assertion time and during power-up/power-down. It is an input-only pin and must be asserted to sample power on configuration pins.		
HRESET_B	I/O	This pin is an open drain signal and should be pulled high through a 2-10 kΩ resistor to OV_{DD}.		
RESET_REQ_B	O	Must not be pulled down during power-on reset.	This pin should be pulled high through a 2-10 kΩ resistor to OV_{DD} and must not be pulled down during power-on reset.	

NOTE

1. If on-board programming of NOR and NAND boot flash, QSPI boot flash, or SD card is needed, then maintain an option (may be via a jumper) that keeps PORESET_B and RESET_REQ_B disconnected from each other. Booting from a blank flash causes boot error, which in turn causes assertion of RESET_REQ_B. When RESET_REQ_B is connected with PORESET_B, the device goes in a recurring reset loop and does not provide enough time for JTAG to take control of the device and perform any operation.
2. For RCW override, RESET_REQ_B should be disconnected from PORESET_B or HRESET_B. An option on board is required.

5.28 JTAG pin termination recommendations

Table 40. JTAG pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
TCK	I	Connect to pin 4 of the Arm Cortex 10-pin header. This pin requires a 2-10 kΩ resistor to OV_{DD}.		

Table continues on the next page...

Table 40. JTAG pin termination checklist (continued)

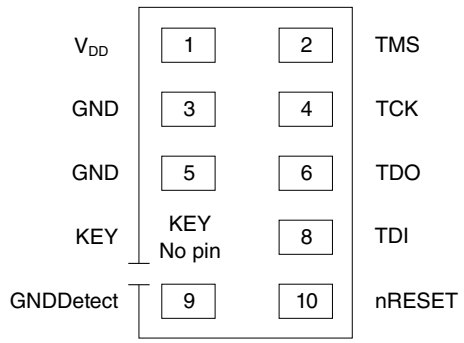
Signal Name	IO type	Used	Not Used	Completed
TDI	I	Connect to pin 8 of the Arm Cortex 10-pin header. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.	May be left unconnected.	
TDO	O	Connect to pin 6 of the Arm Cortex 10-pin header. This output is actively driven during reset rather than being tri-stated during reset.	May be left unconnected.	
TMS	I	Connect to pin 2 of the Arm Cortex 10-pin header. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.	May be left unconnected.	
TRST_B	I	This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled. Connect as shown in Figure 18.	Tie TRST_B to PORESET_B through a 0 kΩ resistor.	

5.28.1 JTAG system-level recommendations

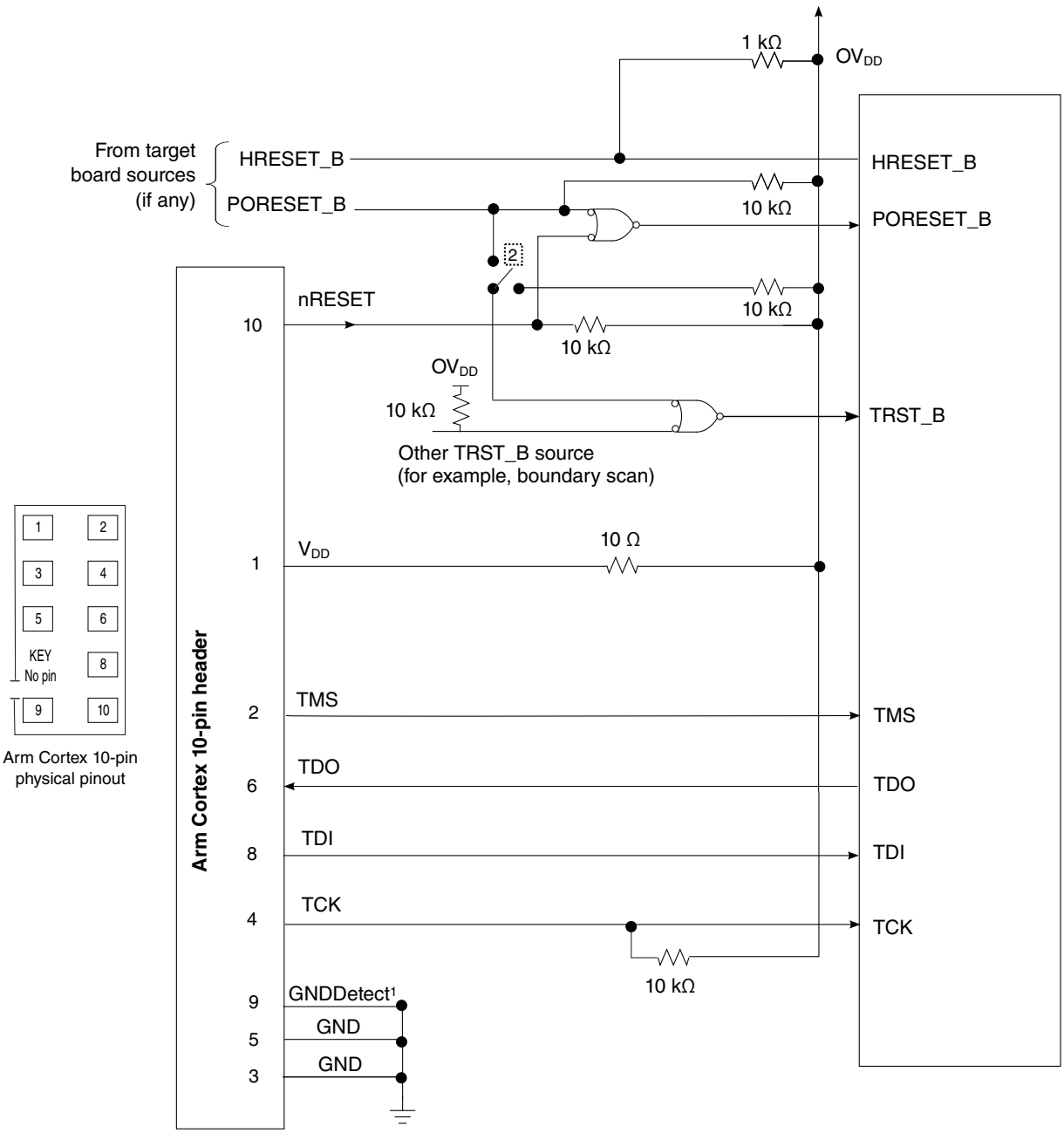
Table 41. JTAG system-level checklist

Item	Completed
Arm®Cortex® 10-pin header signal interface to JTAG port	
Configure the group of system control pins as shown in Figure 18. **NOTE:** These pins must be maintained at a valid deasserted state under normal operating conditions, because most have asynchronous behavior and spurious assertion gives unpredictable results.	
The JTAG port of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The Arm Cortex 10-pin header connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The Arm Cortex 10-pin header interface requires the ability to independently assert PORESET_B in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the nRESET signals must be merged into these signals with logic.	
Boundary-scan testing	
Ensure that TRST_B is asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation.	
Follow the arrangement shown in Figure 18 to allow the Arm Cortex 10-pin header to assert PORESET_B independently while ensuring that the target can drive PORESET_B as well.	
The Arm® Cortex® 10-pin interface has a standard header, shown in the following figure. The connector typically has pin 7 removed as a connector key. The signal placement recommended in this figure is common to all known emulators.	

Table 41. JTAG system-level checklist

Item	Completed
 **NOTE:** The Arm Cortex 10-pin header adds many benefits such as breakpoints, watch points, register and memory examination/modification, and other standard debugger features. An inexpensive option is to leave the Arm Cortex 10-pin header unpopulated until needed.	

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 18. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions, as most have asynchronous behavior and spurious assertion gives unpredictable results.



Note:
1. GNDDetect is an optional board feature. Check with 3rd-party tool vendor.
2. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, ensure this switch is closed.

Figure 18. JTAG interface connection

5.29 SerDes block power supply decoupling recommendations

The SerDes block requires a clean, tightly regulated source of power ($S1V_{DD}$ and $X1V_{DD}$) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below:

1. The board should have at least 1 x 0.1 uF SMT ceramic chip capacitor placed as close as possible to each supply ball of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground

connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.

2. Between the device and any SerDes voltage regulator, there should be a lower bulk capacitor. For example, a 10 uF, low ESR SMT tantalum or ceramic capacitor. There should also be a higher bulk capacitor. For example, a 100-300 uF low ESR SMT tantalum or ceramic capacitor.

NOTE

Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

5.30 Clock pin termination recommendations

Table 42. Clock pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
EC1_GTX_CLK	O	The functionality of this signal is determined by the EC1 field in the reset configuration word (RCW[EC1]). The LS1043A chip has a duty cycle reshaper inside RGMII block. This allows GTX clock from RGMII PHY to be used.	Program as a GPIO and as an output.	
EC1_GTX_CLK125[4]	I			
EC2_GTX_CLK	O	The functionality of this signal is determined by the EC2 field in the reset configuration word (RCW[EC2]). The LS1043A chip has a duty cycle reshaper inside RGMII block. This allows GTX clock from RGMII PHY to be used.	Program as a GPIO and as an output.	
EC2_GTX_CLK125[4]	I			
SYSCLK[1]	I	This is the single-ended primary clock input to the chip. It supports a 64.0 MHz to 100.0 MHz clock range. Note that 64 MHz SYSCLK reference frequency is specifically for Profibus support on QUICC Engine.	This pin should be pulled low through a 2-10 kΩ resistor to GND.	
DIFF_SYSCLK[3]	I	These pins are the differential primary clock input to the chip. These pins support 100 MHz only. When used, these pins should be connected to a 100 MHz differential clock generator.	These pins should be pulled low through a 2-10 kΩ resistor to GND, or they can be left floating.	
DIFF_SYSCLK_B[3]	I			
RTC	I	The functionality of this signal is determined by the RTC field in the reset configuration word (RCW[RTC]).	Pull low through a 2-10 kΩ resistor to GND, or program pin as a GPIO and output.	

Table continues on the next page...

Table 42. Clock pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
		NOTE: RTC is the only clock source for WDOG functionality. To support WDOG functionality RTC required 32 KHz external clock source. Without supplying the 32 KHz external clock source the WDOG functionality will be inoperable.		
DDRCLK[2]	I	The reference clock for the DDR controller supports a 64 MHz to 100 MHz input clock range.	This pin should be pulled low through a 2-10 kΩ resistor to GND.	

NOTE

1. In the "Single Oscillator Source" reference clock mode supported by LS1043A, DIFF_SYSCLK/DIFF_SYSCLK_B (differential) clock inputs are used as primary clock inputs and SYSCLK is unused. Power-on-configuration signal cfg_eng_use0 selects between SYSCLK (single ended) and DIFF_SYSCLK/DIFF_SYSCLK_B (differential) clock inputs.
2. In the "Single Oscillator Source" reference clock mode, DIFF_SYSCLK/ DIFF_SYSCLK_B clock inputs can be selected to feed the DDR PLL. RCW bits [DDR_REFCLK_SEL] are used for this selection and DDRCLK is unused. The options for RCW bits 186-187 (RCW[DDR_REFCLK_SEL], DDR reference clock selection) are as follows:
   a. 2'b00: The DDRCLK pin provides the reference clock to the DDR PLL
   b. 2'b01: DIFF_SYSCLK/DIFF_SYSCLK_B provides the reference clock to the DDR PLL
3. When SYSCLK is chosen as the primary clock input to the chip, these pins are unused.
4. Either of the EC1_GTX_CLK125 or EC2_GTX_CLK125 can be used to clock both the EC interfaces in RGMII mode. The selection can be made through SCFG_ECGTXCMCR[CLKSEL].

5.31 Single source clocking

The chip supports the single source clocking options with single, two, and more reference clocks.

5.32 Single Oscillator Source reference clock mode

In this mode, single onboard oscillator can provide the reference clock (100 MHz) to the following PLLs:

- Platform PLL
- Core PLLs
- USB PLL

- DDR PLL
- SerDes PLLs

The reset configuration field identifies whether the SYSCLK (single-ended) or DIFF_SYSCLK (differential) is selected as the clock input to the chip.

The RCW[DDR_REFCLK_SEL] bit is used to select clock input (DIFF_SYSCLK or DDRCLK) to the DDR PLL.

The following figure shows the system view of single oscillator source clocking. In this figure, the on-board oscillator generates three differential clock outputs. The first differential output is used to provide the clock to system clock associated PLLs and DDR PLL. However, the second and third differential outputs are used to provide clocks to SerDes PLLs.

A multiplexer between system clock and USBCLK is used to provide the USB PHY reference clock to the USB PLL. And, multiplexer between DIFF_SYSCLK/DIFF_SYSCLK_B inputs and DDRCLK is used to provide reference clock to the DDR PLL.

The duty cycle reshaper reshapes the 125 MHz EC*n*_GTX_CLK125 which is fed into frame manager for transmission as EC*n*_GTX_CLK.

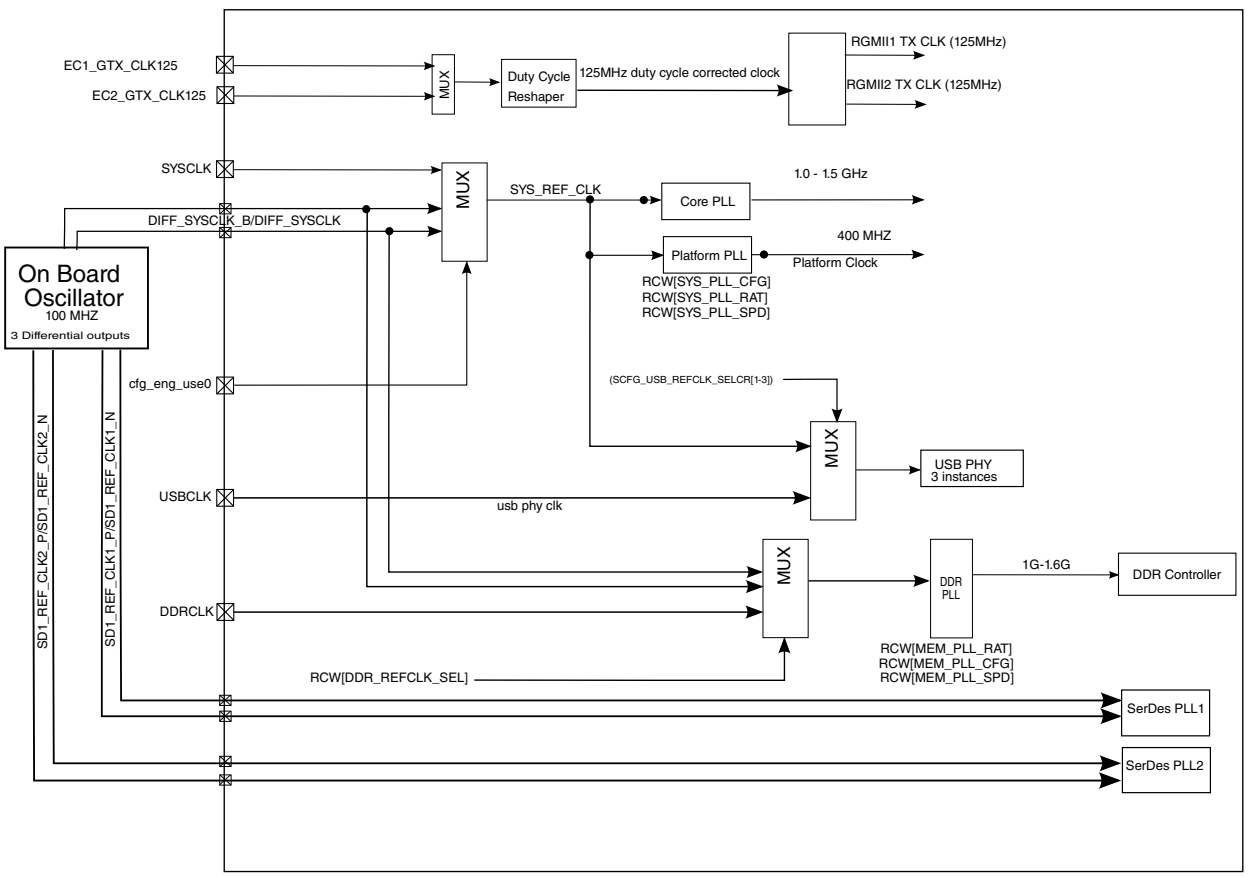


Figure 19. Single oscillator source clocking

5.33 *Single Oscillator Source* clock select

The single oscillator source clock select input, described in this table, selects between SYSCLK (single ended) and DIFF_SYSCLK/DIFF_SYSCLK_B (differential) inputs.

Table 43. Single oscillator source clock select

Functional signals	Reset configuration name	Value (binary)	Options
IFC_WE0_B Default (1)	cfg_eng_use0	0	DIFF_SYSCLK/DIFF_SYSCLK_B (differential)
		1	SYSCLK (single ended)
IFC_OE_B Default (1)	cfg_eng_use1 On-chip LVDS termination must NOT be enabled when external (off-chip) termination are active.	0	On-chip LVDS termination disabled
		1	On-chip LVDS termination enabled
IFC_WP_B[0]	cfg_eng_use2	Don't care	Reserved

5.34 DIFF_SYSCLK/DIFF_SYSCLK_B system-level recommendations

Table 44. DIFF_SYSCLK/DIFF_SYSCLK_B system-level checklist

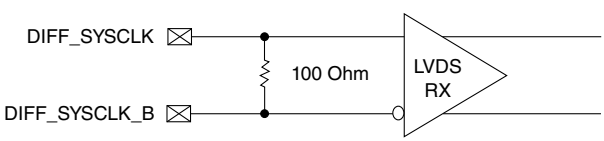
Item	Completed
DIFF_SYSCLK/DIFF_SYSCLK_B can be selected to provide primary clock to the chip. Although it is a Low Voltage Differential Signaling (LVDS) type clock driver but it has AC/DC characteristics identical to the SerDes reference clock inputs which are High-Speed Current Steering Logic (HCSL)-compatible. This eases system design as same clock driver can be used to provide the various differential clock inputs required by the chip  **Figure 20. LVDS receiver**	
Interfacing DIFF_SYSCLK/DIFF_SYSCLK_B with other Differential Signalling levels	
Connection with HCSL Clock driver	

Table continues on the next page...

Table 44. DIFF_SYSCLK/DIFF_SYSCLK_B system-level checklist (continued)

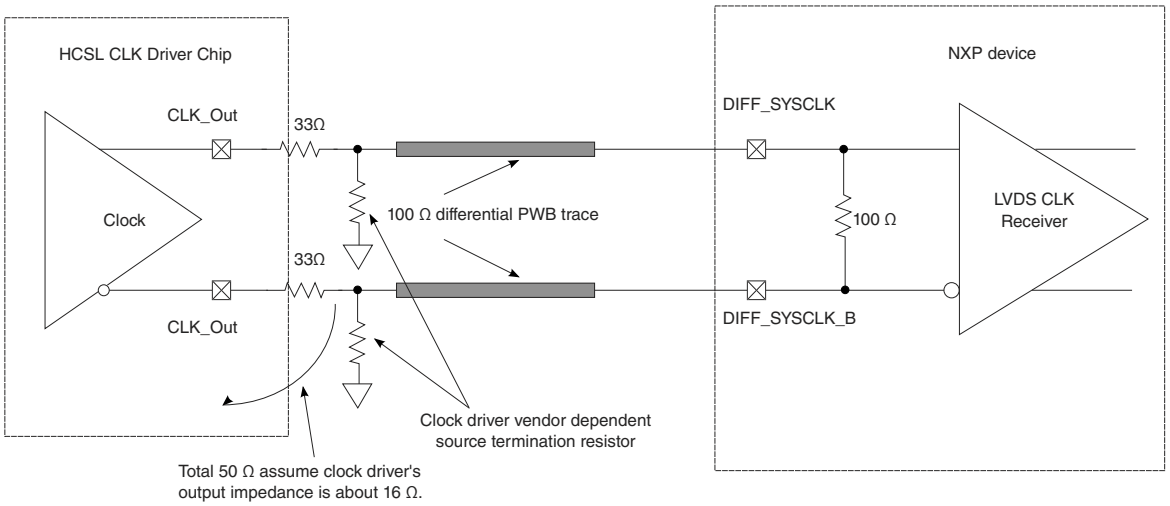
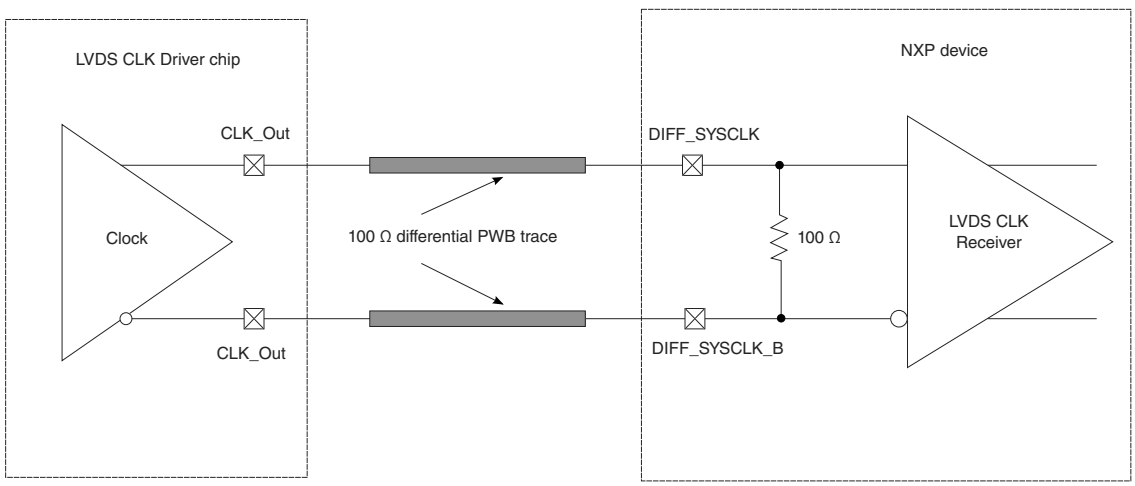
Item	Completed
 **Figure 21. Interfacing with HCSL clock driver (Reference only)**	
Connection with LVDS Clock driver  **Figure 22. Interfacing with LVDS clock driver (Reference only)**	
Connection with LVPECL Clock driver	

Table continues on the next page...

Table 44. DIFF_SYSCLK/DIFF_SYSCLK_B system-level checklist (continued)

Item	Completed

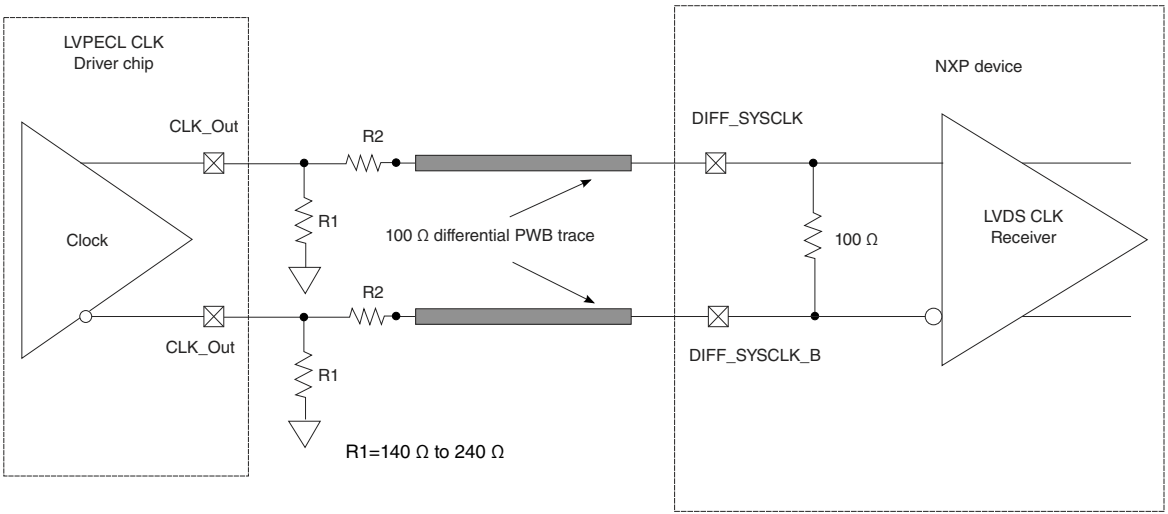
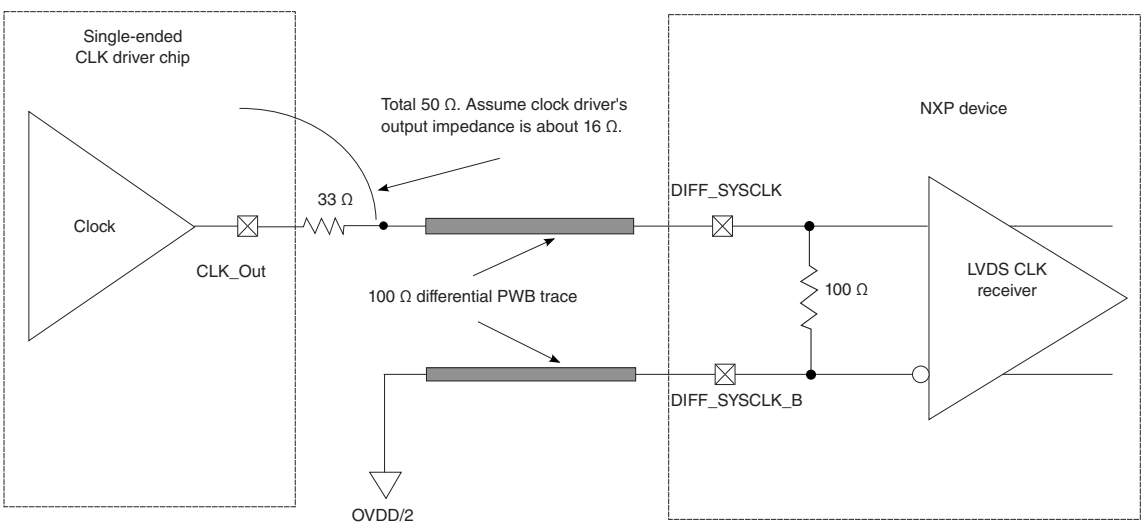



Figure 23. Interfacing with LVPECL clock driver (Reference only)	
Single-Ended Connection with Clock driver The DIFF_SYSCLK_B should be terminated to OVDD/2 	
Figure 24. Single ended connection (Reference only)	

6 Hardware design considerations

6.1 System clocking

This section describes the PLL configuration of the chip.

6.1.1 PLL characteristics

Characteristics of the chip's PLLs include the following:

- Core cluster CGA PLL1 generates a clock for all the cores and/or FMAN, from the externally supplied SYSCLK or LVDS generated (single ended) input.
- Core cluster CGA PLL2 generates a clock for all the cores and/or FMAN & eSDHC, from the externally supplied SYSCLK or LVDS generated (single ended) input.
- The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Platform to SYSCLK PLL ratio.
- The DDR block PLL generates an asynchronous DDR clock from the externally supplied DDRCLK input.
- The 4 lane SerDes blocks has two PLLs which generate a clock from their respective externally supplied SD1_REF_CLK*n*_P/SD1_REF_CLK*n*_N inputs. The frequency ratio is selected using the SerDes PLL RCW configuration bits as described in Valid reference clocks and PLL configurations for SerDes protocols .

6.1.2 Clock ranges

This table provides the clocking specifications for the processor core, platform, memory, and integrated flash controller.

Table 45. Processor, platform, and memory clocking specifications (V_{DD} = 0.9 V)

Characteristic	Maximum processor core frequency				Unit	Notes
	1000 MHz		1200 MHz			
	Min	Max	Min	Max		
Core cluster group PLL frequency	1000	1000	1000	1200	MHz	1
Platform clock frequency	256	300	256	300	MHz	1
Memory Bus Clock Frequency (DDR3L)	500	650	500	650	MHz	1, 2, 3
Memory Bus Clock Frequency (DDR4)	650	650	650	650	MHz	1, 3
IFC clock frequency	-	100	-	100	MHz	4
FMan	350	500	350	500	MHz	-

1. **Caution:**The platform clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.

2. The memory bus clock speed is half the DDR3L/DDR4 data rate. DDR3L memory bus clock frequency is limited to min = 1000 MT/s whereas DDR4 memory bus clock frequency is limited to min/max = 1300 MT/s.

3. The memory bus clock speed is dictated by its own PLL.

4. The integrated flash controller (IFC) clock speed on IFC_CLK[0:1] is determined by the IFC module input clock (platform clock / 2) divided by the IFC ratio programmed in CCR[CLKDIV]. See the chip reference manual for more information.

5. The minimum platform frequency should meet the requirements in Minimum platform frequency requirements for high-speed interfaces.

6. For supported voltage/frequency options, refer to orderable part list of QorIQ LS1043A and LS1023A Multicore Communications Processors at www.nxp.com

Table 46. Processor, platform, and memory clocking specifications (V_{DD} = 1.0 V)

Characteristic	Maximum processor core frequency								Unit	Notes
	1000 MHz		1200 MHz		1400 MHz		1600 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
Core cluster group PLL frequency	1000	1000	1000	1200	1000	1400	1000	1600	MHz	1
Platform clock frequency	256	300	256	300	256	300	256	400	MHz	1
Memory Bus Clock Frequency (DDR3L)	500	800	500	800	500	800	500	800	MHz	1, 2, 3
Memory Bus Clock Frequency (DDR4)	650	800	650	800	650	800	650	800	MHz	1, 3
IFC clock frequency	-	100	-	100	-	100	-	100	MHz	4
FMan	350	500	350	500	350	500	350	500	MHz	

1. **Caution:**The platform clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.

2. The memory bus clock speed is half the DDR3L/DDR4 data rate. DDR3L memory bus clock frequency is limited to min = 1000 MT/s whereas DDR4 memory bus clock frequency is limited to min = 1300 MT/s.

3. The memory bus clock speed is dictated by its own PLL.

4. The integrated flash controller (IFC) clock speed on IFC_CLK[0:1] is determined by the IFC module input clock (platform clock / 2) divided by the IFC ratio programmed in CCR[CLKDIV]. See the chip reference manual for more information.

5. The minimum platform frequency should meet the requirements in Minimum platform frequency requirements for high-speed interfaces.

6. For supported voltage/frequency options, refer to orderable part list of QorIQ LS1043A and LS1023A Multicore Communications Processors at www.nxp.com

6.1.2.1 DDR clock ranges

The DDR memory controller can run only in asynchronous mode, where the memory bus is clocked with the clock provided on the DDRCLK input pin, which has its own dedicated PLL.

This table provides the clocking specifications for the memory bus.

Table 47. Memory bus clocking specifications

Characteristic	Min Freq. (MHz)	Max Freq. (MHz)	Min Data Rate (MT/s)	Max Data Rate (MT/s)	Notes
Memory bus clock frequency and Data Rate for DDR3L	500	800	1000	1600	1, 2, 3
Memory bus clock frequency and Data Rate for DDR4	650	800	1300	1600	1, 2, 3

Notes:

1. **Caution:** The platform clock to SYSCLK ratio and core to platform clock ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform frequency do not exceed their respective maximum or minimum operating frequencies. See Platform to SYSCLK PLL ratio, and Core cluster to SYSCLK PLL ratio, and DDR controller PLL ratios, for ratio settings.

Table 47. Memory bus clocking specifications

Characteristic	Min Freq. (MHz)	Max Freq. (MHz)	Min Data Rate (MT/s)	Max Data Rate (MT/s)	Notes
2. The memory bus clock refers to the chip's memory controllers' Dn_MCK[0:1] and Dn_MCK[0:1]_B output clocks, running at half of the DDR data rate. 3. The memory bus clock speed is dictated by its own PLL. See DDR controller PLL ratios. 4. For supported voltage/frequency options, refer to orderable part list of QorIQ LS1043A and LS1023A Multicore Communications Processors at www.nxp.com					

6.1.3 Platform to SYSCLK PLL ratio

This table lists the allowed platform clock to SYSCLK ratios.

Because the DDR operates asynchronously, the memory-bus clock-frequency is decoupled from the platform bus frequency.

For all valid platform frequencies supported on this chip, set the RCW Configuration field SYS_PLL_CFG = 0b00.

Table 48. Platform to SYSCLK PLL ratios

Binary Value of SYS_PLL_RAT	Platform:SYSCLK Ratio
0_0011	3:1
0_0100	4:1
0_0101	5:1
0_0110	6:1
All Others	Reserved
Notes: 1. For supported voltage/frequency options, refer to orderable part list of QorIQ LS1043A and LS1023A Multicore Communications Processors at www.nxp.com.	

6.1.4 Core cluster to SYSCLK PLL ratio

The clock ratio between SYSCLK and each of the core cluster PLLs is determined by the binary value of the RCW Configuration field CG*m*_PLL*n*_RAT. This table describes the supported ratios. For all valid core cluster frequencies supported on this chip, set the RCW Configuration field CG*n*_PLL_CFG = 0b00.

This table below lists the supported asynchronous core cluster to SYSCLK ratios.

Table 49. Core cluster PLL to SYSCLK ratios

Binary value of CG*m*_PLL*n*_RAT	Core cluster:SYSCLK Ratio
00_1010	10:1
00_1011	11:1
00_1100	12:1
00_1101	13:1
00_1110	14:1

Table continues on the next page...

Table 49. Core cluster PLL to SYSCLK ratios (continued)

Binary value of CG*m*_PLL*n*_RAT	Core cluster:SYSCLK Ratio
00_1111	15:1
01_0000	16:1
01_0001	17:1
01_0010	18:1
01_0011	19:1
01_0100	20:1
01_0101	21:1
01_0110	22:1
01_0111	23:1
01_1000	24:1
01_1001	25:1
All others	Reserved
Notes:	
1. For supported voltage/frequency options, see the orderable part list of QorIQ LS1043A and LS1023A multicore communications processors at www.nxp.com.	

6.1.5 Core complex PLL select

The clock frequency of each core is determined by the binary value of the RCW Configuration field C1_PLL_SEL. The tables describe the selections available for each core, where each individual core can select a frequency from their respective tables.

Table 50. Core PLL select

Binary Value of C*1*_PLL_SEL	Core cluster ratio
0000	CGA PLL1 /1
0001	CGA PLL1 /2
0100	CGA PLL2 /1
0101	CGA PLL2 /2

6.1.6 DDR controller PLL ratios

DDR memory controller operates asynchronous to the platform.

In asynchronous DDR mode, the DDR data rate to DDRCLK ratios supported are listed in the following table. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT (bits 10-15).

The RCW Configuration field MEM_PLL_CFG (bits 8-9) must be set to MEM_PLL_CFG = 0b00 for all valid DDR PLL reference clock frequencies supported on this chip.

Table 51. DDR clock ratio

Binary value of MEM_PLL_RAT	DDR data-rate:DDRCLK ratio	Maximum supported DDR data-rate (MT/s)
00_1010	10:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
00_1011	11:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
00_1100	12:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
00_1101	13:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
00_1110	14:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
00_1111	15:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0000	16:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0001	17:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0010	18:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0011	19:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0100	20:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0101	21:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0110	22:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_0111	23:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
01_1000	24:1	The product of Input DDR Clock X Multiplication factor should range between 1000 MHz-1600MHz.
All Others	Reserved	-

Notes:

1. For supported voltage/frequency options, refer to orderable part list of QorIQ LS1043A and LS1023A Multicore Communications Processors at www.nxp.com.

6.1.7 Valid reference clocks and PLL configurations for SerDes protocols

Each supported SerDes protocol allows for a finite set of valid SerDes-related RCW fields and reference clock frequencies.

The clock ratio between each SerDes PLLs and their respective externally supplied SD1_REF_CLKn_P/SD1_REF_CLKn_N inputs is determined by a set of RCW configuration fields, SRDS_PRTCL_S1, SRDS_PLL_REF_CLK_SEL_S1, and SRDS_DIV_PEX as shown in this table.

Table 52. Valid SerDes RCW encodings and reference clocks

SerDes protocol (given lane)	Valid reference clock frequency	Valid setting for SRDS_PRTCL_S1	Valid setting for SRDS_PLL_REF_CLK_SEL_S1		Valid setting for SRDS_DIV_PEX
			PLL1	PLL2	
High Speed Serial interface					
PCI Express 2.5 Gbit/s (doesn't negotiate upwards)	100 MHz	Any PCIe	0: 100 MHz	0: 100 MHz	10: 2.5 G
	125 MHz		1: 125 MHz	1: 125 MHz	
PCI Express 5 Gbit/s (can negotiate up to 5 Gbit/s)	100 MHz	Any PCIe	0: 100 MHz	0: 100 MHz	01: 5 G
	125 MHz		1: 125 MHz	1: 125 MHz	
SATA (1.5, 3, 6 Gbit/s)	100 MHz	Any SATA	0: 100 MHz	-	Don't Care
	125 MHz		1: 125 MHz	-	
Networking interfaces					
SGMII (1.25 Gbit/s)	100 MHz	SGMII @ 1.25 Gbit/s	0: 100 MHz	0: 100 MHz	Don't Care
	125 MHz		1: 125 MHz	1: 125 MHz	
2.5 G SGMII (3.125 Gbit/s)	125 Mhz	SGMII @ 3.125 Gbit/s	0: 125 MHz	-	Don't Care
	156.25 MHz		1: 156.25 MHz	-	
QSGMII (5 Gbit/s)	100 MHz	Any QSGMII	0: 100 MHz	0: 100 MHz	Don't Care
	125 MHz		1: 125 MHz	1: 125 MHz	
XFI (10.3125 Gbit/s)	156.25 Mhz		1: 156.25 MHz	-	-
				-	
Notes: 1) A spread-spectrum reference clock is permitted for PCI Express. However, if any other high speed interface such as SGMII, QSGMII, SATA, or Debug is used concurrently on the same SerDes bank, spread-spectrum clocking is not permitted. 2) SerDes lanes configured as SATA initially operate at 3.0 Gbit/s. 1.5 Gbit/s operation may later be enabled through the SATA IP itself. It is possible for software to set each SATA at different rates.					

6.1.8 Frequency options

This section discusses interface frequency options.

6.1.8.1 SYSCLK and core cluster frequency options

This table shows the expected frequency options for SYSCLK and core cluster frequencies.

Table 53. SYSCLK and core cluster frequency[1]

Core cluster: SYSCLK Ratio	SYSCLK (MHz)		
	64.00	66.67	100.00
	Core cluster Frequency - (MHz)[1]		
10:1			1000
11:1			1100

Table continues on the next page...

Table 53. SYSCLK and core cluster frequency[1] (continued)

Core cluster: SYSCLK Ratio	SYSCLK (MHz)		
	64.00	66.67	100.00
	Core cluster Frequency - (MHz)[1]		
12:1			1200
13:1			1300
14:1			1400
15:1		1000	1500
16:1	1024	1067	1600
17:1	1088	1133	
18:1	1152	1200	
19:1	1216	1267	
20:1	1280	1333	
21:1	1344	1400	
22:1	1408	1467	
23:1	1472	1533	
24:1	1536	1600	
25:1	1600		

Notes:

1. Core cluster output is the operating frequency of the core.

2. Core cluster frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed)

3. When using Single Source clocking only 100 MHz input is available.

4. For supported voltage/frequency options, see the orderable part list of QorIQ LS1043A and LS1023A Multicore Communications Processors at www.nxp.com.

6.1.8.2 SYSCLK and platform frequency options

This table shows the expected frequency options for SYSCLK and platform frequencies.

Table 54. SYSCLK and platform frequency options

Platform: SYSCLK Ratio	SYSCLK (MHz)		
	64.00	66.67	100.00
	Platform Frequency (MHz)[1]		
3:1			300
4:1	256	267	400
5:1	320	333	
6:1	384	400	

Notes:

1. Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed)

2. When using Single source clocking, only 100 MHz options are valid

3. For supported voltage/frequency options, see the orderable part list of QorIQ LS1043A and LS1023A Multicore Communications Processors at www.nxp.com.

6.1.8.3 DDRCLK and DDR data rate frequency options

This table shows the expected frequency options for DDRCLK and DDR data rate frequencies.

Table 55. DDRCLK and DDR data rate frequency options

DDR data rate: DDRCLK Ratio	DDRCLK (MHz)		
	64.00	66.67	100.00
	DDR Data Rate (MT/s)[1]		
10:1			1000
11:1			1100
12:1			1200
13:1			1300
14:1			1400
15:1		1000	1500
16:1	1024	1067	1600
17:1	1088	1133	
18:1	1152	1200	
19:1	1216	1266	
20:1	1280	1333	
21:1	1344	1400	
22:1	1408	1466	
23:1	1472	1533	
24:1	1536	1600	

Notes:

1. DDR data rate values are shown rounded up to the nearest whole number (decimal place accuracy removed)
2. When using Single Source clocking, only 100 MHz options are available.
3. Minimum Frequency supported by DDR4 is 1300 MT/s. DDR3 supports a minimum of 1000 MT/s.
4. For supported voltage/frequency options, see the orderable part list of QorIQ LS1043A and LS1023A Multicore Communications Processors at www.nxp.com.

6.1.8.4 SYSCLK and eSDHC high speed modes frequency options

This table shows the frequency multiplier options for SYSCLK when eSDHC operates in High Speed modes (>=52 MHz). For low frequency options CGA PLL2 is bypassed and eSDHC receives platform clock directly.

Table 56. SYSCLK multiplier/frequency options when eSDHC operates in High Speed mode (clocked by CGA PLL2 / 1)

Core cluster: SYSCLK Ratio	SYSCLK (MHz)		
	64.00	66.67	100.00
	Resultant Frequency (MHz)[1]		
12:1			1200

Table continues on the next page...

Table 56. SYSCLK multiplier/frequency options when eSDHC operates in High Speed mode (clocked by CGA PLL2 / 1) (continued)

Core cluster: SYSCLK Ratio	SYSCLK (MHz)		
	64.00	66.67	100.00
	Resultant Frequency (MHz)[1]		
18:1	1152	1200	

Notes:

1. Resultant frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed)
2. For Low speed operation, eSDHC is clocked from Platform PLL and does not use CGA PLL2.

6.1.8.5 Minimum platform frequency requirements for high-speed interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below.

For proper PCI Express operation, the platform clock frequency must be greater than or equal to:

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{16}$$

Figure 25. Gen 1 PEX minimum platform frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

Figure 26. Gen 2 PEX minimum platform frequency

See section "Link Width," in the chip reference manual for PCI Express interface width details. Note that "PCI Express link width" in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection. It refers to the widest port in use, not the combined width of the number ports in use.

7 Thermal

This section discusses the thermal model and management of the chip.

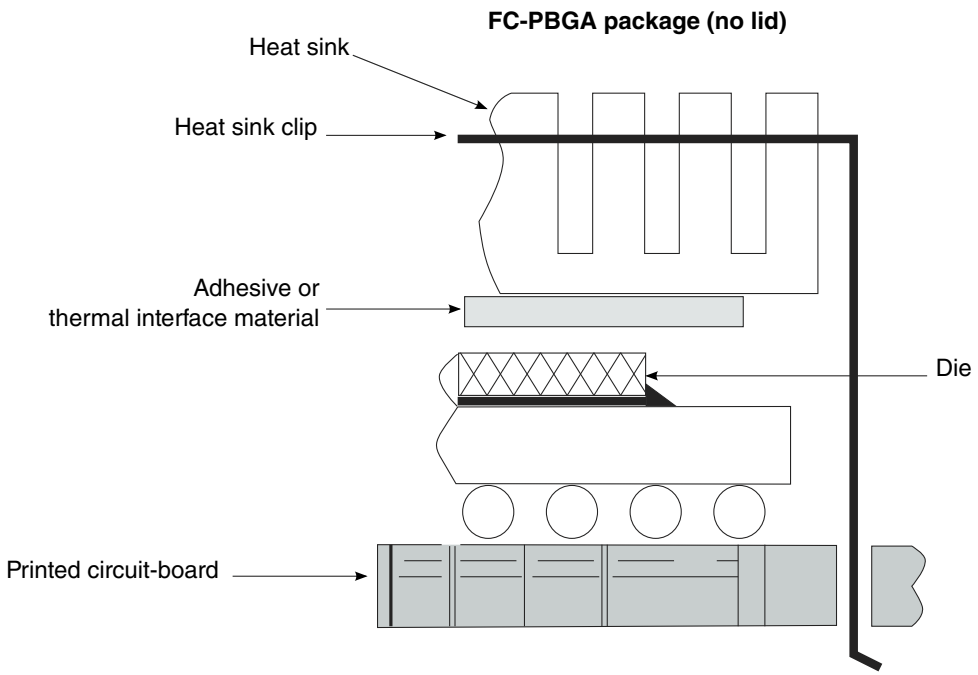
7.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.

7.2 Thermal system-level recommendations

Proper thermal control design is primarily dependent on the system-level design — the heat sink, airflow, and thermal interface material.

Table 57. Thermal system-level checklist

Item	Completed
Use the recommended thermal model. Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.	
Use this recommended board attachment method to the heat sink:[1] The processor heat sink must be connected to GND at one point for EMC performance. GND here specifies processor ground.  **Figure 27. Cross-secitonal view of FC PBGA with no lid**	
Ensure the heat sink is attached to the printed-circuit board with the spring force centered over the package.[2]	
Ensure the spring force does not exceed 15 pounds force (65 Newtons).	
A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance.[3]	
Ensure the method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board.	
A thermal simulation is required to determine the performance in the application.[4]	

Notes:

1. The system board designer can choose among several types of commercially available heat sinks to determine the appropriate one to place on the device. Ultimately, the final selection of an appropriate heat sink depends on factors such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

2. The performance of the thermal interface materials improves with increased contact pressure; the thermal interface vendor generally provides a performance characteristic to guide improved performance.

3. The system board designer can choose among several types of commercially available thermal interface materials.

Table 57. Thermal system-level checklist

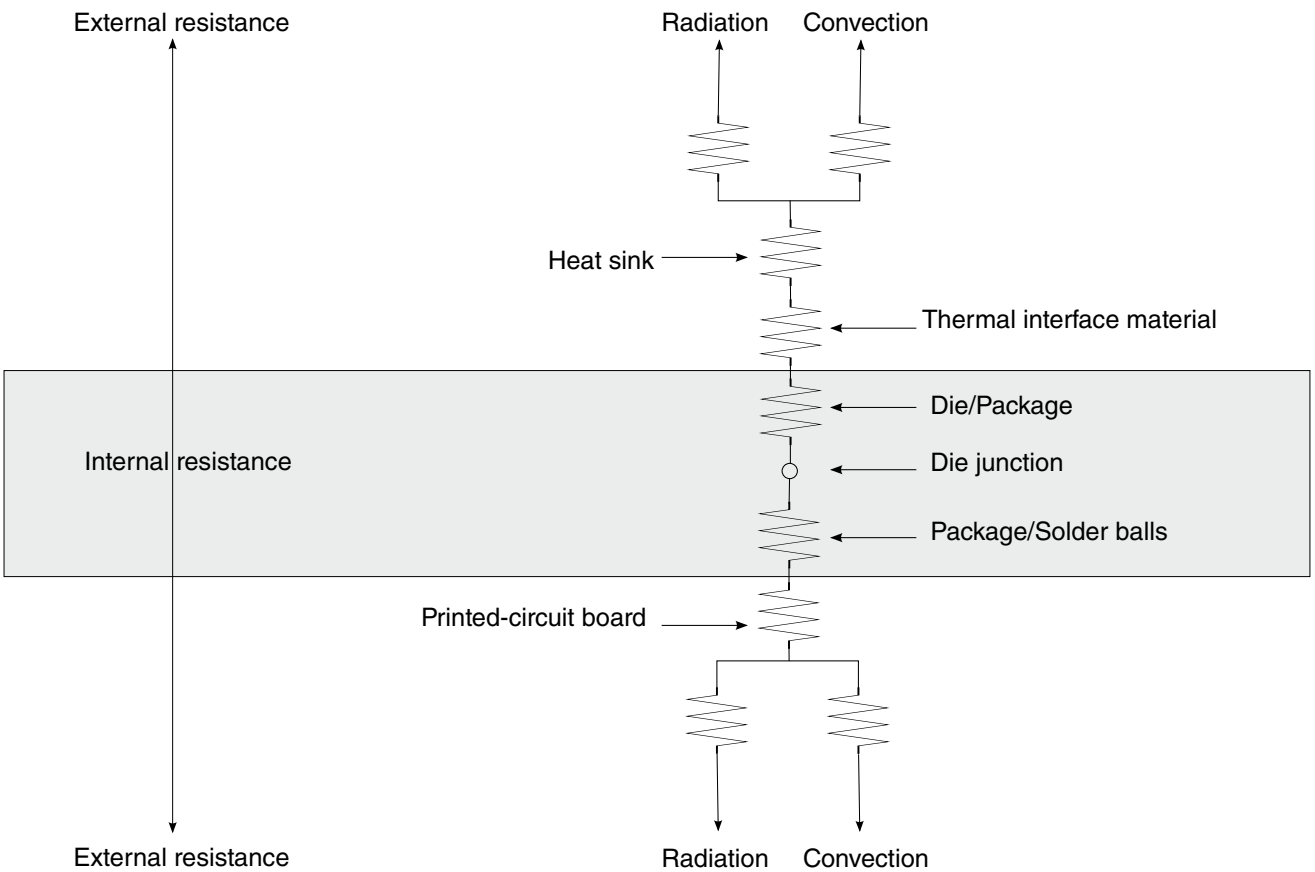
Item	Completed
4. A Flotherm model of the part is available.	

7.3 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

This figure shows the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 28. Package with heat sink mounted to a printed-circuit board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

8 Revision history

This table summarizes changes to this document.

Table 58. Revision history

Revision	Date	Change

5	05/2020	• Added general description for unused pins of different interfaces in Interface recommendations
		• In Ethernet controller pin termination recommendations
		  • Updated description for unused pins
		  • Added "The unused clock pin should be pulled to GND." in note 1
		• Added note 3 regarding the IFC_A26 and IFC_A27 pin termination in QSPI pin termination recommendations

4	11/2019	• Added "QorIQ" in the main heading
		• Changed "ARM" as "Arm"
		• Updated Core Reference Manual information in Recommended resources
		• Removed Signal type column, updated format and added note for USB power supplies in Power pin recommendations
		• In Core and platform supply voltage filtering, updated "as defined per datasheet" to "based on maximum power in the datasheet" of Power system-level recommendations
		• Updated sentence to "USB_SVDD and USB_SDVDD must be provided by the VDD power supply." in Power system-level recommendations
		• In Power-on reset recommendations
		  • Replaced "PLL configuration inputs must meet a 100 µs set-up time to HRESET_B" with "other than cfg_eng_use0"
		  • Added "1ms after V_{DD} ramps up during PORESET_B assertion"
		  • Corrected "configuration signals to the chip when HRESET_B is asserted" to "configuration signals to the chip when PORESET_B is asserted"
		• In Configuration signals sampled at reset
		  • Updated information regarding LS1043A datasheet
		  • Provided JTAG configuration files path
		  • Removed "It is recommened to keep provision for optional pull-down resistor on board." from cfg_eng_use2
		• In Hard-Coded RCW
		  • Added 0x9F hard-coded RCW option
		  • Updated note regarding DDR CLK reference clock when 0x9A, 0x9E or 0x9F hard-coded RCW option is selected
		  • Added note for referring AN12081
		  • Corrected typo "HRESET_REQ_B" to "RESET_REQ_B"
		• In DDR4 and DDR3L SDRAM interface pin termination recommendations
		  • Updated description for not used D1_MCK pins
		  • Added description for MALERT_B pin when discrete DRAM is used
		  • Removed RDIMM information as DDR3L and DDR4 RDIMMs are not supported
		  • Changed name from D1_MAPAR to D1_MAPAR_OUT
		  • Changed IO type of D1_MVREF from I to IO
		  • Added note for case when discrete DDR4 DRAM is used with two chip selects
		• In DDR system-level recommendations
		  • Added CKE termination requirement during self refresh
		  • Updated note 2 as "DDR3L and DDR4 RDIMMs are not supported."
		• In IFC pin termination recommendations
		  • Changed IO type of IFC_PERR_B from O to I
		  • Updated description for not used IFC_PERR_B pins
		  • Changed IFC_RB[0:1]_B to IFC_RB[0:3]_B

Table continues on the next page...

Table 58. Revision history

Revision	Date	Change

		• Updated description for not used UART[1:4]_SIN pins in DUART pin termination recommendations
		• In LPUART pin termination recommendations
		  • Removed *_BASE RCW fields for determining functionality of LPUART signals
		  • Updated description for not used LPUART pins
		• In I2C pin termination recommendations
		  • Updated description for not used IIC pins except IIC1_SDA and IIC1_SCL
		  • Corrected typo in description of used IIC3/4* pins
		• In eSDHC pin termination recommendations
		  • Added RCW[SDHC_EXT] field for determining functionality of SDHC_CMD, SDHC_CLK and SDHC_DATA[0:3] pins
		  • Added RCW[SPI_EXT] field for determining functionality of SDHC_DATA[4:7] pins
		  • Removed RCW[SPI_BASE] field for determining functionality of SDHC_VS and SDHC_CLK_SYNC_IN/OUT pins
		  • Added note 6 for reset of SD card when working on UHS-I speed mode
		  • Added note 7 for availability of SDHC signals when booting from QSPI
		• Removed output power line from Dual voltage regulator to SD card in Figure 14
		• Removed note "Voltage translator requirment depends upon the chosen eMMC voltage and OVDD/EVDD voltage configuration" from Table 17
		• In GIC pin termination recommendations
		  • Updated description for not used IRQ pins
		  • Removed IRQ_OUT_B signal
		  • Added note for polarity of IRQ signals
		• Corrected typo "resistance" to "resistor" in Trust pin termination recommendations
		• Updated description for ASLEEP pin in Power Management pin termination recommendations
		• In Debug and reserved pin termination recommendations
		  • Added debug analog signals
		  • Updated description for EVT pins
		  • Updated description for JTAG_BSR_VSEL and TBSCAN_EN_B
		• Removed section "Analog Signals pin termination recommendations"
		• In SerDes pin termination recommendations
		  • Removed "PLL1 can support 100, 125 and 156.25 MHz, whereas PLL2 can only support 100 and 125 MHz. Therefore, XFI and 2.5 G SGMII 5 which require 156.25 MHz can only be supported by PLL1."
		  • Removed "PLL2 supports only 100 and 125 MHz frequency therefore the support is limited to PCIe, SGMII and QSGMII."
		  • Removed note "2.5 G SGMII requires 125 or 156.25 MHz to operate."
		  • Added note for SerDes lanes termination
		• Updated description of SCFG_USBPWRFAULT_SELCR for USB_PWRFAULT pins in USB PHY pin termination recommendations
		• Added notes regarding pull-up resistor when MDC and MDIO are configured as open-drain mode in Ethernet Management Interface 1/2 pin termination recommendations
		• In Ethernet controller pin termination recommendations
		  • Added note "Either of the EC1_GTX_CLK125 or EC2_GTX_CLK125 can be used to clock both the EC interfaces in RGMII mode. The selection is through SCFG_ECGTXCMCR[CLKSEL]."
		  • Updated description for not used EC1_GTX_CLK and EC2_GTX_CLK pins
		• In QSPI pin termination recommendations
		  • Added note "QSPI signals are multiplexed with IFC signals and only select lines are available on IFC when QSPI is used."
		  • Added note on chip select "To avoid glitches or noise on chip select, it is recommended to use series resistor of 22Ω to 68Ω along with a 20pf capacitor to GND. The capacitor should be placed close to the receiver."
		• Added note for SPI_CLK availability in SPI pin termination recommendations

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Table 58. Revision history (continued)

Revision	Date	Change
		• Updated IO type of GPIO1_13 from IO to O in General Purpose Input/Output pin termination recommendations • Added note regarding clock selection of EC interface in Clock pin termination recommendations • Updated value from "reserved" to "don't care" for IFC_WP_B[0] in *Single Oscillator Source* clock select
3	03/2017	In Table 42, updated RTC "Note used" column for WDOG functionality.
2	01/2017	• Updated PROG_MTR, FA_VL and SENSEVDD, SENSEGND description Power pin recommendations • Updated Core and platform supply voltage filtering in Power system-level recommendations • Added SVR for silicon rev 1.1 in Product revisions • Updated description for SDHC_WP in eSDHC pin termination recommendations • Updated JTAG_BSR_VSEL and TBSCAN_EN_B description in Debug and reserved pin termination recommendations
1	06/2016	• Added footnote in DDR4 and DDR3L SDRAM interface pin termination recommendations • Updated comments for CKSTP_OUT_B in Debug and reserved pin termination recommendations • Updated comments for TA_BB_RTC, TA_BB_TMP_DETECT_B and TA_TMP_DETECT_B in Trust pin termination recommendations • Replaced Freescale instances with NXP in Before you begin, Table 1, Table 44, and Recommended thermal model sections • In the section Recommended resources, added more document references and updated the name, ID, and location for the existing documents • Corrected product revision for LS1023A and added references for 23x23 package in Product revisions • Added description of PROG_MTR, FA_VL, TA_BB_VDD, updated USB supplies state (when unused) and updated SENSEVDD, SENSEGND description (when used) in Power pin recommendations • PoR sequence referred to Design checklist to avoid duplication Power-on reset recommendations • Removed even ration limitation from SYS_PLL_RAT from Hardcoded RCW in Configuration signals sampled at reset • Added DDR4 reference D1_MALERT_B with DDR3 reference D1_MAPAR_ERR_B in DDR controller pin termination recommendations • Updated connectivity diagram in figure 6 in DDR50 mode and updated SDHC_DAT[0:3] cooments in eSDHC system-level recommendations • Updated mux selection for UC1 and UC3 in QUICC Engine pin termination recommendations • Removed QSPI-DQS references in QSPI pin termination recommendations • Corrected typo in Clock pin termination recommendations • Updated description for GPIO_2[13:15] and GPIO_2[25:27] General Purpose Input/Output pin termination recommendations • Updated single oscillator clock sourcing diagram in *Single Oscillator Source* clock select • Removed figures using external translator in DS and HS modes, SDR12, 25, 104 and DDR50 modes, DDR mode in eSDHC system-level recommendations • Corrected typos in Global Interrupt Controller (GIC) recommendations • Updated text in SerDes pin termination recommendations • Added reference for 23x23 package in SPI pin termination recommendations • Updated power-up sequence time in Power system-level recommendations • Updated foot note for selecting DIFF_SYSCLK as DDRCLK Clock pin termination recommendations • Added note related to MDC/MDIO loading at 10 MHz in Ethernet Management Interface 1/2 pin termination recommendations • Updated max current slew rate in Power system-level recommendations • Added SerDes block level power supply decoupling recommendations in SerDes block power supply decoupling recommendations

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Table 58. Revision history (continued)

Revision	Date	Change
		• Updated power system level recommendations in Power system-level recommendations • Added note for hard-coded RCW in Configuration signals sampled at reset • Distributed "Configureation singals sampled at rest" and "Hard Coded RCW" into two different sub-headings • Added EC1/2_TX_EN pull-down recommendations in Ethernet controller pin termination recommendations • Removed duplication of information related to D1_MVREF from Analog Signals pin termination recommendations • Moved analog pin information from Debug and reserved pin termination recommendations to Analog Signals pin termination recommendations • Updated note 1 in System control pin termination recommendations
0	03/2016	Initial release

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