NXP Semiconductors
Application Note

Document Number: AN5113
Rev. 1.0, 7/2016

Powering an i.MX 6SL based system using the PF3000 PMIC

1 Introduction

The PF3000 is a SMARTMOS highly integrated Power Management IC, ideally suited to power NXP's i.MX 6SL, i.MX 6S, i.MX 6DL, and the i.MX 7 series of application processors. This application note discusses the power tree configuration for powering an i.MX6SL based system using the PF3000.

Contents

2 PF3000 voltage regulators

Table 1. shows a summary of the voltage regulators in the PF3000. Output voltage and startup sequence of the regulators is programmed into the PMIC through One Time Programmable (OTP) memory. For more details refer to the product datasheet.

Table 1. PF3000 voltage regulators

Regulator	Output voltage range	Load current rating
SW1A	0.7 V to 1.425 V; 1.8 V; 3.3 V	1000 mA
SW1B	0.7 V to 1.475 V	1750 mA
SW2	1.5 V to 1.85 V; 2.5 V to 3.3 V	1250 mA
SW3	0.9 V to 1.65 V	1500 mA
SWBST	5.0 V to 5.15 V	600 mA
VSNVS	3.0 V	1.0 mA
VLDO1	1.8 V to 3.3 V	100 mA
VLDO2	0.8 V to 1.55 V	250 mA
VLDO3	1.8 V to 3.3 V	100 mA
VLDO4	1.8 V to 3.3 V	350 mA
VCC_SD	1.8 V to 1.85 V; 2.85 V to 3.3 V	100 mA
V33	2.85 V to 3.3 V	350 mA
VREFDDR	VINREFDDR/2	10 mA

3 i.MX 6SL power management using the PF3000

The i.MX 6SL processor features NXP's advanced implementation of the a single ARM® Cortex®-A9 MPCore™ multicore processor, which operates at speeds up to 1.0 GHz. Table 2. shows how PF3000 can be used to power an i.MX 6SL based system. This include the voltage rails required by the processor as well as memory and common peripherals. Being a programming PMIC, the PF3000 can be used in a number of ways to power the i.MX 6SL. Table 2. lists one of the many possibilities. Based on end application requirements, the power tree can be optimized. Contact your NXP representative for a BSP patch for the PF3000 with i.MX 6SL.

Table 2. PF3000 + i.MX 6SL power tree

Regulator	Voltage	Sequence	Load domain
SW1A	1.375	1	VDDCORE
SW1B	1.375	1	VDDSOC
SW2	3.15	2	VDDHIGH, VCC-eMCC, VCCQ-eMMC, MIC_VDD, EPDC Expansion Port, LCD Expansion Port, Mini-PCIe HMC, Debug UART to USB, Ethernet Transceiver, VCC_SPI_NOR_Flash
SW3	1.2	4	DRAM_PWR, VDD2_LPDDR2, NVCC_1.2V
SWBST	5.0	6	SYS_5V (OTG/Host, EPDC Expansion, LCD Expansion)
VSNVS	3.0	Always On	VDD_SNVS_IN
VLDO1	1.8	3	VDD1_LPDDR2, Audio Codec
VLDO2	1.5	Off	CMOS Camera, EPDC Expansion port,
VLDO3	3.0	Off	N/A
VLDO4	1.8	3	NVCC_1.8V, EPDC Expansion Port, LCD Expansion Port, WEIM Expansion
VCC_SD	3.15	2	VCC_SD1, VDD-SD2, VDD-SD3
V33	2.85	Off	CMOS Camera
VREFDDR	0.6	4	DRAM_VREF

4 Schematic

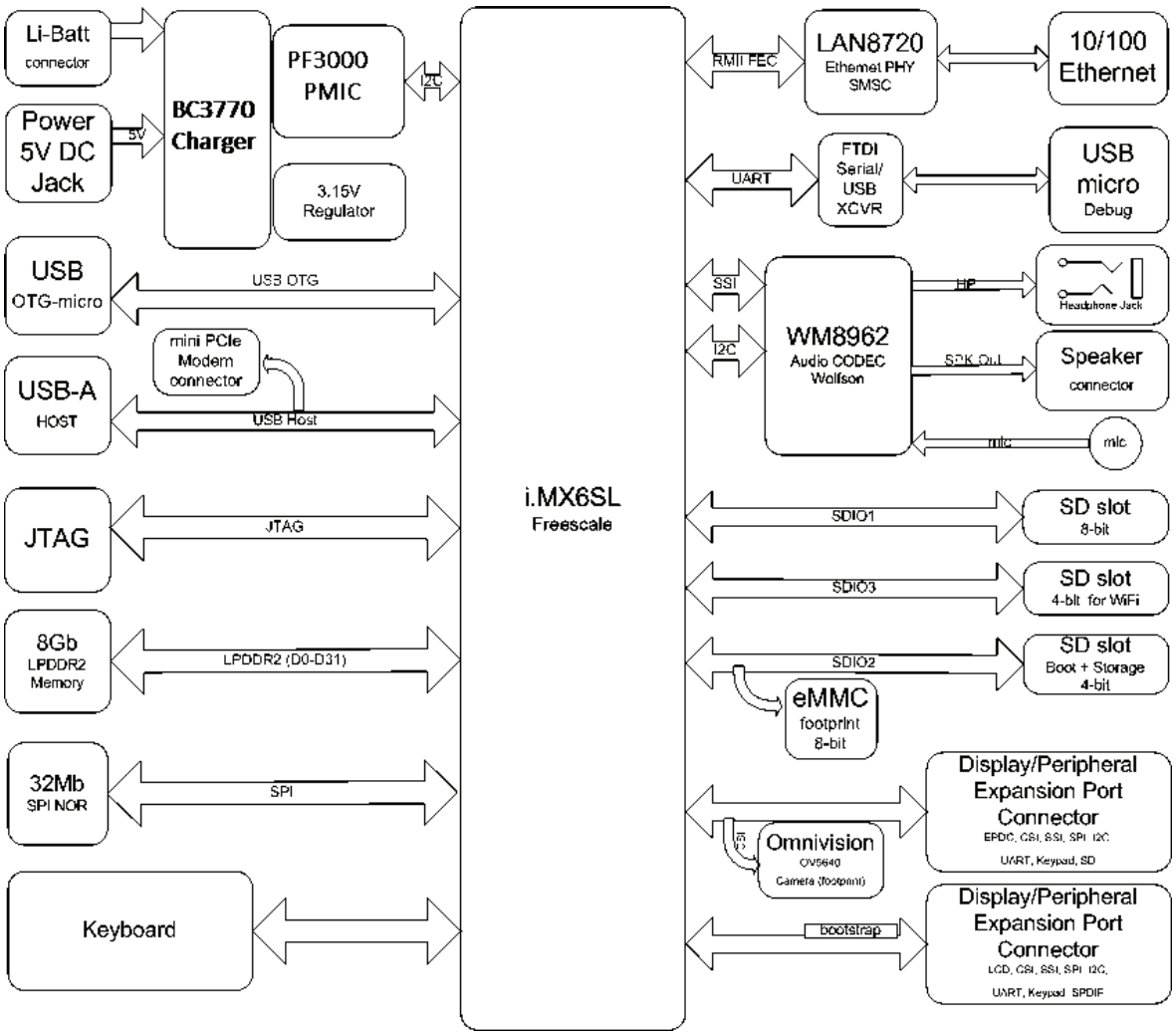
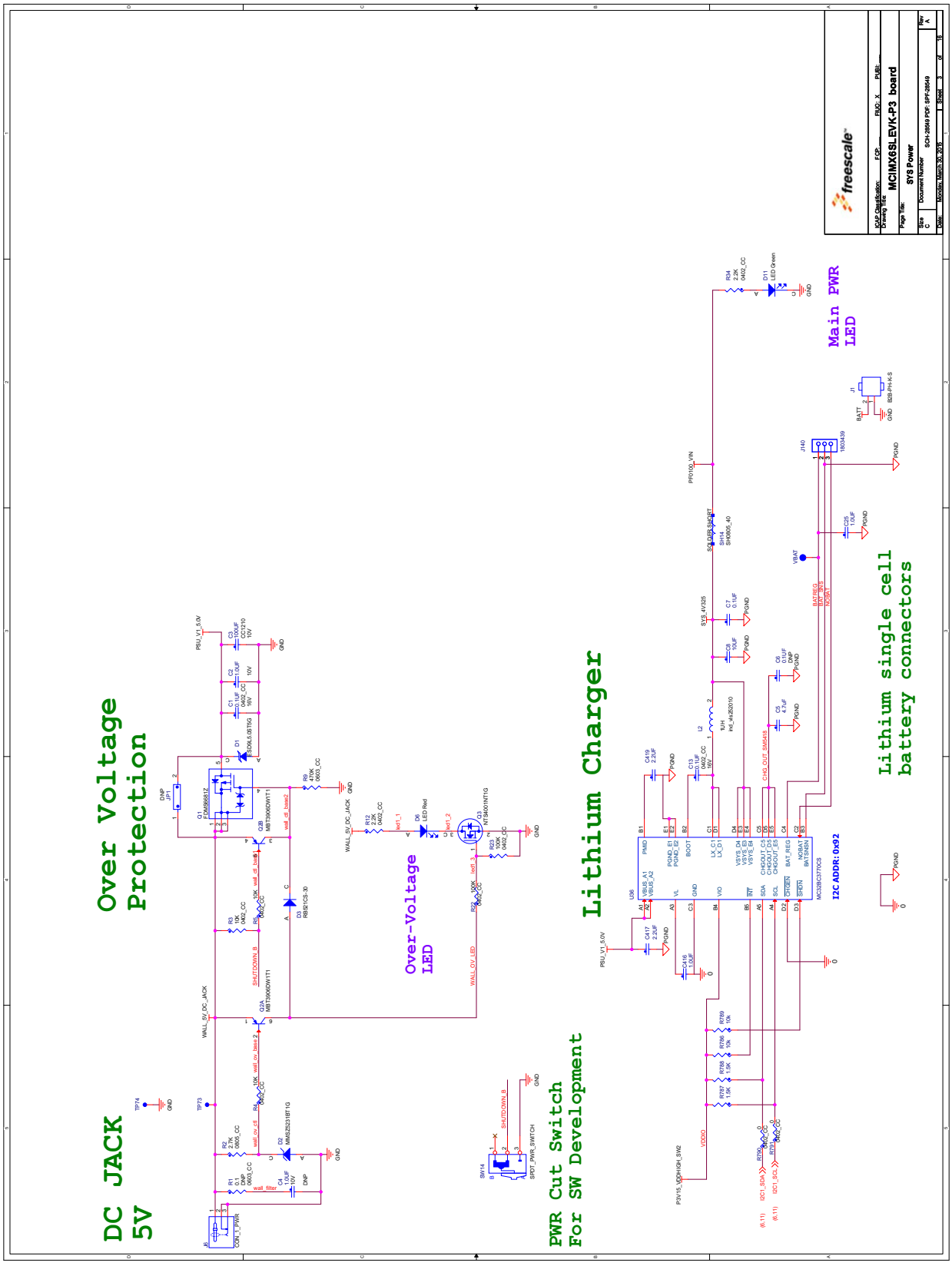
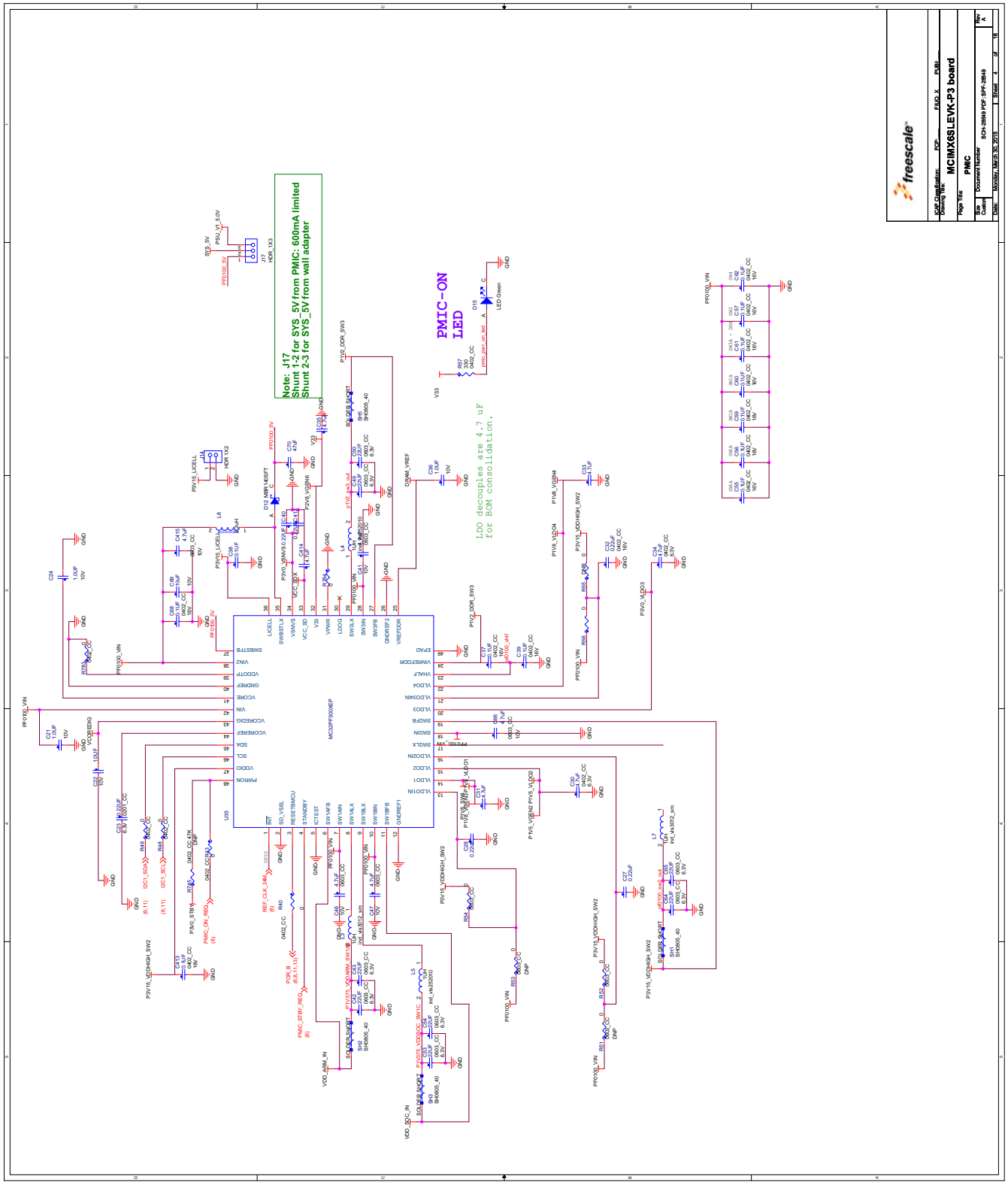
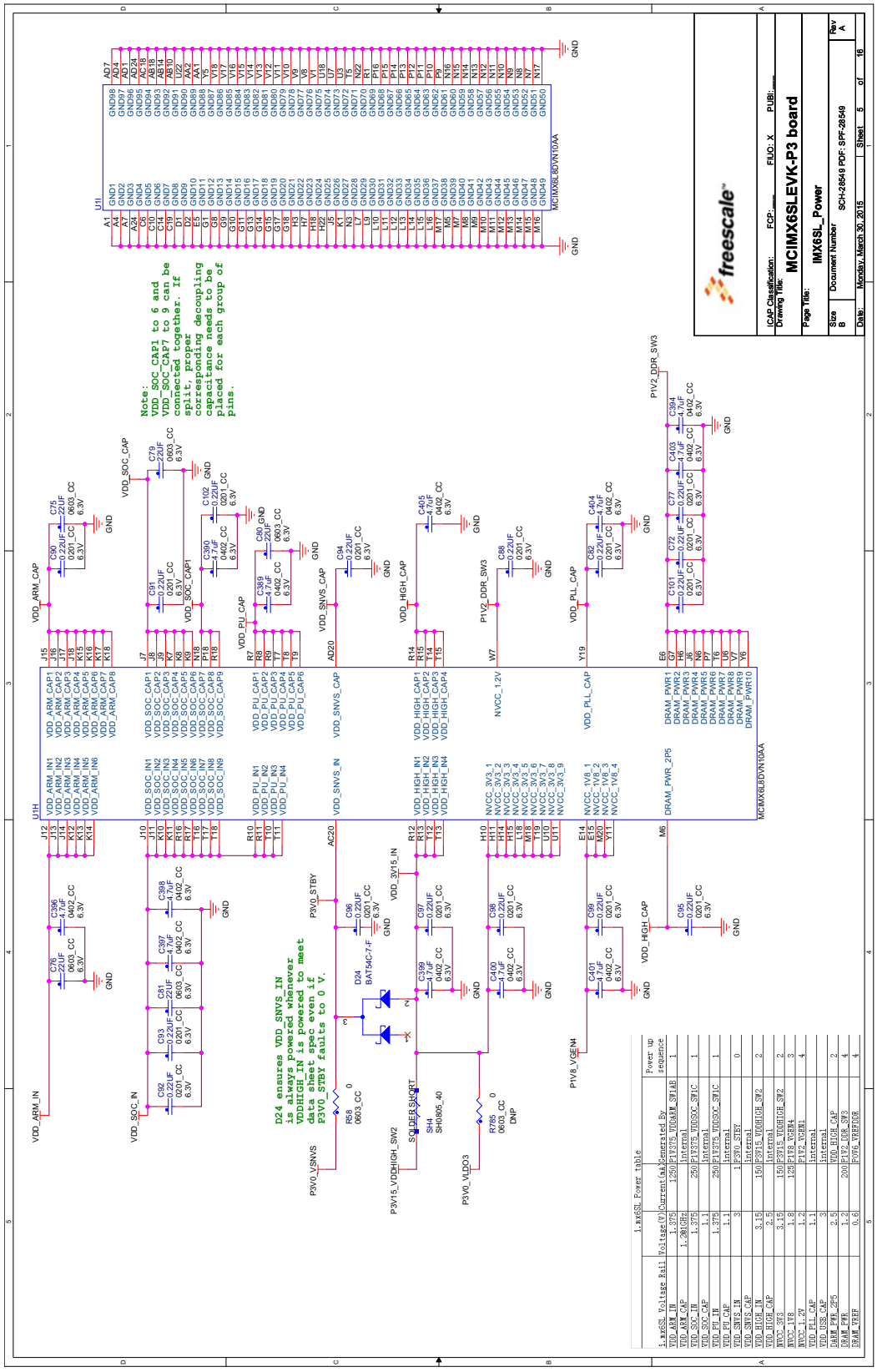
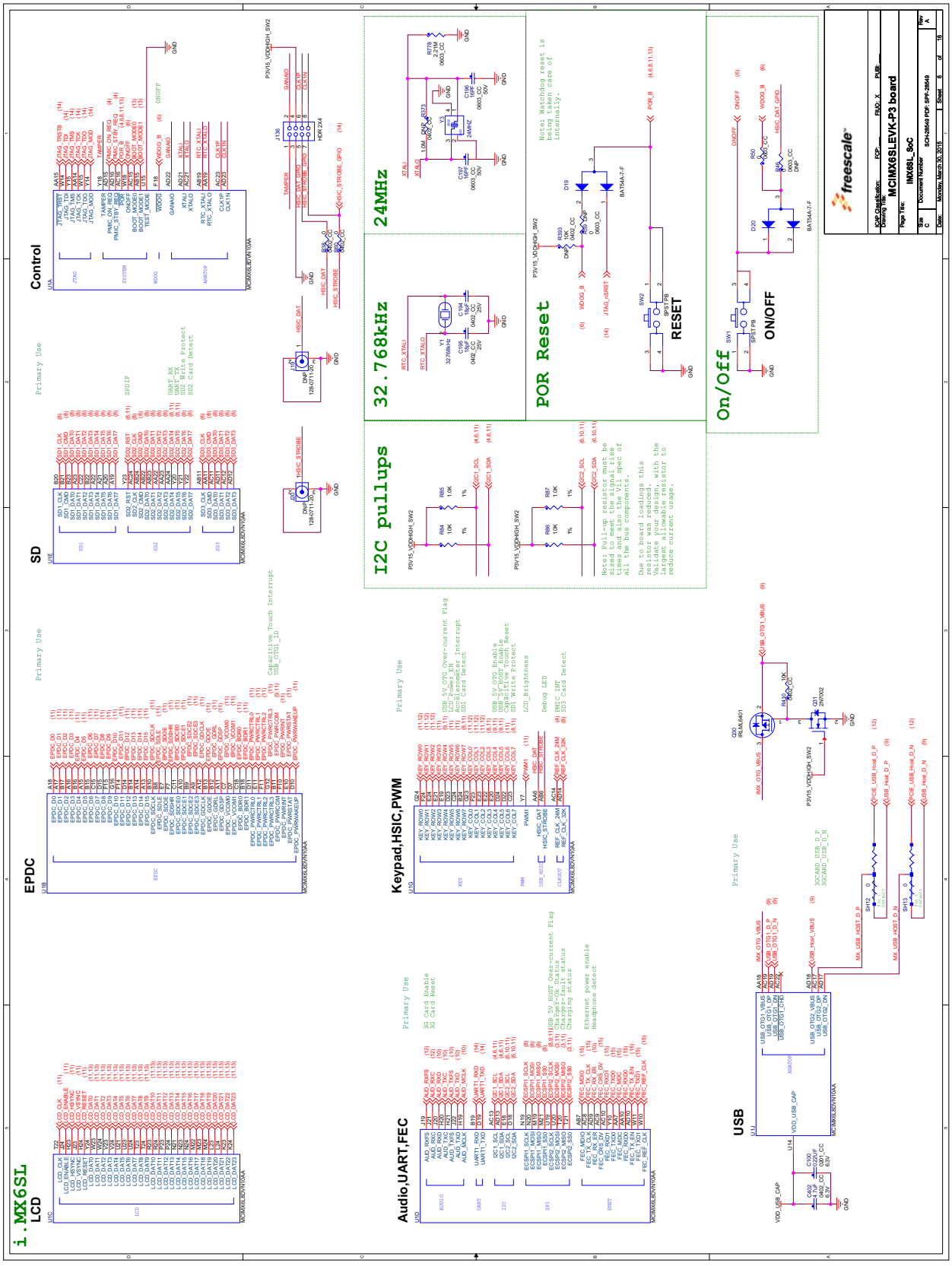


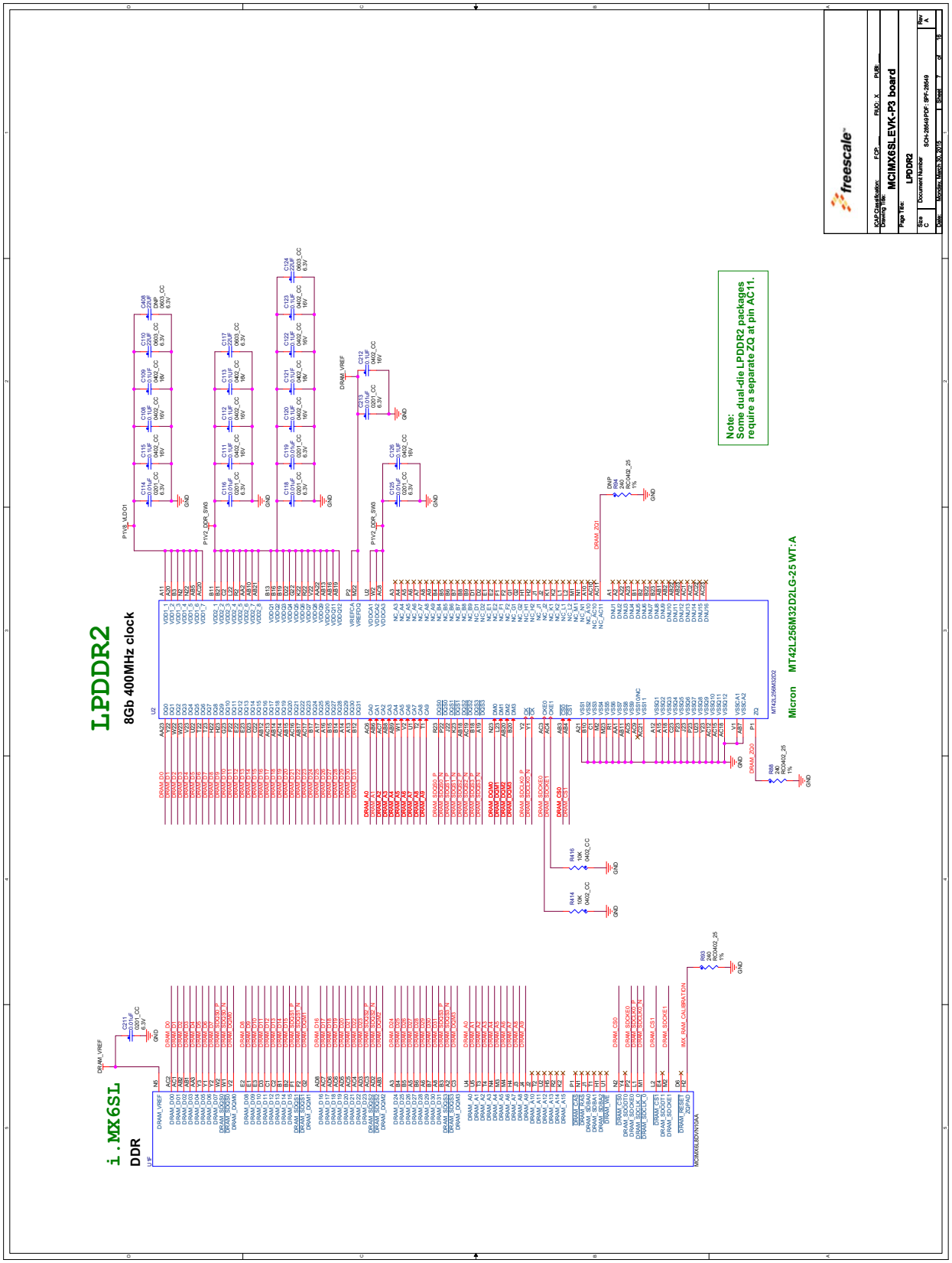
Figure 1. MCIMX6SLEVK-P3 board diagram

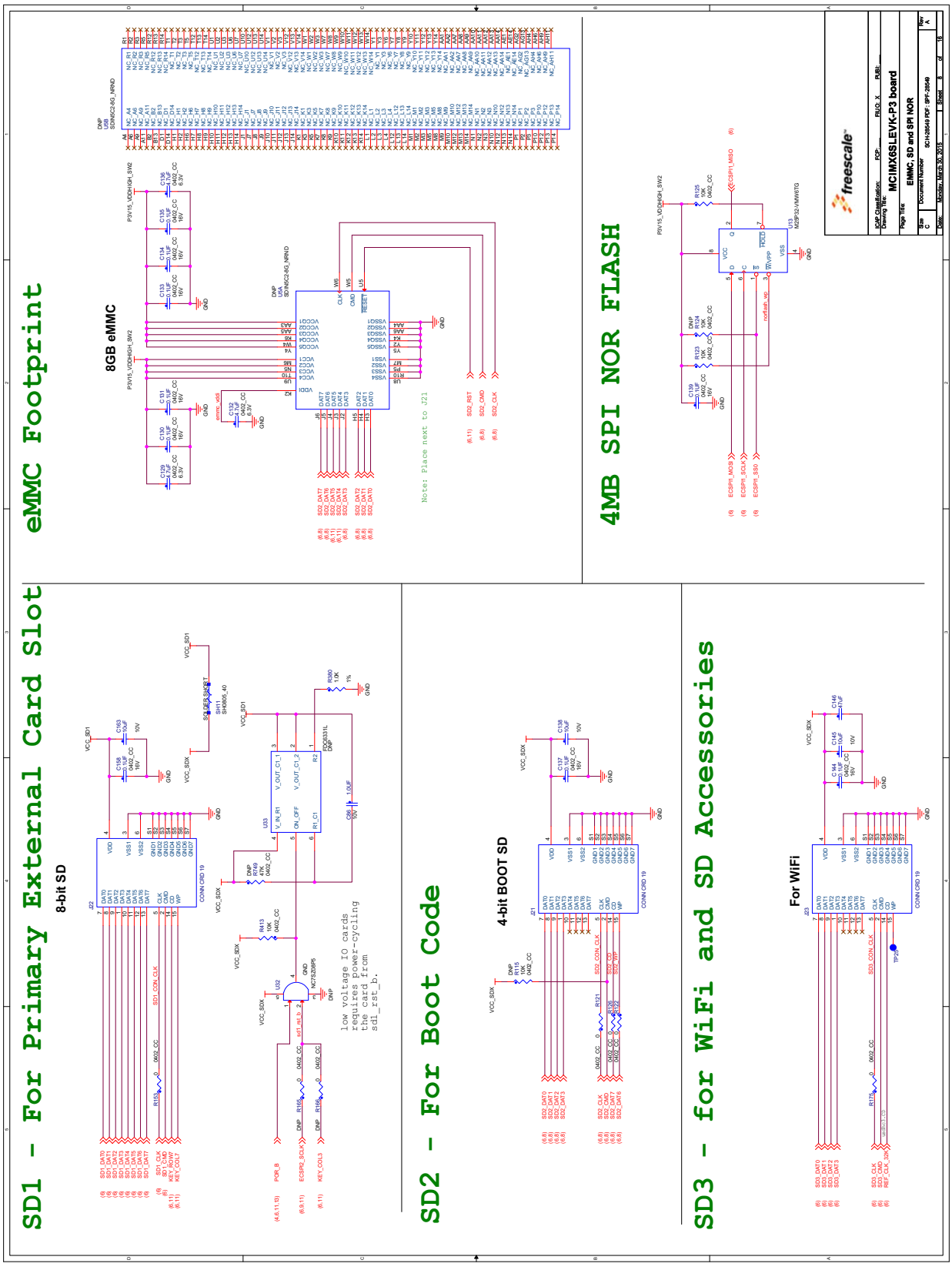

DC JACK
5V
Over Voltage
Protection
Over-Voltage
LED
PWR Cut Switch
For SW Development
Lithium Charger
Main PWR
LED
Lithium single cell
battery connectors
I2C ADDR: 0x92
freescale
MCIMX6SLEVK-P3 board
SY3 Power

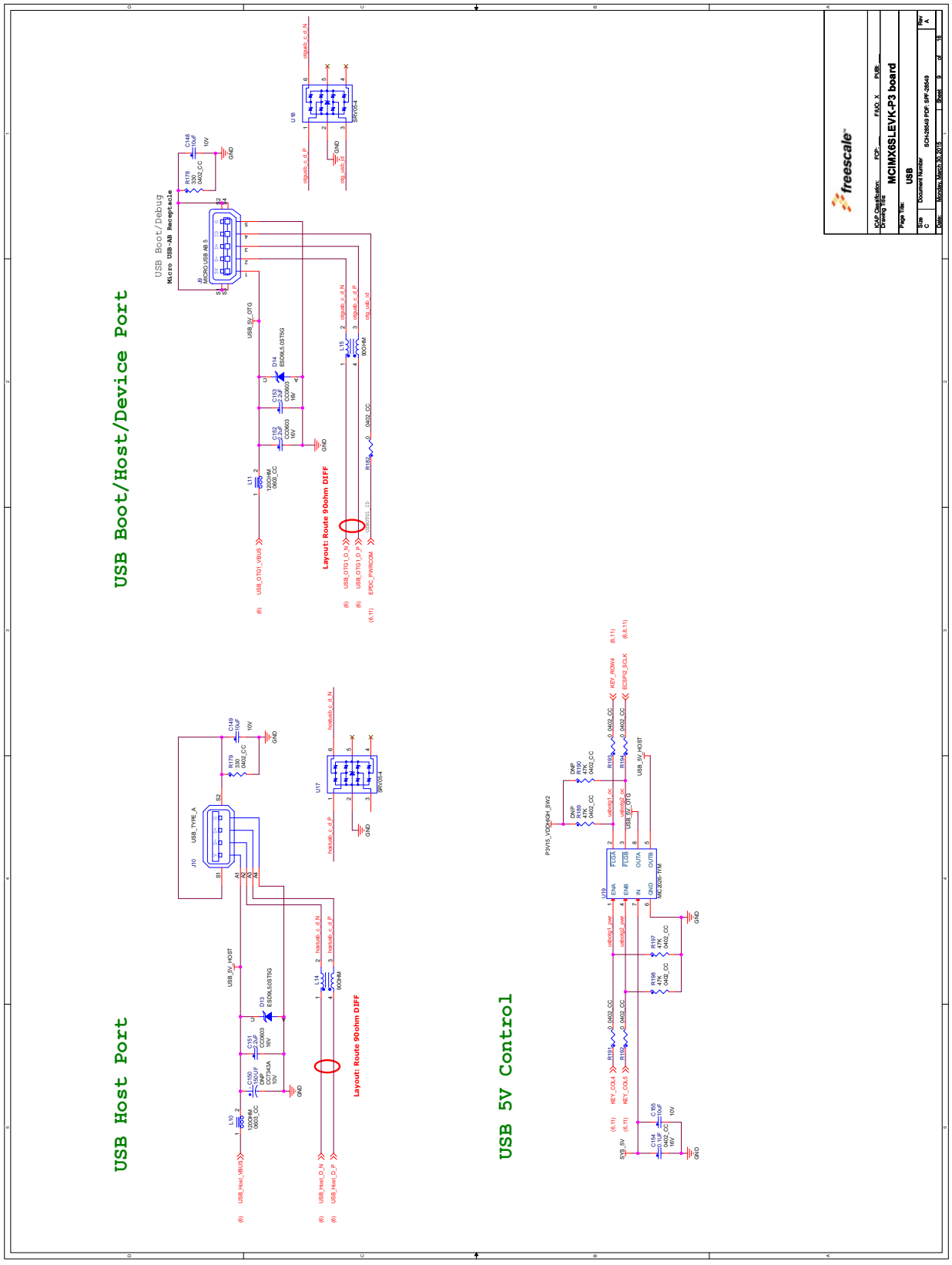

Note: J17
Shunt 1-2 for SYS_5V from PMIC; 600mA limited
Shunt 2-3 for SYS_5V from wall adapter
PMIC-ON
LED
LDO decouples are 4.7 uF
for BOM consolidation.
MC32PF3000AEP
freescale
MCIMX6SLEVK-P3 board
PMIC
SCH-28949 PDF-28949
Rev A
Monday, March 30, 2015
Sheet 4 of 16

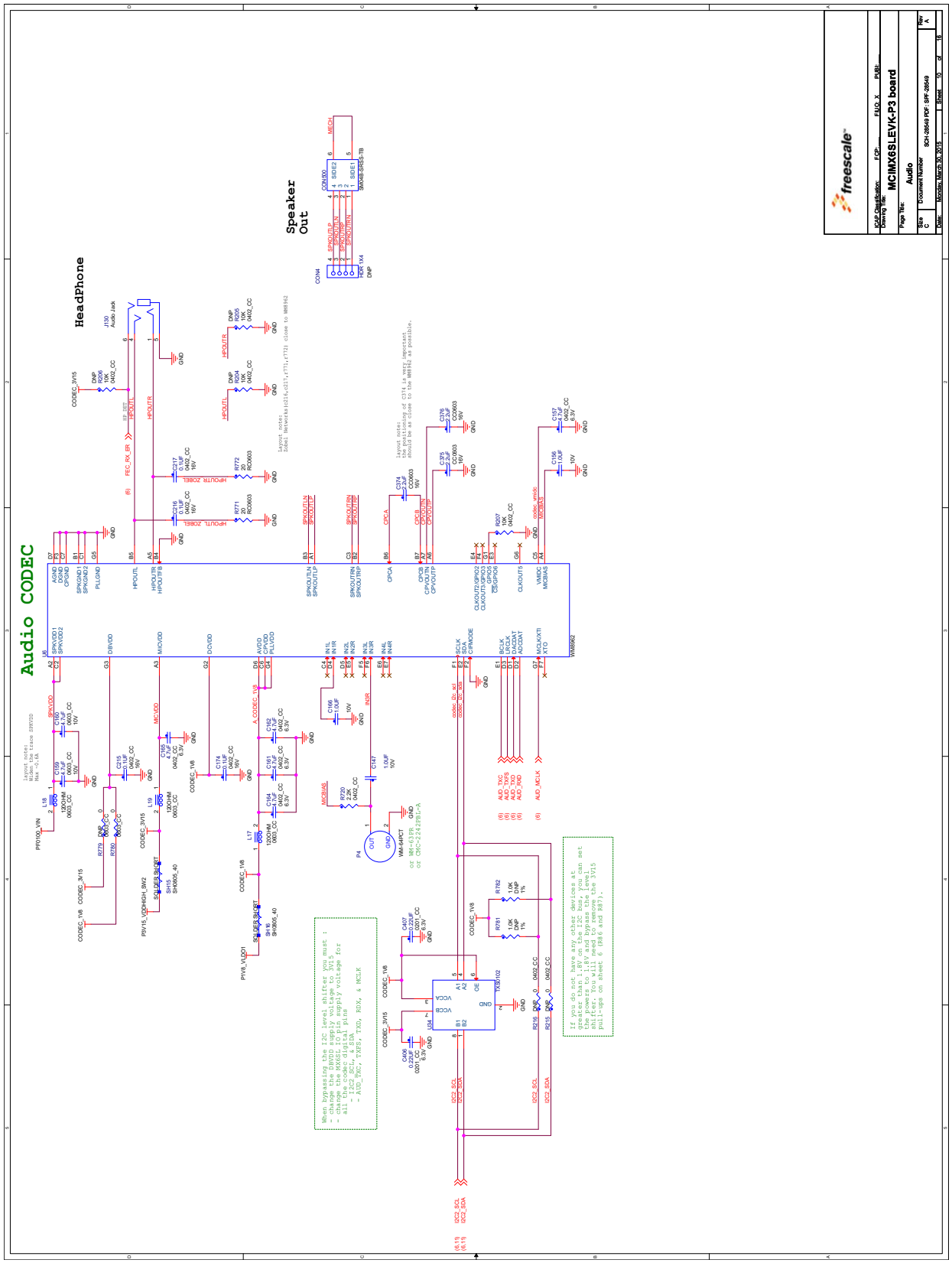

freescale
MCIMX6SLEVK-P3 board
IMX6SL_Power
MCIMX6L8DVN10AA
Note:
VDD_SOC_CAP1 to 6 and
VDD_SOC_CAP7 to 9 can be
connected together. If
split, the corresponding decoupling
capacitance needs to be
placed for each group of
pins.
D24 ensures VDD_SNVS_IN
is always powered whenever
VDDHIGH_IN is powered to meet
data sheet spec even if
P3V0_STBY faults to 0 V.
i.MX6SL Power table

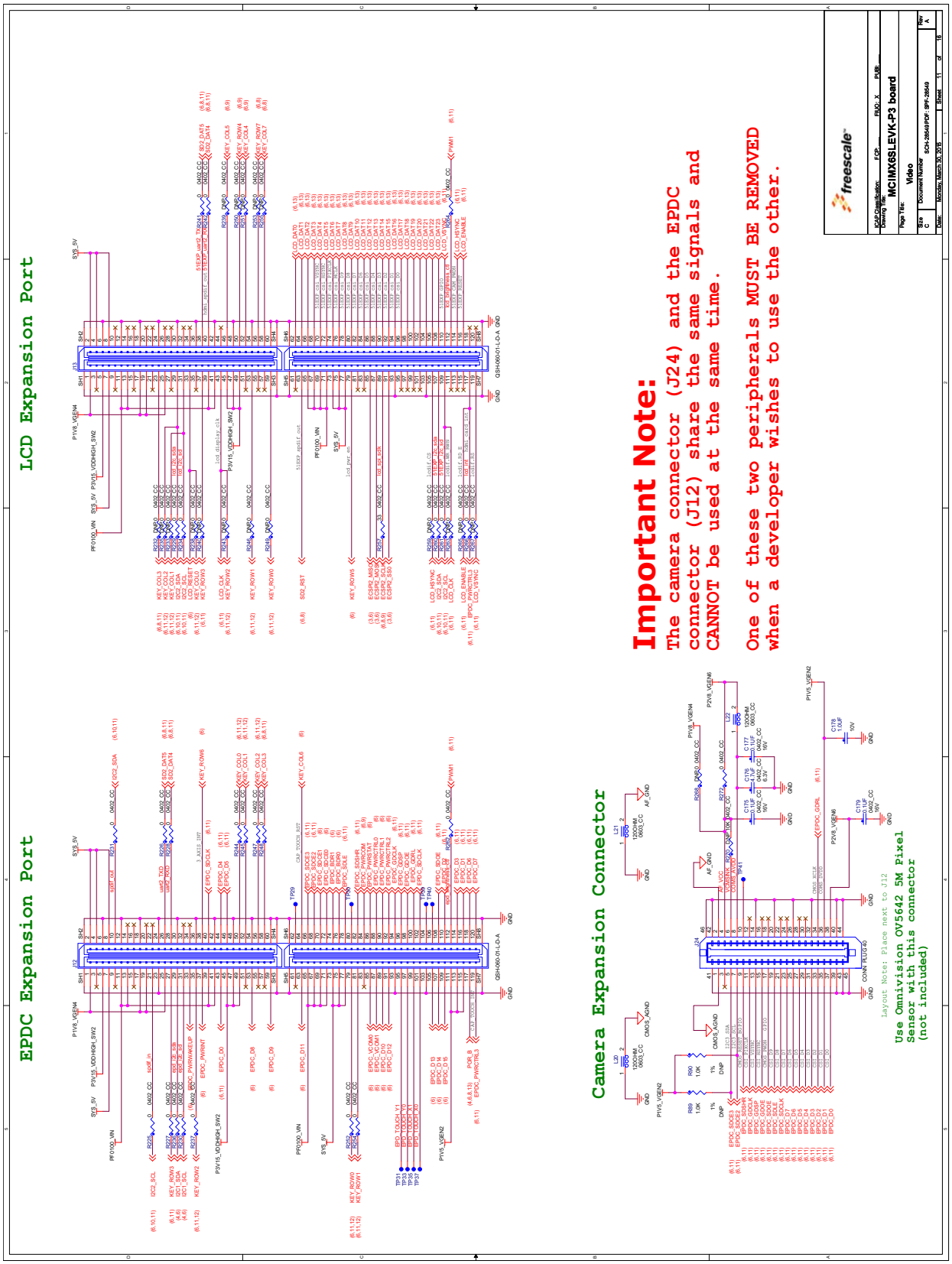

i.MX6SL
LCD
EPDC
SD
Control
Audio,UART,FEC
Keypad,HSIC,PWM
USB
I2C pullups
32.768kHz
24MHz
POR Reset
On/Off
RESET
ON/OFF
freescale
MCIMX6SL-EVK-P3 board
MCIMX6SL_SoC

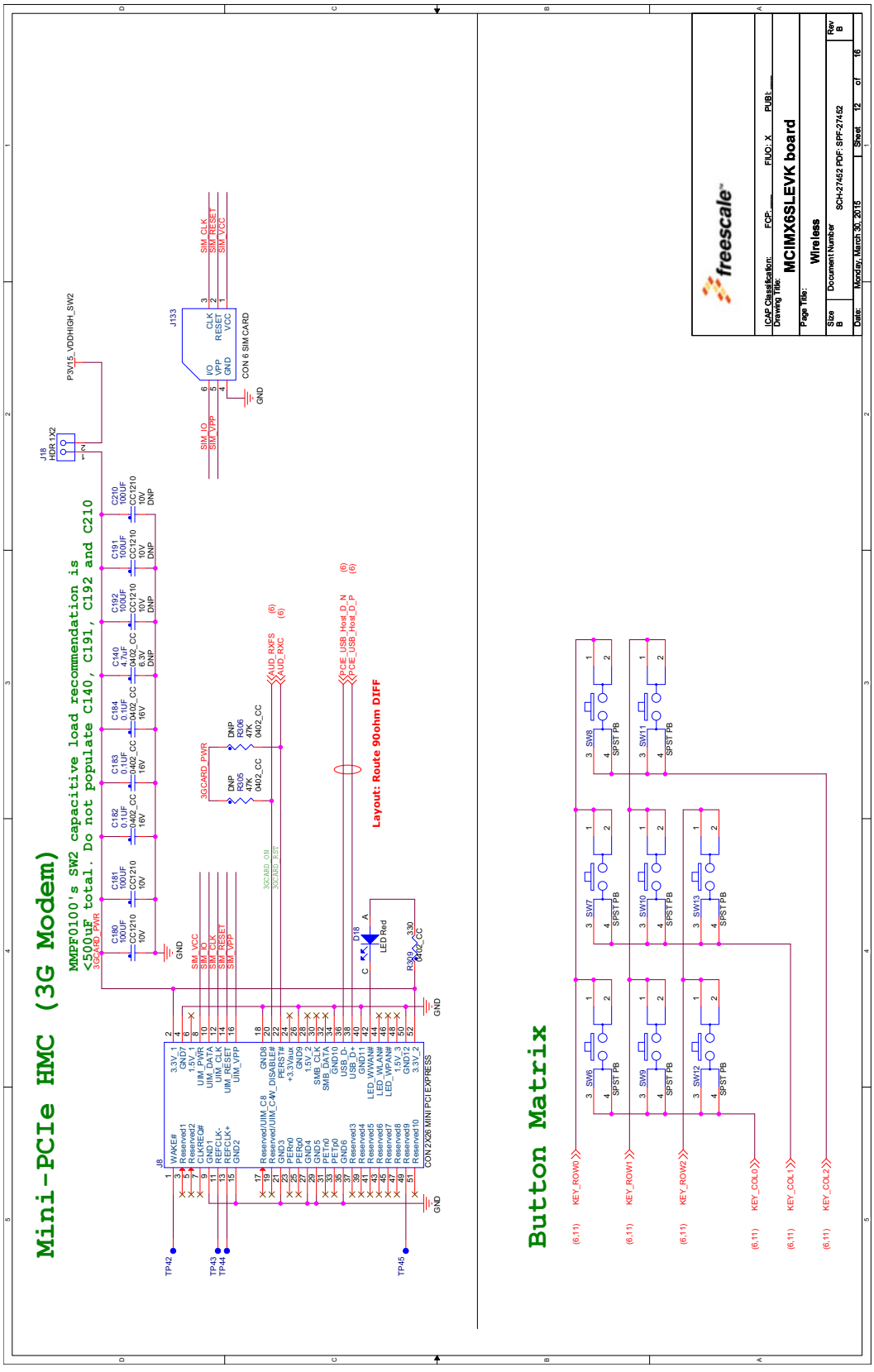

LPDDR2
8Gb 400MHz clock
i.MX6SL
DDR
Micron MT42L256M32D2LG-25 WT:A
Note:
Some dual-die LPDDR2 packages require a separate ZQ at pin AC11.
freescale
MCIMX6SLEVK-P3 board
LPDDR2

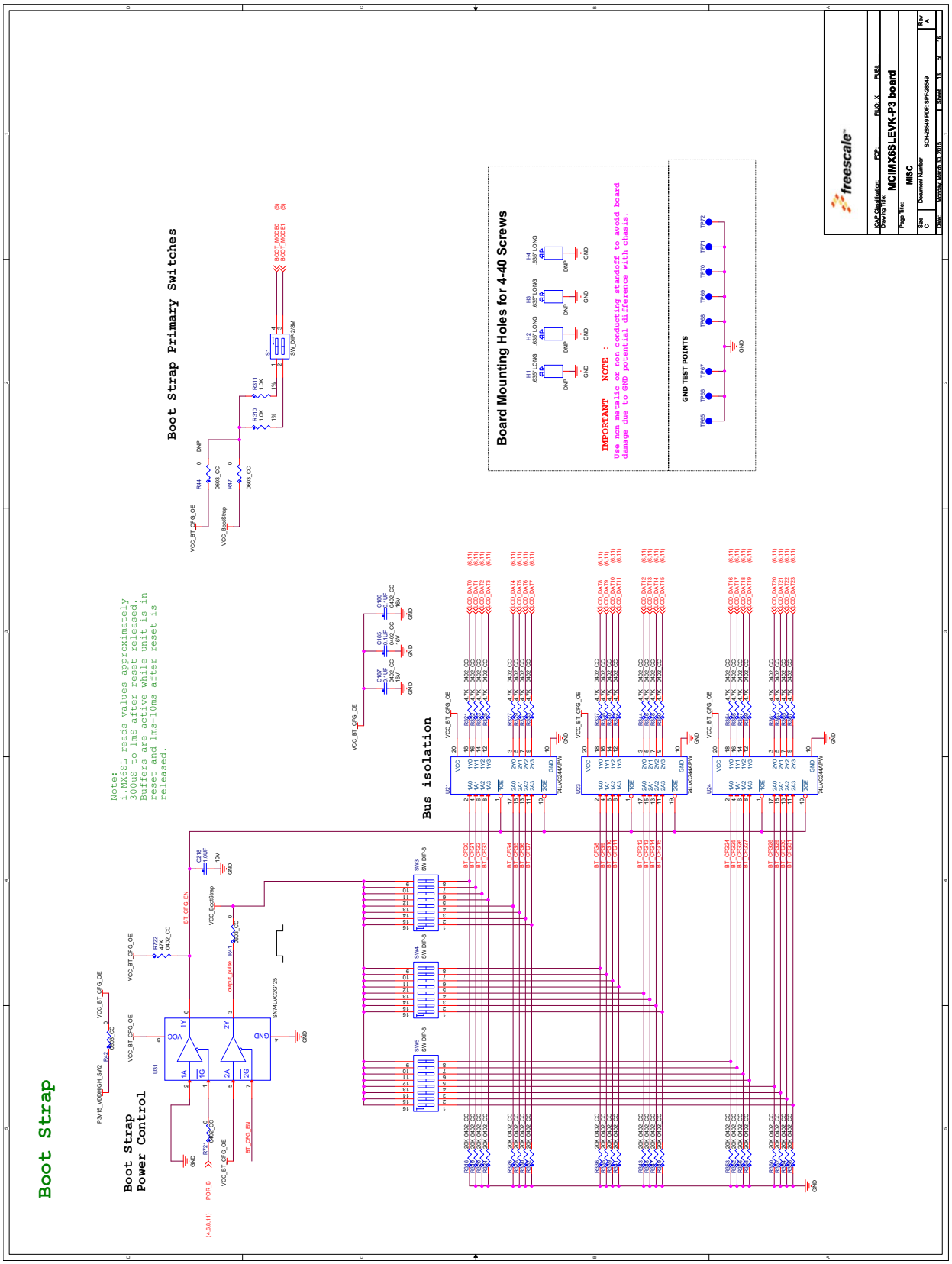

eMMC Footprint
8GB eMMC
4MB SPI NOR FLASH
SD1 - For Primary External Card Slot
8-bit SD
SD2 - For Boot Code
4-bit BOOT SD
SD3 - for WiFi and SD Accessories
For WiFi
freescale
MCIMX6SLEVK-P3 board
EMMC, SD and SPI NOR
Note: Place next to J21
low voltage IO cards
requires power-cycling
the card from
sdi rst_b.

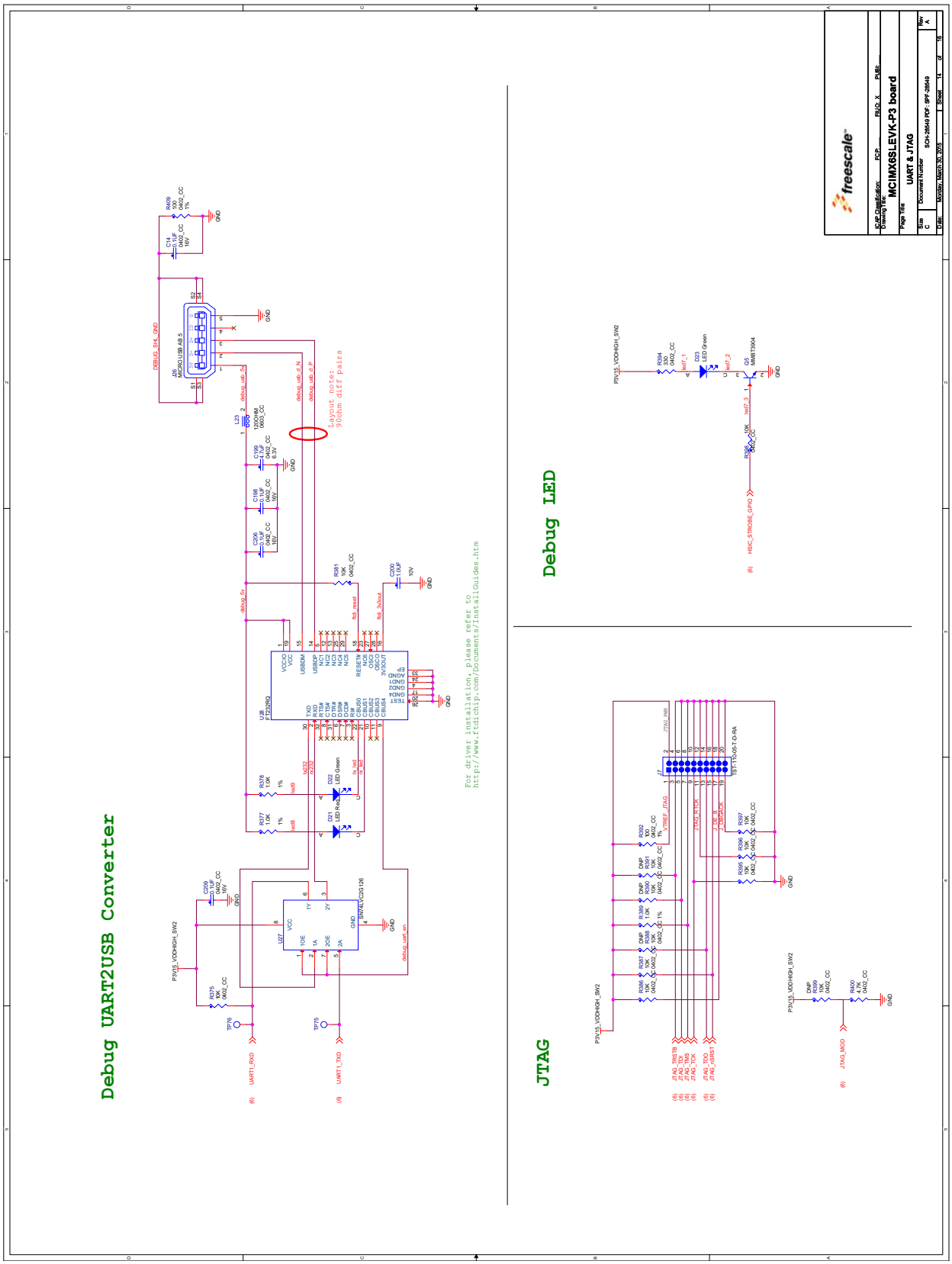

USB Boot/Host/Device Port
USB Host Port
USB 5V Control
USB Boot/Debug
Micro USB-AB Receptacle
USB_TYPE_A
Layout: Route 90ohm DIFF
Layout: Route 90ohm DIFF
freescale
MCIMX6SLEVK-P3 board
USB
SCH-28549 PDF: SPF-28549
Monday, March 30, 2015

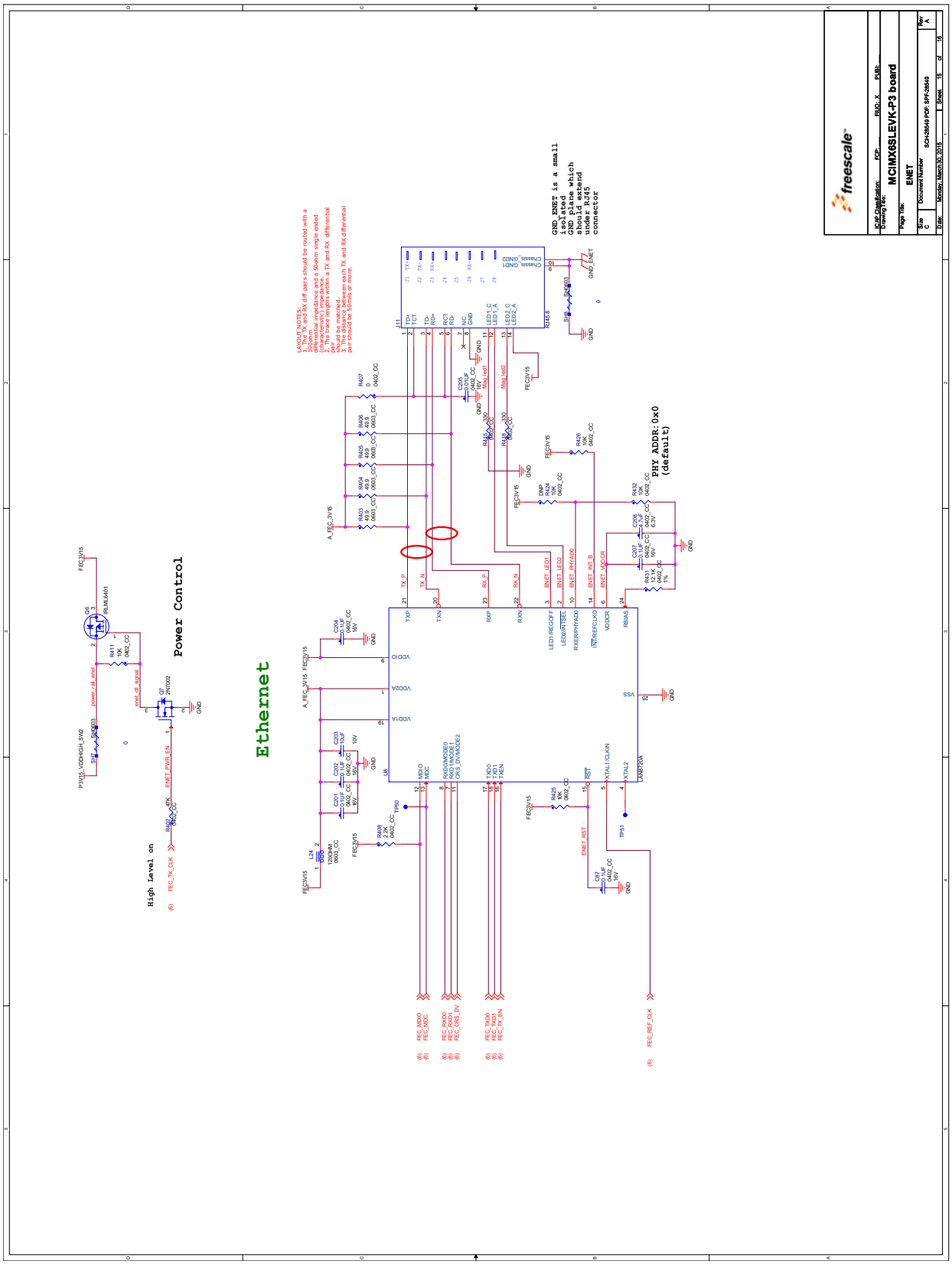

Audio CODEC
HeadPhone
Speaker Out
freescale
MCIMX6SLEVK-P3 board
Audio
SCH-28549 PDF: SPF-28549
Monday, March 30, 2015

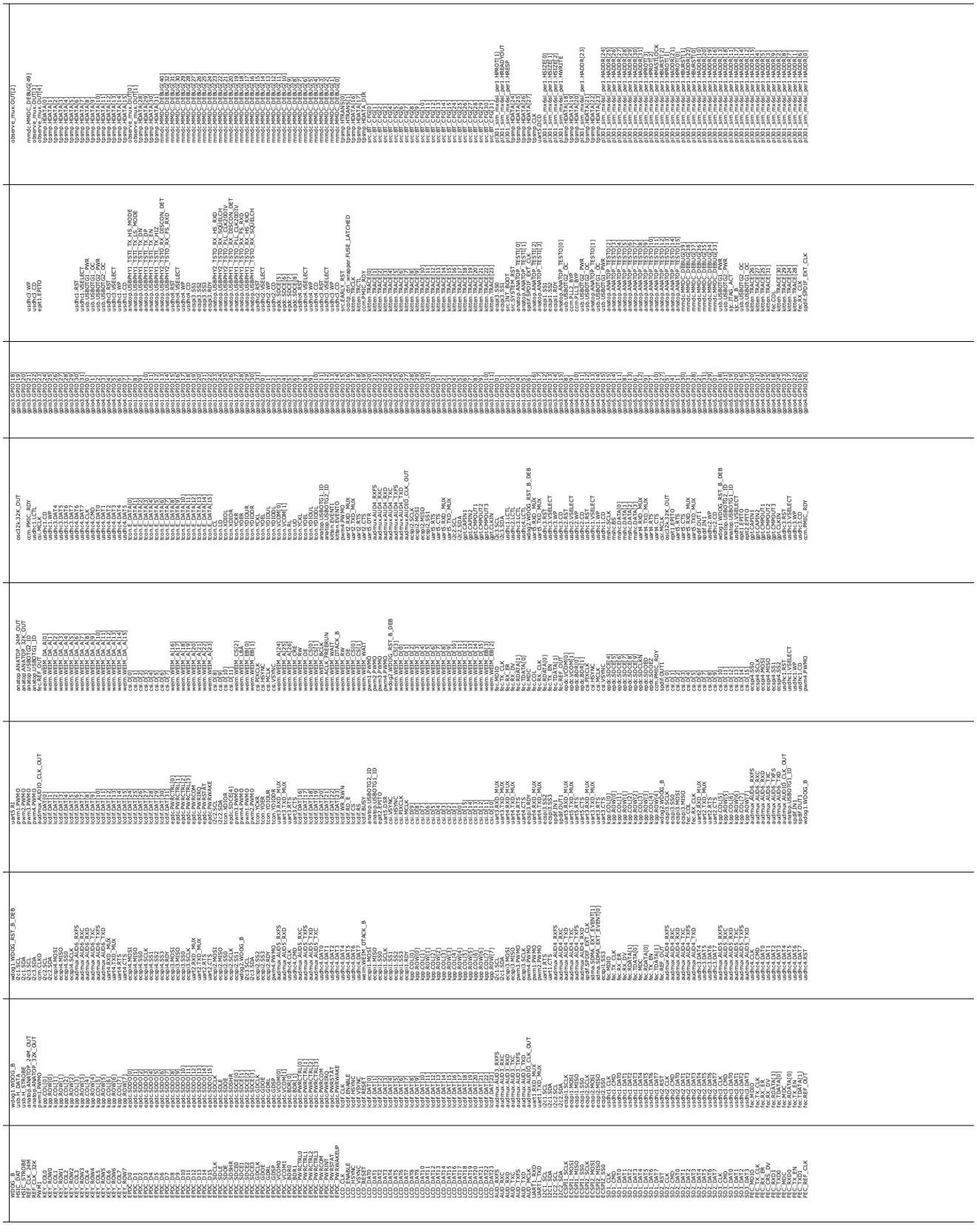

LCD Expansion Port
EPDC Expansion Port
Important Note:
The camera connector (J24) and the EPDC connector (J12) share the same signals and CANNOT be used at the same time.
One of these two peripherals MUST BE REMOVED when a developer wishes to use the other.
Camera Expansion Connector
Use Omnivision OV5642 5M Pixel Sensor with this connector (not included)
freescale
MCIMX6SLEVK-P3 board
Video


Mini-PCIe HMC (3G Modem)
MMPF0100's SW2 capacitive load recommendation is
<500uF total. Do not populate C140, C191, C192 and C210
Layout: Route 90ohm DIFF
Button Matrix
CON 2X26 MINI PCI EXPRESS
CON 6 SIM CARD
freescale
MCIMX6SLEVK board
Wireless


Boot Strap
Boot Strap
Power Control
Boot Strap Primary Switches
Bus isolation
Board Mounting Holes for 4-40 Screws
GND TEST POINTS
IMPORTANT NOTE :
Use non metalic or non conducting standoff to avoid board damage due to GND potential difference with chassis.
Note:
i.MX6SL reads values approximately 300uS to 1mS after reset released.
Buffers are active while unit is in reset and 1ms-10ms after reset is released.
freescale
MCIMX6SLEVK-P3 board
MISC
SCH-29549 PCB: SPF-29549


Debug UART2USB Converter
Debug LED
JTAG
MCIMX6SLEVK-P3 board
UART & JTAG
freescale


Ethernet
Power Control
PHY ADDR: 0x0
(default)
GND ENET is a small isolated GND plane which should extend under RJ45 connector
MCIMX6SLEVK-P3 board
ENET
freescale



5 Revision history

Revision	Date	Description of changes
1.0	4/2015	Initial release
	7/2016	Updated to NXP document form and style

How to Reach Us:

Home Page:
NXP.com

Web Support:
http://www.nxp.com/support

Document Number: AN5113
Rev. 1.0
7/2016