Hardware Design Guidelines for S12ZVM Microcontrollers
by: NXP Semiconductors

1 Introduction

1.1 Purpose and scope

The MC9S12ZVM-Family is an automotive 16-bit microcontroller family using the NVM + UHV technology that offers the capability to integrate 40 V analog components. This family reuses many features from the existing S12/S12X portfolio. The particular differentiating features of this family are the enhanced S12Z core, the combination of dual-ADC synchronized with PWM generation and the integration of “high-voltage” analog modules, including the voltage regulator (VREG), Gate Drive Unit (GDU), and either Local Interconnect Network (LIN) physical layer or CAN Physical layer. These features enable a fully integrated single chip solution to drive up to 6 external power MOSFETs for BLDC, Switching-Reluctance motor or PMSM motor drive applications.

NOTE

Electrical parameters mentioned in this application note are subject to change in individual device specifications. Check each application against the latest data sheet for specific target devices.
2 S12ZVM device family

The MC9S12ZVM-Family allows the integration of several key system components into a single device, optimizing system architecture and achieving significant space savings. The MC9S12ZVM-Family delivers all the advantages and efficiencies of a 16-bit MCU while retaining the low cost, power consumption, EMC, and code-size efficiency advantages currently enjoyed by users of existing S12(X) families. The MC9S12ZVM-Family is available in different pin-out options, using 80-pin, 64-pin and 48-pin LQFP-EP packages to accommodate LIN, CAN and external PWM based application interfaces.

2.1 MC9S12ZVM-family block diagram

Not all pins or all peripherals are available on all devices and packages.

![Block diagram of the MC9S12ZVM-Family](image-url)
### 2.2 MC9S12ZVM-family comparison

#### Table 1. MC9S12ZVM-family comparison

<table>
<thead>
<tr>
<th>Feature</th>
<th>ZVMC256</th>
<th>ZVML128</th>
<th>ZVMC128</th>
<th>ZVML64</th>
<th>ZVMC64</th>
<th>ZVML32</th>
<th>ZVML31</th>
<th>ZVM32</th>
<th>ZVM31</th>
<th>ZVM16</th>
<th>ZVM16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash KB</td>
<td>256</td>
<td>128</td>
<td>128</td>
<td>64</td>
<td>64</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>RAM</td>
<td>32 KB</td>
<td>8 KB</td>
<td>8 KB</td>
<td>4 KB</td>
<td>4 KB</td>
<td>4 KB</td>
<td>4 KB</td>
<td>4 KB</td>
<td>4 KB</td>
<td>2 KB</td>
<td>2 KB</td>
</tr>
<tr>
<td>Package</td>
<td>80 pin</td>
<td>64 pin</td>
<td>64 pin</td>
<td>64 pin</td>
<td>64 pin</td>
<td>64 pin</td>
<td>48 pin</td>
<td>48 pin</td>
<td>48 pin</td>
<td>48 pin</td>
<td>48 pin</td>
</tr>
<tr>
<td>LINPHY</td>
<td>–</td>
<td>1</td>
<td>–</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>HVPHY</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>SCI(1)</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>SPI</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>ADC channels</td>
<td>8+8</td>
<td>4+5</td>
<td>4+5</td>
<td>4+5</td>
<td>4+5</td>
<td>4+5</td>
<td>4+5</td>
<td>4+5</td>
<td>4+5</td>
<td>4+5</td>
<td>4+5</td>
</tr>
<tr>
<td>PMF channels</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>TIM channels</td>
<td>4 TIM0 + 2 TIM1</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>PWM channels</td>
<td>8</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>MSCAN</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>CAN VREG</td>
<td>1</td>
<td>–</td>
<td>1</td>
<td>–</td>
<td>1</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>CANPHY</td>
<td>1</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>External FET gate charge(nC)</td>
<td>Standard + 50%</td>
<td>Standard</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GDU external bootstrap diode</td>
<td>Needed</td>
<td>Not needed</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current sense op-amps</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Auxiliary tracker VREGs</td>
<td>2</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>
3 Power management

The power and ground pins are described in subsequent sections.

3.1 VSUP – main power supply pin

VSUP is the 12 V/18 V supply voltage pin for the on chip voltage regulator. This is the voltage supply input from which the voltage regulator generates the on chip voltage supplies. It must be protected externally against a reverse battery connection, as seen in figure 2.

The designer could choose to add Bulk/Bypass capacitor as a charge tank to provide power when losing battery. The value of this capacitor depends on the current consumption and the amount of time the MCU needs to perform house-keeping activities before shutting down.

3.2 Digital I/O and analog supplies

3.2.1 VDDX, VSSX — pad supply pins

VDDX is the supply domain for the digital Pads. An off-chip Stability and decoupling capacitor between VDDX and VSSX are required. This supply domain is monitored by the Low Voltage Reset circuit. VDDX1 and VDDX2 has to be connected externally to VDDA pin.

3.2.2 VDDA, VSSA — regulator reference supply pins

VDDA and VSSA pins are used to supply the analog parts of the regulator. Internal precision reference circuits are supplied from these signals. An off-chip decoupling capacitor between VDDA and VSSA is required and can improve the quality of this supply. VDDA has to be connected externally to VDDX.

NOTE

All GROUND pins of the microcontroller (VSSX1, VSSX2, VSS1, VSS2, VSSA, and VSSB, VSSC) must be connected together.

3.2.3 BCTL — base control pin for external PNP

The device supports the use of an external PNP to supplement the VDDX supply, for reducing on chip power dissipation. In this configuration, most of the current flowing from VRBATP to VDDX, flows through the external PNP. This configuration, using the BCTL pin.

The BCTL pin is the ballast connection for the on chip voltage regulator for the VDDX/VDDA power domains. It provides the base current of an external PNP Ballast transistor. An additional resistor between emitter and base of the BJT is required.
Table 2. VDDX/VDDA - component description and recommended values

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>D_{RBP}</td>
<td>Reverse Current/Battery diode Protection</td>
<td></td>
</tr>
<tr>
<td>C_{BULK}</td>
<td>Bulk/Bypass capacitor</td>
<td></td>
</tr>
<tr>
<td>C_{DCP}</td>
<td>Decoupling Capacitor</td>
<td></td>
</tr>
<tr>
<td>Q_{PNPX}</td>
<td>PNP Ballast transistor</td>
<td></td>
</tr>
<tr>
<td>R_{BCTL}</td>
<td>Metal Film resistor</td>
<td>1 kΩ</td>
</tr>
<tr>
<td>C_{BT}</td>
<td>Stability Capacitor. X7R Ceramic or Tantalum</td>
<td>4.7 uF – 10 uF</td>
</tr>
<tr>
<td>C_{DDX1,2}</td>
<td>Decoupling Capacitor for VDDX. X7R Ceramic</td>
<td>100 nF - 220 nF</td>
</tr>
<tr>
<td>C_{DDA}</td>
<td>Decoupling Capacitor for VDDA. X7R Ceramic</td>
<td>100 nF - 220 nF</td>
</tr>
</tbody>
</table>

**NOTE**

The C_{BT}-stability capacitor, is mandatory even if the PNP Ballast transistor is not used.

### 3.3 CAN power supply

A supply for an external CANPHY is offered via external device pins BCTLC and VDDC, whereby BCTLC provides the base current of an external PNP and VDDC is the CANPHY supply (output voltage of the external PNP). This is only available in the CANPHY package option.

#### 3.3.1 VDDC— CAN supply pin

VDDC is the supply domain for the CAN module. An off-chip Stability and decoupling capacitor between VDDC and VSSX is required. This supply domain is monitored by the Low Voltage Reset circuit.
3.3.2 BCTLC—base control pin for external PNP for VDDC power domain

BCTLC is the ballast connection for the on chip voltage regulator for the VDDC power domain. It provides the base current of an external BJT (PNP) of the VDDC supply. An additional resistor between emitter and base of the BJT is required.

![BCTLC diagram](image)

Figure 3. VDDC - CAN supply pin

### Table 3. VDDC - components description and recommended values

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q\textsubscript{PNPC}</td>
<td>PNP Ballast transistor</td>
<td></td>
</tr>
<tr>
<td>R\textsubscript{BCTLC}</td>
<td>Metal Film resistor</td>
<td>1 kΩ</td>
</tr>
<tr>
<td>C\textsubscript{DDC1}</td>
<td>Stability Capacitor. X7R Ceramic or Tantalum</td>
<td>4.7 uF – 10 uF</td>
</tr>
<tr>
<td>C\textsubscript{DDC2}</td>
<td>X7R Ceramic</td>
<td>100 nF - 220 nF</td>
</tr>
</tbody>
</table>

**NOTE**
On the ZVMC128 a diode is recommended between VDDA and VDDC, whereby the anode is connected to VDDC.

3.4 Internal Flash NVM power supply

3.4.1 VDDF — NVM logic supply pin

VDDF is the supply domain for the NVM logic. An off-chip decoupling capacitor between VDDF and VSS is required and can improve the quality of this supply. This supply domain is monitored by the Low Voltage Reset circuit.
3.5 Sensor power supply

3.5.1 VDDS1 and VDDS2—sensor supply pins

VDDS1 and VDDS2 are short circuit protected supply domain which are suitable for sensors (which connect externally to the PCB). An off-chip Stability and decoupling capacitor between the power domain and VSSX are required. These supply domains are monitored by a Low Voltage Detect (LVDS1 and LVDS2) circuits.

3.5.2 BCTLS1 and BCTLS2—base control pins for external PNP for VDDS1 and VDDS2 power domains

BCTLS1 and BCTLS2 are the ballast connections for the on chip voltage regulators for the VDDS1 and VDDS2 power domains. These pins provide the base current of an external BJT (PNP) of the VDDS1 and VDDS2 supplies. An additional 1KΩ resistor between emitter and base of the BJT is required per each PNP transistor. The figure 5 shows an application example for the external BCTLS1 pin.

3.5.3 SNPS1 and SNPS2—sense pin

SNPS1 and SNPS2 are the sense inputs associated with the VDDS1 and VDDS2 power domain regulators. The voltage regulators use these pins to detect a short circuit or over current condition and subsequently limits the current to avoid damage.

Equation 1.

\[ R_{NSX} = \frac{V_{NSM}}{I_{NS, MAX}} \]

Where:

- \( R_{NSX} \) – Sense Resistor
- \( V_{NS} \) – SNPS monitor threshold between VSNPS and VDDS, (upto 140 mV).
\( I_{\text{SNS_MAX}} \) – Desired max current flowing

![Figure 5. VDDS1 and VDDS2 — Sensor Supply Pins](image)

### Table 5. VDDS1 and VDDS2 - Components description and recommended values

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q(_{\text{PNPSX}})</td>
<td>PNP Ballast transistor</td>
<td></td>
</tr>
<tr>
<td>R(_{\text{BCTLSX}})</td>
<td>Metal Film resistor</td>
<td>1 kΩ</td>
</tr>
<tr>
<td>R(_{\text{SNSX}})</td>
<td>Sense resistor</td>
<td></td>
</tr>
<tr>
<td>C(_{\text{DDS1}})</td>
<td>Stability Capacitor. X7R Ceramic or Tantalum</td>
<td>4.7 uF-10 uF</td>
</tr>
<tr>
<td>C(_{\text{DDS2}})</td>
<td>X7R Ceramic</td>
<td>100 nF - 220 nF</td>
</tr>
</tbody>
</table>

### 3.6 Selecting the PNP external ballast transistor

The maximum VREG current capability \([I_{\text{VREGMAX}}]\) using a PNP External Ballast transistor \([Q_{\text{PNP}}]\), must be determined by the allowed maximum power of the device. The designer should consider that the maximum power dissipation of the transistor will depend mainly on the following factors:

- Package type
- Dissipation mounting pad area on the PCB
- Ambient temperature

Like maximum power supply potentials, maximum junction temperature is a worst case limitation which shouldn’t be exceeded. This is a critical point, since the lifetime of all semiconductors is inversely related to their operating junction temperature. For almost all transistors packages, the maximum power dissipation is specified to +25°C; and above this temperature, the power derates to the maximum Junction Temperature (+150°C). The \(R_{\text{thJA}}\) depends considerably on the package transistor and the mounting pad.
area. The final product thermal limits should be tested and qualified in order to ensure acceptable performance and reliability.

![Diagram showing maximum power dissipation versus temperature]

**Figure 6. Maximum power dissipation versus temperature**

The maximum power dissipation $PWR_{\text{MAX}}$ by the device is given by:

\[
PWR_{\text{MAX}} = \frac{T_{\text{JMAX}} - T_{\text{AMB}}}{R_{\text{thJA}}}
\]

where $T_{\text{AMB}}$ is ambient temperature, $T_{\text{JMAX}}$ is maximum junction temperature and $R_{\text{thJA}}$ is the Junction to Ambient Thermal Resistance of the Ballast transistor mounted on the specific PCB.

### 3.6.1 Static thermal analysis

It is extremely important to consider the derating of the power device above of $+25^\circ$C (typical value for transistors). This guarantees that the junction temperature will be lower than the maximum operating junction temperature allowed by the device supplier. The following static thermal analysis using PSPICE Simulator demonstrates how the maximum power dissipation and the maximum supply current can be estimated for different voltage levels of VDDX.

**NOTE**

The data used in the next examples are fictional and should not be taken as specifications for particular systems. For specific calculations, please refer to the device datasheet.
Example analysis:

### Static Thermal Analysis

![Static Thermal Analysis Diagram]

Parameter:

\[
\frac{(V(\%IN1) + V(\%IN2))}{(V_{SUP\text{max}} - V_{DDX\text{min}})} \leq \frac{520\text{mW}}{85.280\text{mA}}
\]

As a result of these examples, the maximum power dissipation of the ballast transistor is 520 mW. At this value, the transistor will reach its maximum operating temperature rating of 150°C. Therefore, the transistor can provide a maximum of 85.280 mA.

#### 3.6.2 Recommended ballast transistors

Transistor specifications give the minimum and maximum gain. The worst case is usually significantly lower than the nominal figure on the transistor datasheet cover page. Furthermore, the datasheet values are usually given at room temperature (+25 °C). The required gain should be calculated at cold temperature, because a PNP/NPN transistor has minimum gain at low temperature. The worst case gain at cold temperature can be obtained from the transistor supplier or can be estimated using the graphs given in the transistor datasheet.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package Type</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>BCP53 (Actually used in the EVB)</td>
<td>SOT-223</td>
<td>NXP</td>
</tr>
<tr>
<td>PBSS5360PAS</td>
<td>SOT1061D</td>
<td></td>
</tr>
</tbody>
</table>

The designer must follow and verify all Layout/soldering footprint recommendations of the transistor supplier in order to reach a good performance transistor.

Make sure that the traces for decoupling capacitors are as short as possible. Shortening the capacitor traces to/from the ground/power plane is the most important concern for making a low inductance connection. In order to implement an appropriate decoupling for applications with LIN, CAN, SPI and IIC interfaces, consider the pairing of the power and ground planes close to each other (less than 10 mils). This creates...
an effect interplane capacitance, greatly reduces noise and increases power supply stability at the pins because of the extremely low inductance of this kind of capacitance in the layers. The number of discrete capacitance can be reduced because the effective capacitors are greatly increased and the impedance of the power distribution network is reduced across a very broad frequency range.

4 Programming interface

4.1 BKGD

The background debug controller (BDC) is a single-wire, background debug system implemented in on-chip hardware for minimal CPU intervention. The device BKGD pin interfaces directly to the BDC. The S12ZVM maintains the standard S12 serial interface protocol but introduces an enhanced handshake protocol and enhanced BDC command set to support the linear instruction set family of S12Z devices and offer easier, more flexible internal resource access over the BDC serial interface. The BKGD signal is used as a pseudo-open-drain signal for the background debug communication. The BKGD signal has an internal pull-up device.

![Debug connector configuration](image)

**Figure 8. Debug connector configuration**

4.2 Reset

The RESET signal is an active low bidirectional control signal. It acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset. The RESET pin has an internal pull-up device.

Upon detection of any reset source, an internal circuit drives the RESET pin low for 512 PLLCLK cycles. After 512 PLLCLK cycles the RESET pin is released. The internal reset of the MCU remains asserted while the reset generator completes the 768 PLLCLK cycles long reset sequence. In case the RESET pin is externally driven low for more than these 768 PLLCLK cycles (External Reset), the internal reset remains asserted longer.
In prototype designs, it is common to add a push-button to manually force a reset. In this case, the designer could choose to add a debounce capacitor to this button. In the event of an internal reset event, the MCU forces the RESET pin low and up again so that other circuits connected to this pin are reset as well. This reset pulse must last less than 24 μs. The debounce capacitance on the reset line must ensure that this timing constraint is met. Capacitors smaller than 10 pF are recommended.
4.3 TEST pin

This pin should always be grounded in all applications.

5 Clock circuitry

The S12ZVM devices have an internal 1 MHz internal RC oscillator with +/-1.3% accuracy over rated temperature range. There is an alternative to add an external resonator or crystal, for higher and tighter tolerance frequencies. The S12ZVM includes an oscillator control module capable of supporting either Loop Controlled Pierce (LCP) or Full Swing Pierce (FSP) oscillator configurations. The oscillation mode is selectable by software.

5.1 EXTAL and XTAL

These pins provide the interface for a crystal to control the internal clock generator circuitry. EXTAL is the input to the crystal oscillator amplifier. XTAL is the output of the crystal oscillator amplifier. If XOSCLCP is enabled, the MCU internal OSCCLK_LCP is derived from the EXTAL input frequency. If OSCE=0, the EXTAL pin is pulled down by an internal resistor of approximately 200 kΩ and the XTAL pin is pulled down by an internal resistor of approximately 700 kΩ.

The Pierce oscillator provides a robust, low-noise and low-power external clock source. It is designed for optimal start-up margin with typical crystal oscillators. S12ZVM supports crystals or resonators from 4 MHz to 20 MHz. The Input Capacitance of the EXTAL, XTAL pins is 7 pF.

![Reference oscillator circuit](image)

**Figure 11. Reference oscillator circuit**

**Table 7. Components of the oscillator circuit**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RS</td>
<td>Bias Resistor</td>
</tr>
<tr>
<td>X1</td>
<td>Quartz Crystal / Ceramic Resonator</td>
</tr>
<tr>
<td>C&lt;sub&gt;XTAL&lt;/sub&gt;</td>
<td>Stabilizing Capacitor</td>
</tr>
<tr>
<td>C&lt;sub&gt;EXTAL&lt;/sub&gt;</td>
<td>Stabilizing Capacitor</td>
</tr>
</tbody>
</table>
The load capacitors are dependent on the specifications of the crystal and on the board capacitance. It is recommended to have the crystal manufacturer evaluate the crystal on the PCB.

## 5.2 Suggestions for the PCB layout of oscillator circuit

The crystal oscillator is an analog circuit and must be designed carefully and according to analog-board layout rules:

- External feedback resistor [Rf] is not needed because it’s already integrated.
- It is recommended to send the PCB to the crystal manufacturer to determine the negative oscillation margin as well as the optimum regarding $C_{XTAL}$ and $C_{EXTAL}$ capacitors. The data sheet includes recommendations for the tank capacitors $C_{XTAL}$ and $C_{EXTAL}$. These values together with the expected PCB, pin, etc. stray capacity values should be used as a starting point.
- Signal traces between the S12ZVM pins, the crystal and, the external capacitors must be as short as possible, without using any via. This minimizes parasitic capacitance and sensitivity to crosstalk and EMI. The capacitance of the signal traces must be considered when dimensioning the load capacitors.
- Guard the crystal traces with ground traces (guard ring). This ground guard ring must be clean ground. This means that no current from and to other devices should be flowing through the guard ring. This guard ring should be connected to VSS of the S12ZVM with a short trace. Never connect the ground guard ring to any other ground signal on the board. Also avoid implementing ground loops.
- The main oscillation loop current is flowing between the crystal and the load capacitors. This signal path (crystal to $C_{EXTAL}$ to $C_{XTAL}$ to crystal) should be kept as short as possible and should have a symmetric layout. Hence, both capacitor’s ground connections should always be as close together as possible.

The following figure 12 shows the recommended placement and routing for the oscillator layout.

![Figure 12. Suggested crystal oscillator layout](image)
6 High Voltage Inputs (HVI)

The high-voltage input (HVI) on port L has the following features:

- Input voltage proof up to $V_{\text{HVI}}$
- Digital input function with pin interrupt and wakeup from stop capability
- Analog input function with selectable divider ratio routable to ADC channel. Optional direct input bypassing voltage divider and impedance converter. Capable to wake-up from stop (pin interrupts in run mode not available). Open input detection.

The connection of an external pull device on a high-voltage input can be validated by using the built-in pull functionality of the HVI. Depending on the application type, an external pull down circuit can be detected with the internal pull-up device whereas an external pull-up circuit can be detected with the internal pull down device which is part of the input voltage divider.

Note that the following procedures make use of a function that overrides the automatic disable mechanism of the digital input buffer when using the HVI in analog mode. Make sure to switch off the override function when using the HVI in analog mode after the check has been completed.

An external resistor $R_{\text{EXT,HVI}}$ must be always connected to the high-voltage inputs to protect the device pins from fast transients and to achieve the specified pin input divider ratios when using the HVI in analog mode.

6.1 External pulldown device

![Figure 13. Digital Input Read with Pull-up Enabled](image-url)
6.2 External pull up device

![Figure 14. Digital Input Read with Pull-down Enabled](image)

7 GDU interface

The purpose of motor control is to control the speed, direction of rotation or position of the motor shaft. This requires that the voltage applied to the motor is modulated in some manner. This is where the Power-MOSFET is used. By turning the power-switching elements ON and OFF in a controlled manner, the voltage applied to the motor can be varied in order to vary the speed or position of the motor shaft.

The S12ZVM includes a GDU module, this module is a Field Effect Transistor (FET) pre-driver designed for three phase motor control applications. A combination of bootstrap and charge-pump techniques is used to power the circuitry which drives the upper MOSFETs of the H-Bridge. The bootstrap technique supplies the high instantaneous current needed for turning on the power devices, while the charge pump provides enough current to maintain bias voltage on the upper pre-driver section.
7.1 FETs pre-driver interface

The pre-driver interface is connected directly to the external low-side and high-side power-MOSFETs. The primary function of a driver is to switch a MOSFET from off-state to on-state and vice versa, the pre-driver amplifies the control signals to required levels to drive the power MOSFET. To guarantee reliable operation, the low-side drivers are supplied by the VLS regulator while the high-side drivers are supplied directly by the bootstrap circuit. The gate charge that can be delivered to each external Power-MOSFET is of 50 nC and 75 nC, depending of the GDU version.
Figure 16. S12ZVM Application Diagram - 3 Phase DC
Figure 17. S12ZVMB Application Diagram - Bidirectional DC Motor
Figure 18. S12ZVMA Application Diagram - Electromagnetic Actuator
Figure 19. S12ZVMA Application Diagram - Uni-directional DC Motor
Figure 20. S12ZVMA Application Diagram - Uni-directional DC Motor
7.1.1 HD — FET pre-driver high side drain connection

This is the drain connection of the external high-side FETs. The GDU high side drain voltage input, pin HD, is monitored within the GDU and mapped to an interrupt. A connection to the ADC is provided for accurate measurement of a scaled HD level. The HD pin should be connected as near as possible to the drain connections of the high-side MOSFETs. The external connections for the HD pin must ensure a reverse battery protection.

7.1.2 HG[2:0] — high-side gate pins

The pins are the gate drives for the high-side power FETs. The drivers provide a high current with low impedance to turn on and off the high-side power FETs.
7.1.3 HS[2:0] — high-side source pins

The pins are the source connection for the high-side power FETs and the drain connection for the low-side power FETs. The low voltage end of the bootstrap capacitor is also connected to this pin.

7.1.4 LG[2:0] — low-side gate pins

The pins are the gate drives for the low-side power FETs. The drivers provide a high current with low impedance to turn on and off the low-side power FETs.

7.1.5 LD[2:0] — low-side drain pins (only on GDUV6)

These pins are the drain connections for the low-side power FETs.

7.1.6 LS[2:0] — low-side source pins

The pins are the low-side source connections for the low-side power FETs. The pins are the power ground pins used to return the gate currents from the low-side power FETs.

7.1.7 Selecting the power MOSFET

When determining the gate drive requirements for the switching device in the motor control application, the dynamic characteristics determine the performance of the device. The total gate charge \( Q_G \), is one of most important parameters which define the selection of the right MOSFET. The charge on the gate terminal of the MOSFET as determined by its gate-to-source capacitance. The lower the gate charge, the easier it is to drive the MOSFET. Total gate charge, \( |Q_G| \), affects the highest reliable switching frequency of the MOSFET. The lower the gate charge, the higher the frequency. Operation at higher frequencies allows use of lower value, smaller size capacitors and inductors, which can be significant factors in system cost. A low gate charge also makes it easier to drive the MOSFET, however, designers sometimes need to trade-off switching frequency with EMI considerations.

The amount of charge necessary to switch the MOSFET can be determined from its data sheet by knowing the intended gate-to-source voltage, drain current and drain-to-source voltage. The number can be taken from the characteristic curve for gate charge or taken directly from the electrical characteristics section of the MOSFET data sheet. The gate charge number will give the total gate charge necessary to switch the device. The amount of current required to switch a MOSFET is directly related to the gate charge and can be determined using the next equation:

\[
Q_G = I \times t
\]

Where:
- \( Q_G \) = total gate charge number
- \( I \) = gate current
- \( t \) = device switching time
7.1.7.1 Switching process of the power MOSFET

The turn-on transition is broken down into three phases, refer to figure 17. These phases will be briefly explained. The figure 18 shows the transition through these regions in terms of output characteristics. Gate charge can be derived from the non-linear capacitance curves.

In the stage-1 [S1], from \( t_0 \) to \( t_1 \), the MOSFET is OFF, gate-to-source voltage \( [V_{GS}] \) rises from 0 V to its plateau voltage \( [V_{GP}] \). Once \( V_{GS} \) reaches the threshold voltage \( [V_{TH}] \), the MOSFET starts conducting and \( I_D \) rises. In this phase, the gate current charges the input capacitance \( (C_{ISS}) \) with its \( V_{DS} \) being clamped. MOSFET starts to conduct, and the turn-on process enters the second stage.

In the stage-2 [S2], from \( t_1 \) to \( t_2 \), the drain current finally reaches the level of the total load current. \( V_{GS} \) is clamped at \( V_{GP} \) and remains relatively flat. During this region, the gate current is used to charge the reverse transfer capacitance \( (C_{RSS}) \) and the MOSFET operates in the linear region. After the MOSFET takes over all of the load current, the drain to source voltage \( V_{DS} \) starts to drop, and the circuit enters the third stage.

Switching losses occur between the phase where the \( V^G \) reaches the \( V^{TH} \), in the stage1 to \( t_2 \). The minimum turn-on time is usually governed by the \( dv/dt \) capability of the system. Reducing the turn-on time increases the amount of diode reverse recovery current and hence increases the peak power dissipation, however the total power dissipated tends to reduce.

In the stage-3 [S2], from \( t_2 \) to \( t_3 \), the MOSFET enters into Ohmic mode operation. \( V_{GS} \) rises from \( V_{GP} \) to driver supply voltage \( (V_{GDR}) \). Both \( I_D \) and \( V_{DS} \) remain relatively constant.

Several of the dynamic parameters are highly dependent on the measurement conditions. Consequently, understand the dynamic characteristics before comparing data sheets from suppliers with different standard conditions.
Figure 22. Gate-to-Source voltage and switching versus total charge

Figure 23. On-Region characteristics for different Gate-to-Source voltages
7.1.7.2 Internal diode reverse characteristic

In motor applications that make positive use of a power MOSFET internal diode, there is a requirement for this reverse recovery time \( t_{rr} \) to be fast. The diode characteristics are important if the MOSFET is being used in the so-called "third quadrant". The third quadrant is a typical arrangement where the MOSFET replaces a diode to reduce the voltage drop from the inherent diode forward voltage drop. In such a situation, there is always a small time period when the MOSFET parasitic diode is conducting before the MOSFET turns on. For such applications, the diode switching parameters are important. In addition, diode reverse recovery contributes to the power losses as well as oscillation, which can cause EMC concern.

7.1.8 Circuit layout considerations

The optimum performance of high and low side gate drivers cannot be achieved without taking due considerations on the circuit board design and layout. The precautions which must be taken to minimize the amount of stray inductance in the circuit include:

- Positioning the power MOSFETs as close as possible to the pre-driver interface of the S12ZVM microcontroller.
- Reducing circuit board track lengths to a minimum and using twisted pairs for all interconnections.
- For paralleled devices, keeping all connections short and symmetrical.

7.1.8.1 Recommended N-MOSFET

Table 8. Recommended N-MOSFET

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package Type</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>BUK7Y3R5-40E</td>
<td>SOT669</td>
<td>NXP</td>
</tr>
<tr>
<td>AUIRF1018E</td>
<td>D2PAK</td>
<td>IRF</td>
</tr>
<tr>
<td>AUIRF1018ES</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AUIRF1010EZ</td>
<td>D2PAK</td>
<td></td>
</tr>
<tr>
<td>AUIRF1010EZXS</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

7.2 Bootstrap circuit

A combination of bootstrap and charge-pumping techniques is used to power the circuitry which drives the upper MOSFETs of the H-Bridge. The bootstrap technique supplies the high instantaneous current needed for turning on the power devices, while the charge pump provides enough current to maintain bias voltage on the upper driver sections and MOSFETs. Since voltages on the upper bias supply pin “float” with the source terminals of the upper power switches.

The high side pre-driver must provide a sufficient gate-source voltage and sufficient charge for the gate capacitance of the external FETs. A bootstrap circuit is used to provide sufficient charge. The bootstrap circuit uses a set of external diodes and capacitors to provide a significant amount of current to turn on (Ohmic region) the top MOSFETS rapidly, the gate of each device must be driven approximately 8 V
more positive than the supply voltage. To achieve this an internal charge pump is used to provide the gate drive voltage. For high frequency applications all bootstrap components, are required.

**Figure 24. Charge pump circuitry**
Figure 25. Charge pump circuitry with filter

Recommended values for optional VBS filter $C_{\text{FILT}} = 3.3 \, \text{nF}$, $R_{\text{FILT}} = 10 \, \text{ohms}$, $R_{\text{HS}} = 10 \, \text{ohms}$

The VBS[2:0] pins are the bootstrap capacitor connections for phases HS[2:0]. The capacitor is connected between HS[2:0] and this pin. The bootstrap capacitor provides the gate voltage and current to drive the gate of the high side FET.

### 7.2.1 Bootstrap components selection

**Equation 4.**

$$C_{BSX} \geq \frac{Q_G + (D_{\text{MAX}} \times T_{SW} \times I_{GDU})}{\Delta V}$$

The Bootstrap Capacitor value $C_{BS}$ is determined as:

where:

- $Q_G$ - Total Gate charge of MOSFET
GDU interface

- $D_{MAX}$ - Maximum Duty cycle
- $T_{SW}$ - Switching Period
- $I_{GDU}$ - Current consumption of GDU
- $\Delta V$ - Voltage drop accepted on $C_{BCX}$ at end of ON time

Example:
- Design Requirements:

\[
\begin{align*}
Q_{G_{MOSFET}} &= 47 \, nC \\
T_{SW} &= 1/20 \, kHz = 50 \, \mu s \\
D_{MAX} &= 90\% = 0.9 \\
\Delta V &= 0.5 \, V \\
I_{GDU} &\leq 600 \, \mu A
\end{align*}
\]

- Solution:

**Equation 5.**

\[
C_{BCX} \geq \frac{47nC + (0.9 \times 50 \mu s \times 600 \mu A)}{0.5V} = 148nF
\]

Considering lifetime and tolerances, an appropriate capacitor value would be 220 nF. A low ESR, for example, a X7R capacitor is recommended for the bootstrap circuit and supports both the low-side driver and bootstrap recharge.

The bootstrap diode must use a lower forward voltage drop and a switching time as soon as possible for fat recovery, such as ultra-fast.

### 7.2.2 Printed circuit board layout

The layout for minimize parasitic inductances is as follows:

- Direct tracks between switches with no loops or derivation.
- Avoid interconnect links. These can add significant inductance by lowering package height above the PCB
- Place the bootstrap diodes as close as possible to the bootstrap capacitors.

### 7.3 Charge Pump

A charge pump voltage is used to supply the high side FET pre-driver with enough current to maintain the gate source voltage. To generate this voltage an external charge pump is driven by the pin CP, switching between 0 V and 11 V. The pumped voltage is then applied to the pin VCP.
The CP - Charge Pump In/Output Pin, is the switching node of the charge pump circuit. The supply voltage for charge pump driver is the output of the voltage regulator VLS. The output voltage of this pin switches typically between 0 V and 11 V. The pumped voltage is then applied to the pin VCP.

The VCP - Charge Pump Input for High-Side Driver Supply pin is the pumped output signal which supplies the bootstrap cap and the high-side FET pre-driver supply VBS[2:0].

The charge pump voltage VCP, is determined as:

**Equation 6.**

\[
V_{CP} = V_{IN} + CP - 2(V_{FWD_{DCP}})
\]

The charger pump capacitor value \(C_{CP1}\), depends of the energy required for the high side drivers, is determined as:

**Equation 7.**

\[
C_{CP1} \geq \frac{\Delta Q \times N_{HS}}{V_{CP}}
\]

The voltage ripple is minimum for \(C_{CP2} >> C_{CP1}\), 10x is recommended.

And the steady state of VCP is reached after \(5\tau (\sim 99\%)\); where the time constant is approximately:

**Equation 8.**

\[
\tau = \left(\frac{1}{f_{SWCP} \times C_{CP1}}\right) (C_{CP2} + C_{CP1})
\]

where \(f_{SWCP}\) is the switching frequency configured by the GCPCD register.
Example

- Design requirements:

\[
V_{IN} = 12\,V \\
CP = 11\,V \\
\Delta Q_G = 50\,nC \\
N_{HSD} = 3\; Highside\; drivers \\
V_{fwd_{DCP}} = 0.75\,V
\]

- Solution

The minimum charge-pump capacitance is determined from equation 7.

Equation 9.

\[
C_{CP1} \geq \frac{50nC \times 3}{12V + 11V - (2 \times 0.75V)} = 7nF
\]

Thus \( C_{CP1} = 10\,nF \) and \( C_{CP2} = 100\,nF \) would be the selected values.
7.4 Voltage supply for low-side pre-drivers

A dedicated low drop regulator is used to generate the VLS_OUT voltage from VSUP. The VLS_OUT voltage is used to supply the low side drivers and can be directly connected to the VLS inputs of each low side driver.

The VLS_OUT — Voltage Regulator Output pin is the output of the integrated voltage regulator. The output voltage is typically VVLS=11 V. The input voltage to the voltage regulator is the VSUP pin. A capacitor should be connected to this pin for stability of the voltage regulator output.

The VLS[2:0] — Voltage supply for low-side pre-driver pins are the voltage supply pins for the three low-side FET pre-drivers. These pins should be connected to the voltage regulator output pin VLS_OUT. The output voltage on VLS_OUT pin is typically 11 V. It is recommended to place a ceramic capacitor as close as possible to each VLS pin.
The current sense amplifier is integrated in the S12ZVM microcontroller for low-side current measurements; the interface consists of two on-chip Op-Amps, each one linked to an independent ADC channel, for simultaneous measurement of two different currents. The current sense amplifier is usually connected as a differential amplifier (refer to figure 23). It senses the current flowing through the external power FET as a voltage across the current sense resistor Rsense.

- The AMPP[1:0] — *Current Sense Amplifier Non-Inverting Input Pins*, are the non-inverting inputs to the current sense amplifiers.
- The AMPM[1:0] — *Current Sense Amplifier Inverting Input Pins*, are the inverting inputs to the current sense amplifiers.
- The AMP[1:0] — *Current Sense Amplifier Output Pins*, are the outputs of the current sense amplifiers. At the MCU level these pins are shared with ADC channels. For ADC channel assignment; see the MCU pinout section in the Reference Manual.

In order to measure both positive and negative currents, it is configured an offset voltage, using VDDA as voltage reference. The sense voltage will be amplified with a gain selected by the external resistors. The output of the current sense amplifier is connected to the non-inverting input of the overcurrent comparator internally.
Figure 29. Current sense amplifier interface

where the transfer function is defined as:

\[ V_{AMPx} = (A \times V_{SENSE}) + \frac{V_{DDA}}{2} \]

where the grain \([A]\) is:

\[ A = \frac{R_2}{R_1} \]

Example

Design Parameters:

\[ I_{SENSE} = 20 \text{ Amp} \]
\[ R_{SENSE} = 10 \text{ m\Omega} \]

- Analysis:

The VAMPx to the maximum sense current, must lower equal than VDDA = 5V, for this example 4.8V on VAMPx will indicate the maximum current by the sense resistor, the gain defined as follows is:

\[ A = \frac{V_{AMPx} - \left(\frac{V_{DDA}}{2}\right)}{I_{RENSE} \times R_{RENSE}} \]

Equation 13.

\[ A = \frac{4.8V - (5V/2)}{20 \text{ Amp} \times 0.01} = 11.5 \]

If \( R_1 = 3.4 \text{ k\Omega} \), and a gain \( A = 11.5 \), then \( R_2 \) is calculated from equation 11:
Equation 14. \[ R_2 = \frac{3.5\, k\Omega}{11.5} = 39.1\, k\Omega \]

The VAMPx is obtained from equation 13.

Equation 15. \[ V_{AMPx} = \left( \frac{39.1\, k\Omega}{3.4\, k\Omega} \right) (20\, Amp \times 0.01\Omega) + \frac{5V}{2} \]

Equation 16. \[ VAMP_x = 2.3V + 2.5V = 4.8V \]

7.6 Shunt resistor - design considerations

Shunt resistors are the most versatile and cost effective means to measure current. But the selection of this component must be careful due to some parameters can affect the sensing current and reading by the microcontroller.

The ideal resistors are considerate purely as resistive device, but the real model of the resistor can be modeled as a network of inductor, capacitor, and resistor that can accurately represent their real-world behavior. These parasitics components as inductance is often an unwanted side-effect and in this context it is called “parasitic inductance”. Parasitic inductances in an AC or switching applications can cause unwanted couplings and high oscillations between the shunt resistor and ADC port. The simulations of this network models can help to understand how the finished circuit will react at high frequencies and allow a designer to avoid unwanted behaviors. Therefore, the shunt resistor should be of a minimal parasitic inductance or high quality.
For the calculation of the maximum power dissipation of the shunt resistor, should be considerate the maximum ambient temperature of the application, due to the derating power by the temperature in the resistor; in other words, the power dissipation allowed is decreases according the temperature increases, this information is indicated in the supplier datasheet of resistor.

Example:

In this example is considerate the electrical characteristics of a shunt resistor BOURNS-BR3FB10L0, and a fictional requirements of current and temperature.

Assumptions:

$I_{MAX} = 16$Amps  
$R_{SENSE} = 10$mΩ @ 5W  
$T_{amb\,MAX} = +150^\circ$C

Analysis:
Due to the derating power dissipation curve the power capability is reduced to 65%, then the maximum power dissipation allowed (to +150°C) is estimated as follows.

Equation 18.  
\[ P_{wr\_max} +150^\circ C = 5W \times 0.65 = 3.25W \]

Due the maximum power dissipated allowed of the resistor is 3.25W to +105°C, and higher than the 2.56W required, the resistor can be used in the application.

### 7.7 Boost converter

The GDU module in the S12ZVM integrates a controller to implement a boost converter. This module implements a switch which is controlled by a selectable frequency of the bus. There are two possible setups for the Boost converter option.

- Connect VBAT as input voltage to the boost converter, in this case an additional diode as VBAT reverse protection is required.
- Connect a Reverse protected Voltage to the converter. In this option D2 is not required, see figure 25.
Figure 33. Options of the Boost circuitry

The boost converter clock which is driving the transistor T1 is derived from the bus clock. This clock can be divided down as described in GDU section in the reference manual. The boost converter also includes a circuit to limit the current through coil. This current limit can be adjusted with the bits GBCL[3:0] in the GDUBCL register.

When the transistor gets connected to ground, the power diode is reverse biased and the current flowing through the coil is increasing and the energy gets stored in the coil. When the transistor gets switched off the current flows through the diode and is charging up the capacitor. The coil current is decreasing again and the voltage on the coil is inverted which leads to a higher output voltage.

The output voltage of the boost converter on VSUP pin is divided down and compared with a reference voltage [V<sub>ref</sub>]. As long as the divided voltage V<sub>VSUP</sub> is below V<sub>ref</sub> the boost converter clock is enabled assuming that GBOE (GDU Boost Option Enable) is set.
7.7.1 BST — boost converter pin

This pin provides the basic switching elements required to implement a boost converter for low battery voltage conditions. This requires external diodes, capacitors and a coil.

Boost Converter Coil selection

The maximum output current, boost frequency and on-time strongly influence the Coil inductance value. The average current in the coil is defined as follows.

\[
IL_{AVG} = I_{OUT} \times \frac{V_{OUT}}{V_{IN}}
\]

Equation 19.

The minimum combination of inductance and switching frequency for continuous current in the boost converter is defined as follows

\[
L_{MIN} = \frac{V_{OUT}}{I_{OUT}} \left( \frac{D(1-D)^2}{2f_{SW}} \right)
\]

Equation 20.

Where the duty ratio, is determined as:

\[
D = 1 - \frac{V_{IN}}{V_{OUT}}
\]

Equation 21.

From a design perspective, it is useful to express L in terms of a desired \(\Delta I_L\):

\[
L = \frac{V_{IN}D}{\Delta I_L f_{SW}}
\]

Equation 22.

Where:

\(\Delta I_L\) — Estimated inductor ripple current = (0.2 to 0.4)\(\times IL_{AVG}\)

Boost converter capacitor selection

To provide relatively smooth DC voltage to the load, the output capacitor in a boost converter must absorb pulsating ripple current. For this to occur, the impedance of the capacitor at the switching frequency and the ESR of the capacitor must be low enough to keep the ripple voltage across the capacitor very small as compared to the average output voltage. The output capacitance in terms of output voltage ripple yields is defined as follows:

\[
C_{OUT} = I_{OUT} \times \frac{D}{f_{SW} \Delta V_0}
\]

Equation 23.

Diode Rectifier Selection

The rectifier must be capable of handling the capacitor’s peak input current and of dissipating the rectifier’s average power—the rectifier voltage drop times the load current. The voltage breakdown of the device must be greater than the output voltage plus some margin. The typical choice for a rectifier in applications with low output voltage is a low-capacitance schottky diode. If the output voltage is high, a fast-recovery diode is an alternate possibility. For converters operating in CCM, a diode with a soft-recovery characteristic will minimize EMI.

Example:

- Design requirements:
\[ V_{IN} = 3.5 \, V \]
\[ V_{OUT} = 11 \, V \]
\[ I_{OUT} = 70 \, mA \]
\[ \%\Delta I_L = 20\% \]
\[ \%\Delta V_O = 0.01\% \]
\[ f_{SW} = 500 \, kHz \]

- Solution:

First, determine the duty ratio from equation 19.

**Equation 24.**

\[ D = 1 - \frac{3.5 \, V}{11 \, V} = 0.6818 \]

If the switching frequency is selected at 25 kHz to be above the audio range, then the minimum inductance for continuous current is determined from equation 20.

**Equation 25.**

\[ L_{MIN} = \frac{11 \, V}{70 \, mA} \left( \frac{0.6818(1-0.6818)^2}{2(500 \, kHz)} \right) = 10.847 \, uH \]

The minimum capacitance required to limit the output ripple voltage to 0.01 percent is determined from equation 21.

**Equation 26.**

\[ C_{OUT} = 70 \, mA \times \frac{0.6818}{(500 \, kHz)11 \, mV} = 8.7 \, uf \]

The average inductor current is determined from equation 17.

**Equation 27.**

\[ I_{LAVG} = 70 \, mA \times \frac{11V}{3.5V} = 220 \, mA \]

The variation in inductor current to meet the 20 percent specification is then \( \Delta I_L = 0.2(220 \, mA) = 44 \, mA \). The inductance is then determined from Equation 20.

**Equation 28.**

\[ L = \frac{V_{IN}D}{\Delta I_{L}f_{SW}} = \frac{(3.5V)(0.6818)}{(44mA)(500kHz)} = 108.5 \, uH \]
Figure 34. BOOST Converter – Pspice Simulation A) Using a minimum inductor value, $L_{MIN} = 10.874 \, \text{uH}$ and B) Using a $L = 108.5 \, \text{uH}$
8 CAN physical layer

The physical layer characteristics for CAN are specified in ISO-11898-2. This standard specifies the use of cable comprising parallel wires with an impedance of nominally 120 Ω (95 Ω as minimum and 140 Ω as maximum). The use of shielded twisted pair cables is generally necessary for electromagnetic compatibility (EMC) reasons, although ISO-11898-2 also allows for unshielded cable. A maximum line length of 40 meters is specified for CAN at a data rate of 1 Mb. However, at lower data rates, potentially much longer lines are possible. ISO-11898-2 specifies a line topology, with individual nodes connected using short stubs.

Though not exclusively intended for automotive applications, CAN protocol is designed to meet the specific requirements of a vehicle serial data bus: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth.

Each CAN station is connected physically to the CAN bus lines through a transceiver device. The transceiver is capable of driving the large current needed for the CAN bus and has current protection against defective CAN or defective stations. A typical CAN system with an S12Z microcontroller is shown in figure 27.

![Figure 35. CAN system](image)

The S12ZVM family has a version with an on-chip CAN physical transceiver and a dedicated power supply using an external ballast transistor. Having these modules on-chip helps reduce the total amount of components required to implement CAN communication.

Like most others CAN physical transceivers, the CANH, CANL and SPLIT pins are available for the designer to terminate bus depending on the application. The figure 28 and figure 29 show examples of the CAN node terminations.
Figure 36. CAN physical transceiver circuit

Figure 37. CAN Physical transceiver circuit with common mode choke
8.1 CAN components data

Table 10. CAN components

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="guard-track.png" alt="Guard Track" /></td>
<td>Denotes a guard track next to a high/medium speed track. Guard tracks are connected such that each end of the track is connected to ground. A guard track should be connected to the ground plane at least every 500 mils. Spacing from any protected conductor and the guard track must not exceed 20 mils.</td>
</tr>
<tr>
<td>CBUS1 and CBUS2</td>
<td>The Capacitors CBUS1 and CBUS2 are not specifically required. They may be added for EMC reasons, in which case the maximum capacitance from either bus wire to ground must not exceed 300 pF total. If zener stacks are also needed, the parasitic capacitance of the zener stacks must also be included in the total capacitance budget.</td>
</tr>
<tr>
<td>Z1 and Z2</td>
<td>The zener stacks Z1 and Z2 could be required to satisfy Automotive EMC requirements (ESD in particular). These devices should be placed close to the connector.</td>
</tr>
<tr>
<td>RTERM1, RTERM2 and CCOM1</td>
<td>Depending on the position of the node within the CAN network it might need a specific termination. RTERM1, RTERM2 and CCOM1 must be that they assist in having an overall cable impedance. On a bus implementation of a CAN network only the two nodes on the two ends of the bus have terminator resistors. The nodes not placed on the end of the CAN bus do not have termination. A thorough analysis is required to maintain this requirement of the CAN networks. The SPLIT pin on the transceiver is optional and the designer might choose not to use it. This pin helps stabilize the recessive state of the CAN bus and can be enabled or disabled by software when required.</td>
</tr>
<tr>
<td>LBUS1 – Common mode choke</td>
<td>A common node choke on the CANH and CANL lines can help reduce coupled electromagnetic interference and needed to satisfy Automotive EMC requirements. This choke, together with transient suppressors on the transceiver pins can greatly reduce coupled electromagnetic noise, and high-frequency transients. LBUS1 is not specifically required</td>
</tr>
</tbody>
</table>

8.1.1 CAN termination

In a transmission line, there are two current paths, one to carry the currents from the driver to the receiver and another to provide the return path back to the driver. In the CAN transmission lines is more complex because there are two signals that are sharing a common termination as well as a ground return path. For reliable CAN communications, it is essential that the reflections in the transmission line be kept as small as possible. This can only be done by proper cable termination. Figure 30 and figure 31 demonstrates two CAN termination schemes.
Reflections happen very quickly during and just after signal transitions. On a long line, the reflections are more likely to continue long enough to cause the receiver to misread logic levels. On short lines, the reflections occur much sooner and have no effect on the received logic levels.

8.1.1.1 Parallel termination

In CAN applications, both ends of the bus must be terminated because any node on the bus may transmit/receive data. Each end of the link has a termination resistor equal to the characteristic impedance of the cable, although the recommended value for the termination resistors is nominally 120 Ω (100 Ω as minimum and 130 Ω as maximum).

There should be no more than two terminating resistors in the network, regardless of how many nodes are connected, because additional terminations place extra load on the drivers. ISO-11898-2 recommends not integrating a terminating resistor into a node but rather attaching standalone termination resistors at the furthest ends of the bus. This is to avoid a loss of a termination resistor if a node containing that resistor is disconnected. The concept also applies to avoiding the connection of more than two termination resistors to the bus, or locating termination resistors at other points in the bus rather than at the two ends.

8.1.1.2 Parallel termination with common-mode filtering

To further enhance signal quality, split the terminating resistors at each end in two and place a filter capacitor, CSPLIT, between the two resistors. This filters unwanted high frequency noise from the bus lines and reduces common-mode emissions.
9 LIN Interface Circuit

The Local Interconnect Network (LIN) is a serial communication protocol, designed to support automotive networks. As the lowest level of a hierarchical network, LIN enables cost-effective communication with sensors and actuators when all the features of CAN are not required.

The LIN Physical Layer module includes the following distinctive features:

- Compliant with LIN Physical Layer 2.2 specification.
- Compliant with the SAE J2602-2 LIN standard.
- Standby mode with glitch-filtered wake-up.
- Slew rate selection optimized for the baud rates: 10.4 Kbit/s, 20 Kbit/s and Fast Mode (up to 250 Kbit/s).
- Switchable 34 kΩ/330 kΩ pull up resistors (in shutdown mode, 330 kΩ only)
- Current limitation for LIN Bus pin falling edge.
- Overcurrent protection.
- LIN TxD-dominant timeout feature monitoring the LPTxD signal.

The LIN transmitter is a low-side MOSFET with current limitation and overcurrent transmitter shutdown. A selectable internal pull up resistor with a serial diode structure is integrated, so no external pull up components are required for the application in a slave node. To be used as a master node, an external resistor of 1 kΩ must be placed in parallel between VLINSUP and the LIN Bus pin, with a diode between VLINSUP and the resistor. The fall time from recessive to dominant and the rise time from dominant to recessive is selectable and controlled to guarantee communication quality and reduce EMC emissions. The symmetry between both slopes is guaranteed.

**NOTE**

According to the maskset of the S12ZVML the reference of the LIN Physical Layer’s power supply can vary from HD or VSUP. Please refer chapter “Device Overview” in the Reference Manual.

Typical applications for LIN include switches, actuators (e.g., window lift and door lock modules), body control electronics for occupant comfort (e.g., door, steering wheel, seat and mirror modules), motors, and sensors (e.g., in climate control, lighting, rain sensors, smart wipers, intelligent alternators and switch panels).

![Figure 40. LIN Bus topology](image-url)
The LIN bus topology utilizes a single master and multiple nodes, as shown below. Connecting application modules to the vehicle network makes them accessible for diagnostics and service.

![Circuit diagram for LIN interface](image)

Figure 41. Circuit diagram for LIN interface

### 9.1 LIN components data

#### Table 11. LIN components

<table>
<thead>
<tr>
<th>Reference</th>
<th>Part</th>
<th>Mounting</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMLIN</td>
<td>Diode</td>
<td>Mandatory only for master ECU</td>
<td>Reverse Polarity protection from LIN to VSUP.</td>
</tr>
</tbody>
</table>
| RML1 and RML2 | Resistor: 2 kΩ  
Power Loss: 250 mW  
Tolerance: 1%  
Package Size: 1206  
Requirement: Min Power rating of the complete master termination has to be ≥ 500 mW | Mandatory only for Master ECU | For Master ECU  
If more than 2 resistors are used in parallel, the values have to be chosen in a way that the overall resistance RM of 1 kΩ and the minimum power loss of the complete master termination has to be fulfilled.  
For Slave ECU  
RMLIN1 and RMLIN2 are not needed on the PCB layout |
| C1        | Capacitor: Slave ECU: typically 220 pF  
Master ECU: from 560 pF up to approximately ten times that value in the slave node [C_{SLAVE}], so that the | Mandatory | The value of the master node has to be chosen in a way that the LIN specification is fulfilled. |
<table>
<thead>
<tr>
<th>Reference</th>
<th>Part</th>
<th>Mounting</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>C2</td>
<td>Capacitor:</td>
<td>Optional</td>
<td>Mounting of the optional part only allowed if there is an explicit written permission of the respective OEM available. Place close to the connector.</td>
</tr>
<tr>
<td></td>
<td>Package Size: 0805</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESD1</td>
<td>ESD Protection</td>
<td>Optional</td>
<td>Layout pad for an additional ESD protection part. Mounting of the optional part only allowed if there is an explicit written permission of the respective OEM available. Place close to the connector.</td>
</tr>
<tr>
<td></td>
<td>Package Size: 0603 -0805</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

10 Unused pins

Unused digital pins can be left floating. To reduce power consumption, it is recommended that these unused digital pins are configured as inputs and have the internal pull resistor enabled. This will decrease current consumption and susceptibility to external electromagnetic noise. ADC unused pins should be grounded to reduce leakage currents. The EXTAL and XTAL pins default reset condition is to have pull-downs enabled. These pins should be connected to ground if not used.

The voltage regulator controller pin BCTL should be left unconnected if not used, and the VDDX voltage regulator must be configured to operate with the internal power transistor by setting the appropriate register (CPMUVREGCTL register, bit EXTXON = 0, bit INTXON = 1). If the VDDC regulator is not used, the VDDC pin must be shorted with VDDX, and the BCTLC pin must be left unconnected.

GDU pins BST, CP, and VCP must be left unconnected if not used. VSSB must always be connected to ground, even if the boost DC/DC converter is not used. The pins corresponding to unused phases (VBSx, HGx, HSx, VLSx, LGx, LSx) should be left open.
11 General board layout guidelines

11.1 Traces recommendations

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner and the characteristic impedance changes. This impedance change causes reflections. Avoid right-angle bends in a trace and try to route them with at least two 45° corners. To minimize any impedance change, the best routing would be a round bend, as shown in figure 34.

![Diagram showing incorrect and correct bending of traces]

**Figure 42. Poor and correct way of bending traces in right angles**

To minimize crosstalk, not only between two signals on one layer but also between adjacent layers, route them 90° to each other.

Complex boards need to use vias while routing; you have to be careful when using them. These add additional capacitance and inductance, and reflections occur due to the change in the characteristic impedance. Vias also increase the trace length. While using differential signals, use vias in both traces or compensate the delay in the other trace.

11.2 Grounding

Grounding techniques apply to both multi-layer and single-layer PCBs. The objective of grounding techniques is to minimize the ground impedance and thus to reduce the potential of the ground loop from circuit back to the supply.

- Route high-speed signals above a solid and unbroken ground plane.
- Do not split the ground plane into separate planes for analog, digital, and power pins. A single and continuous ground plane is recommended.
- There should be no floating metal/shape of any kind near any area close to the microcontroller pins. Fill copper in the unused area of signal planes and connect these coppers to the ground plane through vias.
11.3 EMI/EMC and ESD considerations for layout

These considerations are important for all system and board designs. Though the theory behind this is well explained, each board and system experiences this in its own way. There are many PCB and component related variables involved.

This application note does not go into the electromagnetic theory or explain the whys of different techniques used to combat the effects, but it considers the effects and solutions most recommended as applied to CMOS circuits. EMI is radio frequency energy that interferes with the operation of an electronic device. This radio frequency energy can be produced by the device itself or by other devices nearby. Studying EMC for your system allows testing the ability of your system to operate successfully counteracting the effects of unplanned electromagnetic disturbances coming from the devices and systems around it. The electromagnetic noise or disturbances travels via two media: conduction and radiation.
The design considerations narrow down to:

- The radiated & conducted EMI from your board should be lower than the allowed levels by the standards you are following.
- The ability of your board to operate successfully counteracting the radiated & conducted electromagnetic energy (EMC) from other systems around it.

The EMI sources for a system consists of several components such as PCB, connectors, cables, etc. The PCB plays a major role in radiating the high frequency noise. At higher frequencies and fast-switching currents and voltages, the PCB traces become effective antennas radiating electromagnetic energy; e.g., a large loop of signal and corresponding ground. The five main sources of radiation are: digital signals propagating on traces, current return loop areas, inadequate power supply filtering or decoupling, transmission line effects, and lack of power and ground planes. Fast switching clocks, external buses, PWM signals are used as control outputs and in switching power supplies. The power supply is another major contributor to EMI. RF signals can propagate from one section of the board to another building up EMI. Switching power supplies radiate the energy which can fail the EMI test. This is a huge subject and there are many books, articles and white papers detailing the theory behind it and the design criteria to combat its effects.

Every board or system is different as far as EMI/EMC and ESD issues are concerned, requiring its own solution.

However, the common guidelines to reduce an unwanted generation of electromagnetic energy are as shown below:

- Ensure that the power supply is rated for the application and optimized with decoupling capacitors.
- Provide adequate filter capacitors on the power supply source. The bulk/bypass and decoupling capacitors should have low equivalent series inductance (ESL).
- Create ground planes if there are spaces available on the routing layers. Connect these ground areas to the ground plane with vias.
- Keep the current loops as small as possible. Add as many decoupling capacitors as possible. Always apply current return rules to reduce loop areas.
- Keep high-speed signals away from other signals and especially away from input and output ports or connectors.

12 References

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer’s technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, I2C BUS, ICODE, JCOP, LIFE VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTlx, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, AltIVec, C-5, CodeTest, CodeWarrior, ColdFire, ColdFire+, C-Ware, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QoriQ, QoriQ Qonverge, Ready Play, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, SMARTMOS, Tower, TurboLink, and UMEMS are trademarks of NXP B.V. All other product or service names are the property of their respective owners. ARM, AMBA, ARM Powered, Artisan, Cortex, Jazelle, Keil, SecurCore, Thumb, TrustZone, and µVision are registered trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. ARM7, ARM9, ARM11, big.LITTLE, CoreLink, CoreSight, DesignStart, Mali, mbed, NEON, POP, Sensinode, Socrates, ULINK and Versatile are trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

Document Number: AN5207
Rev. 2
12/2017