MPC5675K Hardware Design Guide

by: Tomas Kulig

1 Introduction

This document summarizes necessary information to design the board based on MPC5675K. It describes the differences of internal and external power supply mode, decoupling of power supplies, and boot configuration.

2 Power sequencing

Power rail sequencing recommendations (Power Up):
- Power up all VDD_HV_xxx rails before VDD_LV_xxx rails
- Power up all VDD_HV_xxx rails simultaneously
- Power up all VDD_LV_xxx rails simultaneously

Power rail sequencing recommendations (Power Down):
- Power down VDD_LV_xxx rails before VDD_HV_xxx rails
- Power down all VDD_LV_xxx rails simultaneously
- Power down all VDD_LV_xxx rails simultaneously

2.1 Power supply modes
MPC5675K implements two power supply modes namely internal and external mode. The state on VREG_INT_ENABLE pin selects the power supply mode. There are internal weak pull downs (100K) on VREG_INT_ENABLE_B and RESET_SUP_B. The following table summarizes the differences between both modes.

### Table 1. Power Supply modes

<table>
<thead>
<tr>
<th>Power Supply Modes</th>
<th>Package Pins</th>
<th>Power On Reset Source</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Internal VREG Mode</strong></td>
<td>VREG_INT_ENABLE_B</td>
<td>Not used. Tie to VSS</td>
<td>Internal POR enabled. All internal LVDs and HVD enabled. VDD_LV_xxx rail is supplied by internal VREG.</td>
</tr>
<tr>
<td></td>
<td>RESET_SUP_B</td>
<td>Internal VREG output that controls the gate of external SMPS pMOS</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VREG_CTRL</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>External VREG Mode</strong></td>
<td>High level on this pin selects external VREG mode</td>
<td>Power On Reset Source (RESET_SUP_B shall be protected by a 10 kOhm series/pull up resistor depending on POR generator output push/pull or open drain)</td>
<td>Internal VREG in bypass mode. LVD and HVD for core voltage disabled out of reset. LVDs for high voltage rails enabled. VDD_LV_xxx needs to be regulated by external voltage regulator.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Not used. Pull up to VDD_HV_PMU</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>RESET_SUP_B (must be asserted as long as core voltage is outside of its valid range of operation) and internal HV POR</td>
<td></td>
</tr>
</tbody>
</table>

Why external LVDs are required if core supply is regulated externally:
- Margin required between external voltage and internal voltage (voltage drop over bond wires)
- Internal IR drop between LVD location and location of lowest voltage (dynamic conditions in different modes of operation)
- Limited accuracy of internal bandgap before trimming
- Hysteresis between rising edge (need to come out of reset) and falling edge of LVD (detection of minimum guaranteed operating range)
- Limited guaranteed operating range of given technology (especially analog IP)

MPC5675K dual supply concept:
- Separate internal VREG operation from external VREG operation
- One dedicated pin to select between internal or external VREG mode
- Optimize internal core voltage LVD and HVD thresholds for internal VREG operation
- In external VREG mode internal core voltage, LVDs and HVD can be enabled by software after reset with adjusted thresholds to allow redundant operation to external LVDs (second level of detections)
- All LVDs and HVD are supplied by VDD_HV_PMU

### 2.1.1 Internal VREG mode

1.2 V core supply is regulated by an internal SMPS regulator with external power components.

PMU related signals in internal VREG mode:
- VREG_INT_ENABLE_B low level selects internal VREG mode
- VREG_CTRL used to control gate of external pMOS
• RESET_B used as bidirectional functional reset. No POR functionality. It can be used by debugger to determine start of instruction execution
• RESET_SUP_B not used. It should be tied to VSS

Sequencing:
• Internal PMU will start generating core voltage as soon as PMU supply is valid

LVDs and HVD
• All internal LVDs and HVD active

VREG PCB layout is critical for efficient and reliable PMU operation. NXP can assist in PCB layout design and review process. Ensure supplies for PMC and Ballast are star routed. Please Review the application note AN3898.

The parameters of used components is summarized in the table below.

**Table 2. Internal VREG mode circumstance component list**

<table>
<thead>
<tr>
<th>Part name</th>
<th>Part Type</th>
<th>Nominal value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>U11</td>
<td>SUD50P04 / SQD50P04 pMOS</td>
<td>2 A - 40 V</td>
<td>Vishay TM low threshold p-MOS, Vth &lt; 2.5 V, Rdson@4.5 V &lt; 20 mOhm, Cg &lt; 5 nF</td>
</tr>
<tr>
<td>D8</td>
<td>SS8P3L Schottky</td>
<td></td>
<td>Vishay TM low Vf Schottky diode</td>
</tr>
<tr>
<td>L8</td>
<td>inductor</td>
<td>3.9 µH -1.5 A</td>
<td>Buck shielded coil low ESR</td>
</tr>
<tr>
<td>C129</td>
<td>capacitor</td>
<td>4 x 2.2 µF</td>
<td>Filter capacitor</td>
</tr>
<tr>
<td>C137</td>
<td>Capacitor (DNP)</td>
<td>X times 0.1 µF - &gt; 16 V</td>
<td>Ceramic–See VDD_LV_COR slides for more details on placement and quantity</td>
</tr>
<tr>
<td>C133</td>
<td>capacitor</td>
<td>X times 0.1 µF - &gt; 16 V</td>
<td>Ceramic–See VDD_LV_COR slides for more details on placement and quantity</td>
</tr>
<tr>
<td>C52</td>
<td>capacitor</td>
<td>0.1 µF - 20 V</td>
<td>Filter capacitor</td>
</tr>
<tr>
<td>C50</td>
<td>capacitor</td>
<td>10 µF - 20 V</td>
<td>Filter capacitor</td>
</tr>
<tr>
<td>R28</td>
<td>Resistor</td>
<td>20 k – 100 k</td>
<td>Pull up for power p-MOS gate</td>
</tr>
</tbody>
</table>

*Table continues on the next page...*
The voltage rating of 20 V or higher is recommended for the SMPS input capacitors (C45, C174, C50 and C52), as these capacitors are exposed to the high current switching of the drain, therefore voltage peaks might be high under heavy load conditions. It is critical that capacitor C45 have a very low ESR and a high bandwidth of at least 50 MHz to dampen higher order harmonics of the SMPS.

2.1.1.1 Capacitor ratings

General Remarks on Capacitor Voltage Ratings:
- The following recommendation assumes that all capacitors used are ceramic capacitors.
- The reason for a proposed voltage rating which is higher than its nominal operating voltage is primarily driven by the higher pulse current capability of capacitors with higher voltage ratings compared to capacitors with the same capacitance but lower voltage ratings.
- Tentatively a higher voltage rating is recommended for capacitors with higher capacitance values as they typically have a lower ESR which leads to higher pulse currents through the capacitor. On the other side those capacitors also allow higher energy densities due to their bigger size. Based on that a detailed analysis with information from the capacitor manufacturer is a recommended way to determine the minimum required voltage rating for a given capacitor and a given pulse current exposure over lifetime.
A more detailed analysis is also recommended to be executed with more detailed data from the capacitor manufacturers on the capacitor's current surge capabilities over lifetime.

The following figure (source: edn.com) shows the two different current loops of a buck converter. A high di/dt current loop (iCin) on the converter input side and a lower di/dt current loop (iCout) on the output side of the buck converter. Depending on whether a capacitor is used on the input side or at the output side different pulse current capabilities are required for the capacitors used. Typically capacitors with a higher voltage rating also provide a higher pulse current capability at the same capacitance value.

![Buck Converter Power Stage](image)

**Figure 3. Buck Converter Power Stage**

### 2.1.2 External VREG mode

1.2 V core supply is regulated by an an external voltage regulator. PMU related signals in external VREG mode.
- VREG_INT_ENABLE_B high level selects external VREG mode by putting the internal VREG in bypass mode
- VREG_CTRL not used. Tie to VDD_HV_PMU via 100 kOhm pull up. Pull Up might be replaced by 0 Ohm (hard tie) or floating after char (HTOL) results are available
- RESET_B used as bidirectional functional reset. No POR functionality. Can be used by debugger to determine start of instruction execution
- RESET_SUP_B determines POR. Must not be deasserted by external reset generator if core voltage is outside of specified range. Input shall be protected by a 10 kOhm series resistor

**Sequencing**
- See chapter Power sequencing

**LVDs and HVD**
- Core voltage LVD and HVD disabled. Can be enabled by software after start up
- Internal LVDs on high voltage rail are active

**Voltage levels**
- RESET_SUP_B, INT_VREG_ENABLE_B need 3.3 V signal levels
2.1.3 SoC voltages generated with linear regulators

In case when SoC voltages are generated with linear regulators none of the capacitors directly connected to one of the SoC supply rails is exposed to huge pulse currents during system power up or steady system operation. In this case the current through the capacitors is limited by the voltage which slowly ramps up to its nominal value during power on.

For this case NXP recommends a minimum voltage rating for noise filtering and decoupling capacitors of 16 V.

2.1.4 High voltage rails supplied by external SMPS regulator

In case the pulse current capability (voltage rating) of the SMPS output capacitors depend on the type of SMPS selected by the customer for the supply of the high voltage rails. For standard SMPS regulators also a minimum 16 V rating for the output capacitors (capacitors connected to SoC VDD_HV_IO, VDD_HV_FLASH, VDD_HV_ADC, VDD_HV_DRAM, VDD_HV_PDI) is recommended.

The input capacitors pulse current (voltage rating) highly depends on the design of the SMPS and its parameters selected by the customer.

3 Nexus and JTAG

6 pin JTAG Interface IEEE 1149.1 with 3.3 V levels.
- JTAG_RST, weak pull down, dedicated pin
- JCOMP input that provides the ability to share the TAP, internal weak pull down, dedicated pin
- TMS, internal weak pull up, dedicated pin
• TCK, internal weak pull up, dedicated pin
• TDI, internal weak pull up, muxed with GPIO
• TDO, muxed with GPIO

During reset sequence a low level (tbc) on MDO[0] indicates that SoC is ready for debugger communication. No polling required. 22 pin Nexus class 3+ debug interface.

• EVTO_B
• EVTI_B
• MCKO, typical frequency 45 MHz @ 180 MHz core clock
• MSEO_B[1:0]
• RDY_B, can selectively be enabled via JTAG register
• Full port mode with 16 MDO[15:0] signals (FPM)
• Reduced port mode with 12 MDO[11:0] signals (RPM)
• DDR mode supported (tbc after validation)

Nexus Interface is enabled via JTAG configuration setting. All Nexus pins except for MDO[0] muxed with GPIOs and other alternate functions. Default state for muxed Nexus pins after reset is GPIO.

• Nexus pins are automatically muxed from GPIO setting to Nexus functionality when Nexus is enabled via JTAG. This affects:
  • MCKO
  • MSEO_B[1:0]
  • MDO[15:1] in FPM
  • MDO[11:1] in RPM
• Nexus RDY_B can be enabled separately via JTAG TEST_CTRL register bitfield NEX_RDY_PORT_EN, JTAG TEST_CTRL register bitfield NEX_RDY_sel select whether RDY from Core 0 or Core 1 is driven as an output
• Nexus EVTI_B together with EVTO_B can be enabled by a single bit via Nexus PCR register bitfields EVT_EN

For 12 bit or 16 bit MDO port mode, the following Nexus connector is recommended:
• HP25-2 (ASP-148422-01) by Samtec (2 rows with 25 pins each; 0.8 mm pitch)
• Supported by Lauterbach

NXP will provide example schematics. The final connector signal assignment depends on the development tool requirements.

4  Reset considerations

4.1  SoC Power Up Reset Considerations

In internal VREG mode, all the standard GPIOs are kept in High-Z unless none of the following LVDs and HVD detect any under/over voltage condition:
• VDD_LV_COR LVD/HVD
• VDD_HV_IO LVD
• VDD_HV_FLASH LVD
• VDD_HV_ADC LVD
• VDD_HV_PMU LVD

Built in self tests are executed (if enabled) as soon as POR is released
• When no LVD and no HVD is asserted
• Independent of state of RESET_B

The recommended reset circuitry is shown in the Figure 5.
Reset considerations

• External Pull Up as RESET_B is a bidirectional functional reset.
• Tie RESET_SUP_B to VSS.

VDD_LV_CORE LVD and HVD circuitries are enabled from POR.

External VREG Mode
• All standard GPIOs are kept in High-Z unless none of the following LVDs detect any under voltage condition:
  • VDD_HV_IO LVD
  • VDD_HV_FLASH LVD
  • VDD_HV_ADC LVD
  • VDD_HV_PMU LVD
• All standard GPIOs are kept in High-Z if RESET_SUP_B is asserted.
  • RESET_SUP_B must not be released if VDD_LV_XXX rails are out of specified range of operation.

Built in self tests are executed (if enabled) as soon as POR is released
• When no active internal LVD is asserted (3.3V rail LVDs only)
• When RESET_SUP_B is de-asserted

The recommended reset circuitry is shown in the Figure 5.
• Series resistor if POR generator has push pull output
• Pull up resistor to VDD_HV_PMU if POR generator has open collector output

VDD_LV_CORE LVD and HVD circuitries are disabled from POR, but can be enabled by software after SoC is out of reset condition.

![Figure 5. Recommended Reset circuitry](image)

4.2 SoC reset considerations

SAFE Mode
• All standard GPIO pads go to High-Z upon entering Safe_Mode
• Weak pulls can be configured for standard GPIOs to become active in Safe_Mode

The following pads have their input buffers enabled during reset:
• TCK (internal weak pull up)
• TMS (internal weak pull up)
• TDI (internal weak pull up)
• JCOMP (internal weak pull down)
• NMI (internal weak pull up)
• eTimer1_ETC[3] (FAB) (internal weak pull down)
• eTimer0_ETC[4] (ABS[0]) (internal weak pull down)
• eTimer0_ETC[3] (ABS[2]) (internal weak pull down)
The following pads get their input buffers and output buffers enabled automatically after reset:

- FCCU_F_0 (external pull recommended; shall be selected in alignment to configured FCCU “error out protocol”)
- FCCU_F_1 (external pull recommended; shall be selected in alignment to configured FCCU “error out protocol”)

## 5 Clock out pins

Two dedicated clockout signals are available. Both pins muxed between Clock Output Generator and eTimer 2 channel 5.

- BGA 257:
  - Pin B3: GP Fast/Slow pad, 3.3 V
  - Pin F14: PDI Fast pad, 1.8 V – 3.3 V
- BGA 473:
  - Pin B3: GP Fast/Slow pad, 3.3 V
  - Pin E20: PDI Fast pad, 1.8 V – 3.3 V

Other possibility of generating Clkout:

- All FlexPWM timer outputs usable as clockoutput generators
- All eTimer outputs usable as clockoutput generators

Series termination recommended for high frequency outputs to reduce reflections.

## 6 Digital IO pads

MPC5675K implements different pads with different IO capabilities and characteristics. Following pad types are available for nominal 3.3 V operation:

- GP Slow: \( F_{\text{max}} = 4 \text{ MHz} @ 25 \text{ pF} \)
- GP Medium: \( F_{\text{max}} = 40 \text{ MHz} @ 25 \text{ pF} \)
- GP Fast: \( F_{\text{max}} = 72 \text{ MHz} @ 25 \text{ pF} \)
- GP Symmetric: \( F_{\text{max}} = 50 \text{ MHz} @ 25 \text{ pF} \)

Following pad types are available for nominal 1.8 V – 3.3 V (1.62 V – 3.6 V) operation (package dependent):

- PDI Fast
- PDI Medium
- DRAM ODT CTL
- DRAM ACC
- DRAM CLK
- DRAM DQ

Please refer to IBIS models and Data Sheet information for more detailed information on IO characteristic. Refer to Data Sheet and Reference Manual on mapping of package pins to pad information.

## 7 Built in Oscillator XOSC

### 7.1 Crystal / Oscillation mode
The crystal is connected between XTALIN and XTALOUT pins, as shown in the figure below:

Refer to Data Sheet for internal feedback resistor value.

### 7.2 Bypass mode

In this mode, the analog portion of crystal oscillator (amplifier) is disabled. An external clock, compatible to CMOS levels, can be applied at XTALOUT (XTAL). XTALIN (EXTAL) can be tied to VSS or can be left floating. See the figure below:
Refer to Data Sheet for internal feedback resistor value.

8 Boot configuration pins

MPC5675K provides three boot configuration pins which are evaluated during SoC reset sequence.

**Table 3. Boot Configuration Pins**

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>LBGA257 Pad</th>
<th>LBGA473 Pad</th>
<th>Description</th>
<th>Internal weak pull</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAB</td>
<td>P8</td>
<td>Y11</td>
<td>Force Alternate Boot</td>
<td>Pull Down</td>
</tr>
<tr>
<td>ABS[0]</td>
<td>D7</td>
<td>C6</td>
<td>Alternate Boot Selection [0]</td>
<td>Pull Down</td>
</tr>
</tbody>
</table>

Boot configuration pins can be used as GPIOs or alternate functions after boot. For "normal" booting from internal flash (FAB=0), make sure that internal weak pull down is strong enough for potential leakage current generated by external circuitry connected to FAB pin.

**Table 4. Boot possibility**

<table>
<thead>
<tr>
<th>Boot Configuration Pins</th>
<th>Boot Options</th>
<th>Boot Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

*Table continues on the next page...*
Table 4. Boot possibility (continued)

<table>
<thead>
<tr>
<th>Boot Configuration Pins</th>
<th>Boot Options</th>
<th>Boot type</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

9 Special signals

DRAM Reference Pin

- Always needs valid reference level even if DRAM interface is not used.
- Voltage level on this pin is used as comparator reference for DRAM input pads. All alternate functions available on DRAM pins are affected by that.
- BGA 473:
  - Provide 50% voltage level of VDD_HV_DRAM to VDD_HV_DRAM_VREF
- BGA 257:
  - Provide 50% voltage level of VDD_HV_IO to VDD_HV_DRAM_VREF

Figure 8. DRAM Reference Pin Circuitry

Unused Pins (not used in application but present on SoC) are recommended to be put in this configuration:

- Output buffer disabled
- Input buffer disabled
- Weak Pull Down enabled

Reserved Pins (no functionality provided by SoC):

- Reserved pins are internally not connected.
- It is recommended to leave them floating for future compatibility.

10 Decoupling
10.1 Core supply

10.1.1 Internal VREG mode

Place 100 nF circuitry 8 times as close as possible to VDD_LV_COR and VSS_LV_COR pins. Ideal placement at bottom side of PCB between center ball matrix and IO ring.

![Diagram of internal VREG mode](image)

**Figure 9. Core supply decoupling circuitry in internal VREG mode**

Place 20 µF circuitry as close to the coil of the VREG circuitry as possible.

![Diagram of core supply burst capacitor circuitry](image)

**Figure 10. Core supply burst capacitor circuitry**

For more information see Internal VREG mode.

10.1.2 External VREG mode

Place four times the circuitry from the figure **Figure 11** as close as possible to VDD_LV_COR and VSS_LV_COR pins. Ideal placement at bottom side of PCB between center ball matrix and IO ring. One 2.2 µF per package side.
10.1.3 PLL supply

Place caps as close to the corresponding VDD and VSS pin pair. The decoupling circuitry is shown in the figure below:

![Figure 12. PLL supply decoupling circuitry](image)

10.2 Flash Power supply

Place caps as close as possible to the corresponding VDD and VSS pin pair.

![Figure 13. Flash supply decoupling circuitry](image)
10.3 Oscillator supply

Place caps as close as possible to the corresponding VDD and VSS pin pair.

![Oscillator supply decoupling circuitry](image)

**Figure 14. Oscillator supply decoupling circuitry**

10.4 Parallel digital interface supply

Place caps (2x) as close as possible to the corresponding VDD and VSS pin pair.

![PDI supply decoupling circuitry](image)

**Figure 15. PDI supply decoupling circuitry**

10.5 DRAM

10.5.1 DRAM supply

Place caps as close as possible to their corresponding VDD and VSS pin pairs, 4 pairs in total.
10.5.2 DRAM reference supply

Place the circuitry from figure below close to VDD_HV_DRAM_VREF pin. VDD_HV_DRAM_VREF needs to be supplied with 50% of the supply used for VDD_HV_DRAM (BGA473) or 50% of the supply used for VDD_HV_IO (BGA 257). VDD_HV_DRAM_VREF needs to be supplied with a valid voltage level even if the DRAM interface is not used and pins are used with an alternate function.

10.5.3 DRAM VTT supply

Recommended DRAM memory type is mobile DDR which does not use On Die Termination (ODT). Tie VDD_HV_DRAM_VTT to GND. Disable ODT by software if not used.

10.6 General purpose IO supply
Place nF/pF caps as close as possible to the corresponding VDD and VSS pin pair, the values of capacitors depends on the frequency of switching interface.

### 10.6.1 High frequency switching interfaces

For BGA473:
- High speed: A3& C1 (A1, A2, B1, B2), G2 (H2), M4 (L4), U22 (V22), P23 (P22), L23 (L22), H22 (H23), A14 (B14)

For BGA257:
- High speed: High speed or low speed recommendation depends on pin usage in customer application and external load.

![Figure 19. High frequency switching interfaces decoupling circuitry](image)

### 10.6.2 Low frequency switching interfaces

BGA473:
- Low speed: D8 (D9), M2 (N2), T4 (R4), V2 (W2), AB2 (AB1, AC1, AC2), Y13 (Y12), Y20 (AA21), AB22 (AB23, AC22, AC23), L20 (K20), B22 (A22, A23, B23)

BGA257:
- Low speed: High speed or low speed recommendation depends on pin usage in customer application and external load.

![Figure 20. Low frequency switching interfaces decoupling circuitry](image)

### 10.7 ADC

VDD_HV_ADV as common ADC supply (3.3 V). VDD_HV_ADRx as ADC reference voltage (3.3 V or 5.0 V). All references supplies must be at the same supply level - either 3.3 V or 5.0 V.

ADC channels alternatively available as general purpose digital inputs.
• Digital signal input levels allowed up to VDD_HV_ADRx
• Digital input thresholds as for 3.3 V CMOS inputs independent of VDD_HV_ADRx level

Both packages allow four simultaneous A/D conversions. Four common channels are shared between two ADCs. For detailed calculation of required ADC channel input circuitries please refer to MPC5675K DS and RM.

**Table 5. Number of external ADC channels**

<table>
<thead>
<tr>
<th>ADC Number</th>
<th>BGA 257</th>
<th>BGA 473</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>3 channels</td>
<td>9 channels</td>
<td></td>
</tr>
<tr>
<td>0 &amp; 1</td>
<td>4 channels</td>
<td>4 channels</td>
<td>Shared channels. Conversion either by ADC_0 or by ADC_1 because Accurate results cannot be guaranteed if both ADCs are configured to simultaneously sample the same shared channel.</td>
</tr>
<tr>
<td>1</td>
<td>3 channels</td>
<td>9 channels</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>4 channels</td>
<td>4 channels</td>
<td></td>
</tr>
<tr>
<td>2 &amp; 3</td>
<td>4 channels</td>
<td>4 channels</td>
<td>Shared channels. Conversion either by ADC_2 or by ADC_3 because Accurate results cannot be guaranteed if both ADCs are configured to simultaneously sample the same shared channel.</td>
</tr>
<tr>
<td>3</td>
<td>4 channels</td>
<td>4 channels</td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td>22 channels</td>
<td>34 channels</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 21. ADC Channel muxing**
10.7.1 ADC ground

Create analog GND for the ADC as shown in figure below.

![Figure 22. Creating analog ground for ADC](image)

10.7.2 ADC supply voltage

Shared among all four ADCs. Voltage supply must be at 3.3 V. Place 1 µF + 47 nF capacitor pair close between VDD_HV_ADV and VSS_HV_ADV supply pins.

![Figure 23. ADC Supply Voltage Decoupling](image)

10.7.3 ADC reference voltage

Reference supply can be 3.3 V or 5.0 V. All references supplies must be at the same supply either 3.3 V or 5.0 V.

Reference Voltage Supply BGA 257:

- ADC_0 and ADC_2:
  - Share VDD_HV_ADR02, VSS_HV_ADR02
  - Place two 1 µF + 10 nF capacitor pair close to these supply pins
- ADC_1 and ADC_3:
  - Share VDD_HV_ADR13, VSS_HV_ADR13
  - Place two 1 µF + 10 nF capacitor pair close to these supply pins
Reference Voltage Supply BGA 473
- Place one 1 μF + 10 nF capacitor pair close to these supply pins
- ADC_1: VDD_HV_ADR1, VSS_HV_ADR0 (separated reference)
  - Place one 1 μF + 10 nF capacitor pair close to these supply pins
- ADC_2 and ADC_3:
  - Share VDD_HV_ADR23, VSS_HV_ADR23
  - Place two 1 μF + 10 nF capacitor pair close to these supply pins

Figure 24. ADC Reference voltage supply decoupling (BGA257 package)

Figure 25. ADC Reference voltage supply decoupling (BGA473 package)
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