Freescale Semiconductor
Application Note

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MAC57D5xx Hardware Design Guidelines

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1 Introduction

The MAC57D5xx family is the next generation platform of devices specifically targeted to the instrument cluster market using single and dual high-resolution displays. Leveraging the highly successful MPC56xxS product family, NXP is introducing a multi-core architecture powered by ARM® Cortex®-M (for real time) and Cortex-A processors (for applications and HMI), coupled with 2-D Graphics Accelerators (GPU), Heads Up Display (HUD), Warping Engine, Dual TFT display drive, integrated Stepper Motor Drivers and a powerful I/O Processor, that will offer leading edge performance and scalability for cost-effective applications.

The MAC57D5xx requires multiple power supply voltages. A 5 V supply is required if the Stepper Motors or the ADC need to operate at this voltage. Additionally, if a DDR2 memory is included in design, 1.8 V is required for the power supplies and 0.9 V as reference voltage.

This application note shows the options of power supplies for MAC57D5xx and the correct external circuitry required:

- Power supplies, including digital supplies, analog supplies, SRAM standby supply, and phase-locked loop supply
- Proper configuration of the PLL circuitry

Contents

- Other major external hardware required for the device
- Examples of other common external interfaces for communication between physical devices, as well as typical analog circuitry

2 Package options overview

MAC57D5xx is available in two package options. The table below describes the main differences between both packages. For further details please refer to the device Reference Manual.

Table 1. Package differences

Package	Feature differences due to the package

208 LQPF	• Some of the interfaces are multiplexed:
	  • SDR is multiplexed with the secondary video output
	  • Ethernet is multiplexed with the video input interface
	  • LCD interface is multiplexed with various interfaces
	• DDR2 is not available
	• LVDS video interface is not available

516 BGA	Provides maximum performance and dedicated interfaces due to available pin count. • Dedicated TRACE debug port • LVDS/OLDI interface

The decision of which package to use should be based on the number of input/output pins required for the application, whether the external DRAM is required in the system, and the amount of layers that are allowed for the printed circuit board. The table below shows the package size differences. Drawings are available on nxp.com, search for the case outline number shown in the table.

Table 2. Package sizes

Package	Body Size	Pitch	NXP Document Number
208 LQFP	28 mm x 28 mm	0.5 mm	98ASA00649D
516 MAPBGA	27mm x 27 mm	1.0 mm	98ASA00623D

3 Power supplies

MAC57D5xx can be used on various types of applications. Based on system requirements and available power supplies, some applications may require different methods of powering the device. The Table 3 below summarizes the options available for powering the MCUs. The minimum configuration requires a 3.3 V supply, a 1.25 V supply and a few external components to power the device.

3.1 Power supply pins

The table below shows all pins related to power supply along with the voltage range and description. The nominal voltages are shown in the table. The device data sheet should be referenced for the minimum and maximum voltages allowed on each of the pins.

Table 3. Power Supply Pins

Pin name	Voltage Range	Description
VDD12	1.20 V to 1.32 V	Core Logic Low Voltage Supply
VSS	0 V	Core Logic & HV Ground Supply
VDDE_A	3.15 V to 3.6 V	I/O Segment A Voltage Supply
VDDE_B	3.15 V to 3.6 V	I/O Segment B Voltage Supply
VDDE_SDR	3.15 V to 3.6 V	I/O Segment SDR Voltage Supply
VDDE_DDR	1.7 V to 1.9 V	DDR2 DRAM I/O Segment Voltage Supply
DDR_VREF	(VDDE_DDR/2) +/-1%	0.9V DDR2 Reference Voltage
VDDM_SMD	3.15 V to 5.5 V	Stepper Motor Drive Voltage Supply
VPP_TEST	0V	Flash Test Supply / Test Mode Input
VDDA_REF	3.15 V to 5.5 V	SAR ADC High Voltage Reference
VDDEH_ADC	3.15 V to 5.5 V	SAR ADC I/O Segment Voltage Supply
VDDA	3.15 V to 5.5 V	SAR ADC Voltage Supply
VSSA_REF, VSSEH_ADC, VSSA	0V	SAR ADC Low Voltage Reference, Segment and Supply ground
VDD_LP_DEC	-	VDD_LV Decoupling Capacitor
VRC_CTRL	-	PMC Voltage Regulator Control Output (output), it should be left open.

3.1.1 Power supply domains

Some of the supplies can be configured with different supply voltages. In particular, the MCU allows flexibility in the selection of voltage levels on some of the supplies that power input and output pins.

The table below shows the different power supply segments that are available on MAC57D5xx. The modules associated with the pins shown are as per the definitions in the "IO Signal Description and Input Multiplexing Table" spreadsheet in the MAC57D5xx reference manual.

Table 4. Power Domain Table

Power Domain	Voltage Range	Main Functions
VDDE_A Domain	3.3 V	Ethernet, JTAG, QSPI, CAN, SGM
VDDE_B Domain	3.3 V	VOUT, DSPI, FlexTimer, LIN
VDDE_SDR Domain	3.3 V	SDR DRAM
SMD I/O Domain	3.3 V to 5 V	Stepper Motor Control and Stall detection (Stall Detection only valid at 5V)

Table continues on the next page...

Table 4. Power Domain Table (continued)

Power Domain	Voltage Range	Main Functions
ADC I/O Domain	3.3 V to 5 V	ADC
DDR I/O Domain	1.8 V	DDR2 DRAM

3.1.2 Power supply package differences

There are different numbers of pins/balls available for the power supply in each of the different package options. In addition, for some package options, some power supplies are not available. The table below shows, for each package, the number of balls available for power supply input to the device. All supply balls that are available on the package should be connected to a supply voltage.

Table 5. Number of power supply pins versus package

Pin name	Nominal Voltage	208 LQFP	516 BGA
VDD12	1.25 V	8	20
VSS	0 V	12	98
VDDE_A	3.3 V	4	14
VDDE_B	3.3 V	4	15
VDDE_SDR	3.3 V	4	7
VDDE_DDR	1.8 V	NA	12
DDR_VREF	0.9 V	NA	1
VDDM_SMD	3.3 V to 5 V	2	3
VSSM_SMD	0 V	2	NA
VPP_TEST	0 V	1	1
VDDA_REF	3.3 V to 5 V	1	1
VDDEH_ADC	3.3 V to 5 V	1	1
VDDA	3.3 V to 5 V	1	1
VSSA_REF, VSSEH_ADC, VSSA	0 V	3	3
VDD_LP_DEC	-	1	1
VRC_CTRL	-	1	1

3.1.3 Power Supply Bypass Capacitors

The table below lists recommended decoupling capacitors that should be used on the various supply pins. Note that these are general recommendations that attempts to compensate for various board designs. It is not a strict requirement to exactly match these recommendations. It is far more important to select capacitors based on the intended application, temperature, noise, and operating conditions. Make sure to place smaller capacitors closer to the supply pairs and distribute the capacitors evenly around the supply pins.

Table 6. Recommended decoupling capacitors

Supply	Decoupling Capacitors
VDDE_A, VDDE_B, VDDE_SDR, VDDE_DDR, VDDA, VDDEH_ADC, VDDA_REF, DDR_VREF, VDDE_SMD	• 0.1 µF: Close to each VDD/VSS pin pair. • 1 µF: On each side of the chip for each supply domain. • 10 µF: Near for each power supply source (except for VDDM_SMD pins where a higher capacitance value may be needed depending upon motor characteristics).
VDD12	• 0.1 µF: Close to each VDD/VSS pair
VDD_LP_DEC	• 1.0 µF

3.2 Power supply configurations

The table below show the possible options for each one of the power supplies.

Table 7. MAC57D5xx power supplies

Power Supply	Description and Requirements
3.3V Supply	• It is always required • It must be externally provided • Required for Low Power modes
5V Supply	• Only required when 5V I/O circuitry is required like Stepper Motors. • Only SMD and ADC VDD domains accept 5V • It must be externally provided
1.25V Supply	• It is always required • It must be externally provided
1.8V Supply	• Only required when DDR2 is used • It must be externally provided
0.9V Supply	• Only required when DDR2 is used • It can be generated by a simple resistive voltage divider but some designs may require an additional VTT (termination) supply for the control signals.

3.3 External 1.25 V regulation

MAC57D5xx VDD12 requires 1.25 V to be provided by an external supply, VRC_CTRL should be left open.

The PORST pin must be driven until the supplies are stable. This can be accomplished by driving the PORST pin so that when the external VDD12 supply is not stable, PORST is driven LOW externally. Once VDD12 is stable, PORST is driven HIGH. Alternatively, another equally robust solution is to connect PORST pin to VDDE_A supply. In the latter case, multiple voltage monitor resets may be seen during power-up / power-down in presence of a non-monotonic or slow ramp VDD12 supply.

3.3.1 External regulator and low power modes

MAC57D5xx provides means to control the external regulator or power supply being used to supply 1.25 V to the core. There are 3 pins available that can be configured to enable or disable the external power supply:

- PE[9]
- PM[7]
- PM[1]

The signal on the selected pin will be asserted when the device enters into a low power mode to signal the external supply to shut down. These pins are fully configurable using DCF records. The figure below shows a simplified diagram of the connection of the external regulator control signal (EXT_REG_CTRL).

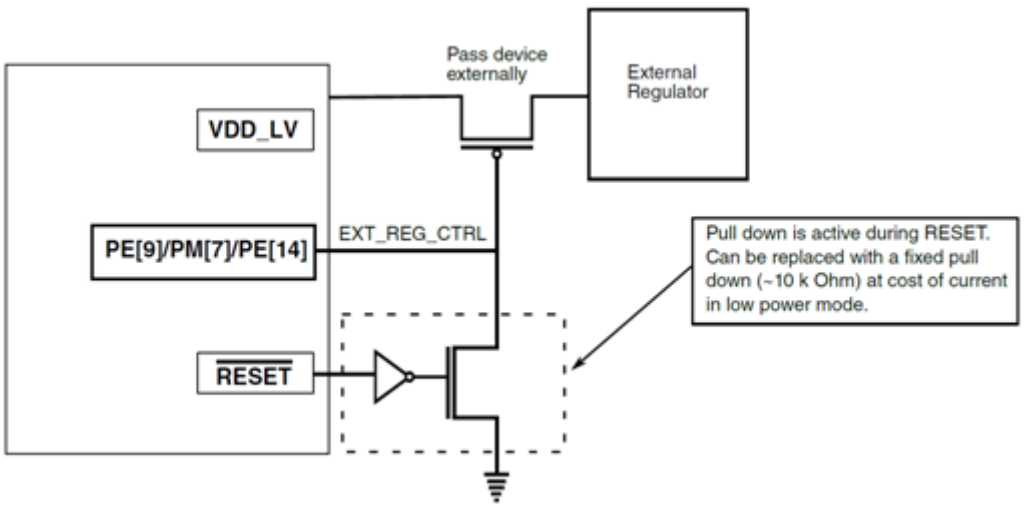


Figure 1. Example diagram for external regulator control

When using the external regulator it may be possible that the regulator asserts the PORST pin when turned off. In the case of low power modes this is not desirable so a mechanism is provided to disable PORST during low power modes. This is configurable using DCF records.

3.4 Power Management Controller (PMC)

The power management controller (PMC) handles all of the on-chip voltage regulators, regulator controllers, power-on reset, and the low-voltage detect (LVD) circuitry.

3.4.1 Power-on Reset

The PMC controls the internal power-on reset (POR) for the MCUs. When the critical power supplies are below minimum levels, MAC57D5xx is held in a reset state. PMC will check that all logic domains are above minimum threshold voltage, referred as LVD, and then release power up for the MC_RGM (Reset Generation Module). Output pins are not driven and inputs are at default value. For details on the state of each pad on reset, refer to the device I/O Signal Description and Input Multiplexing tables attached to the MAC57D5xx reference manual.

The monitors mentioned in table below are active at power up and will gate the power up recovery and prevent exit from POWERUP phase until the minimum voltage level is crossed. The actual voltage levels can be obtained from the device datasheet.

Table 8. Voltage monitors

Symbol	Parameter
VPOR_LV	LV supply power on reset detector
VLVD_LV_PD2_hot	LV supply low voltage monitoring, detecting in the PD2 core (hot) area
VLVD_LV_PD1_hot	LV supply low voltage monitoring, detecting in the PD1 core (hot) area
VLVD_LV_PD0_hot	LV supply low voltage monitoring, detecting in the PD0 core (hot) area
VPOR_HV	HV supply power on reset detector
VLVD_IO_A_LO	HV IO_A supply low voltage monitoring – low range
VLVD_FLASH	Flash HV supply low voltage monitoring

These symbols refer to internal signals in the device which are supplied by the VDD12 and VDDE_A external pins.

Additionally, the PORST pin state must be high to exit from the POWERUP phase.

3.4.2 Power up/down sequencing

As long as the following two requirements are met, there is no power sequencing required among power sources during power up and power down in order to operate within specification:

- Ensure VDD_LV supply ramps up before VDDE_DDR
- In Standby mode, it should be ensured that the VDDE_DDR supply is powered off.

The recommended power supply behavior is as follows: Use 25 V/millisecond or slower rise time for all supplies. Power up each VDDE/VDDEH first and then power up VDD. For power down, drop VDD to 0 V first, and then drop all VDDE/VDDEH supplies.

4 Clock Circuitry

The most important aspects of an accurate clock source require that some care be taken in the layout and design of the circuitry around the crystal and Frequency Modulated Phase Locked Loop (FMPLL) power supplies. Any noise in these circuits can affect the accuracy of the clock source to the FMPLL.

MAC57D5xx provides two options for external oscillators:

- The Fast External Oscillator: Ranging from 8 to 40 MHz, used to accurately generate the clock sources for the PLL or directly drive the clock into the MAC57D5xx modules.
- The Slow External 32 KHz Oscillator: An ultra-low power oscillator that can be used to drive timers such as the Real Time Clock or the LCD module.

The figure below shows the typical connections required for the crystal circuitry.

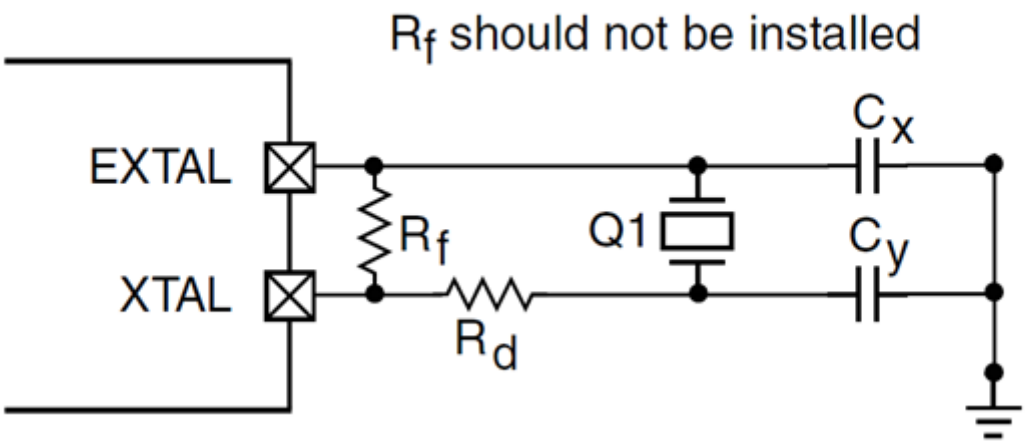


Figure 2. Oscillator Circuitry connections

In the figure above, R_f should not be installed with any current devices or crystals, as there is an internal feedback resistor. Room should be left in the layout in case a resistor is needed in the future for new types of crystals. Since the layout of the module/board can affect the component values required, customers should have their board characterized by their crystal vendor to recommend values for R_d, C_x, and C_y. The values shown in this document should be used as a starting point. These should be re-characterized for any change to the oscillator circuit layout, including routing changes of other circuitry near the crystal circuit.

NOTE

The oscillator circuit should be placed as close as possible to the MCU. In order to minimize signal degradation, the circuitry should be placed entirely on only one PCB layer, avoiding unnecessary vias where possible.

NOTE

Do not allow any signals to cross the crystal connections to the device. Absolutely no high current or high speed signals should be run near any of the crystal components.

NOTE

Other than the connections shown in the above schematics, no other connections should be made to the crystal or EXTAL and XTAL device pins. Do not use XTAL to drive any other circuitry than shown.

The recommendations from the crystal manufacturer will include not only a series resistor value but also the load capacitance required for the crystal (the total crystal load capacitance is usually specified in the crystal data sheet). Keep in mind that the load capacitance is the sum of:

- Physical capacitors (C_x and C_y)
- Capacitance of the MCU
- Capacitive loading of the board (C_{BOARD})
- Pin capacitance (C_{MCU_PIN}) of the MCU EXTAL and XTAL balls (BGA balls are specified as 7 pF maximum)

The requirement for the crystal vendor to measure the customer board is due to the board capacitance effect on the crystal load capacitors.

Generally, the method to calculate the capacitor values to use for C_x and C_y is given by the following:

- $C_A = C_B = 2 \times C_L$
- $C_A = C_X + C_{MCU\_PIN} + C_{BOARD}$
- $C_B = C_Y + C_{MCU\_PIN} + C_{BOARD}$

C_L should come from the crystal specifications (requirements). C_{BOARD} should also include any socket capacitance if a socket is used. This is listed in the device data sheet as the discrete load capacitance to connect to EXTAL and XTAL:

- $C_{L\_EXTAL} = (2 \times C_L) - C_{SOCKET\_EXTAL} - C_{PCB\_EXTAL}$
- $C_{L\_XTAL} = (2 \times C_L) - C_{SOCKET\_XTAL} - C_{PCB\_XTAL}$

In some cases, the crystal vendor may recommend different values for C_X and C_Y (not equal).

5 Reset and Boot

It is common that some microcontrollers use external pins to set up the boot configuration. The MAC57D5xx does not uses any external input pins for boot configuration. Instead, it uses Device Configuration Format (DCF) records to determine boot configuration. DCF records are stored in a specific section of the internal Flash memory. The DCF records not only control the boot and reset behavior of the device, but also control a broad range of functionality. Please check the device RM for further details.

5.1 Pin configuration

Below are the different pins involved in the reset and boot sequences (including low power modes exit):

- PORST: Power-on reset pin. When asserted low, it will cause a destructive reset (as a power on reset). This pin must be held low until all the power supplies are stable. One way to achieve this is connecting PORST to the VDDE_A supply. Since the PORST pin may be asserted low during low power modes and cause an undesirable destructive reset, it is possible to disable it using DCF records.
- RESET: This is an input output pin, driven low in reset mode. Behaves as a weak pull-up after exiting Reset Phase 3. This pin has to be pulled high.
- EXT_REG_SUPPLY: External regulation control pins are available in case the external regulation option is used and turning off the supplies during low power modes is required (typically when STANDBY current consumption is critical). Connect this pin to the enable/disable pin of the external regulator. This pins are configurable using DCF records.
- VPP_TEST: This is a NXP only test mode, all designs must have this pin pulled-down to ground.
- Serial Boot pins: If there is no boot header on the internal flash memory the MAC57D5xx will start the Serial Boot Mode sequence on the PM[9] (Tx) and PM[8] (Rx) pins. Both CAN and UART/LIN are supported.
- Pad Keepers: The device is capable of retaining the output value of some selected pads when the device is in low power. The following pads are capable of this feature: PE[15], PF[0], PF[1] and PM[0]
- Wake up pins: The device is able to wake up from lower power states using different internal and external signals. External signals are available at some pin inputs. Please check the RM to find out which pins have wake up capabilities.
- LCD_PAD: The device is capable of driving an LCD display. To avoid ghosting during startup the device LCD pins are capable of enabling a weak pull down during startup.

The figure below shows a generic configuration for the reset and boot pins in the MAC57D5xx.

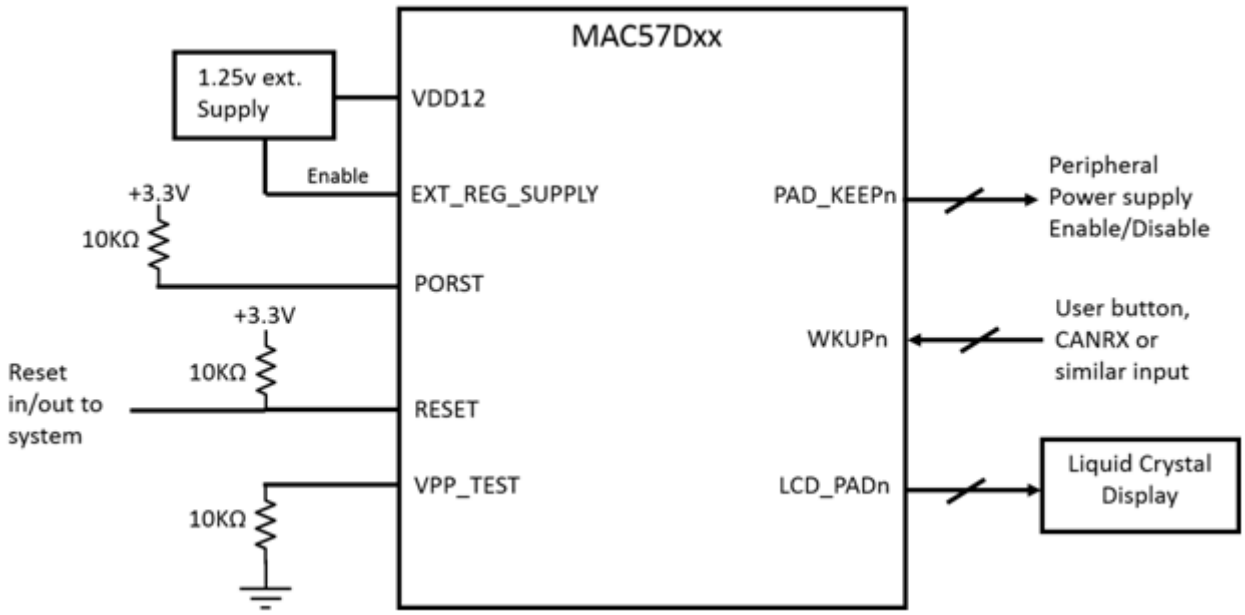


Figure 3. Reset and boot pin configuration example

6 Debug connections

The table below shows the recommended JTAG connectors for different applications for MAC57D5xx

Table 9. Recommended JTAG connectors

Debug Connector Style	Target system part number	Connector type
ARM Standard JTAG (20-pin)	HTST-110-01-L-DV	JTAG Only
ARM Cortex Debug (10-pin)	FTSH-105-01-L-DV-K	JTAG Only
ARM ETM Mictor (38-pin)	Tyco 767054-12	JTAG + ETM
ARM Cortex Debug + ETM (20-pin)	Samtec FTSH-110-01	JTAG + ETM

6.1 JTAG connectors

The ARM Standard JTAG 20-pin connector is considered a legacy connector by ARM and the recommendation is to use the ARM Cortex Debug (10-pin) instead because the 10-pin connector requires less space and has a lower cost while conserving the same functionality. Below is the pinout for both types of connectors.

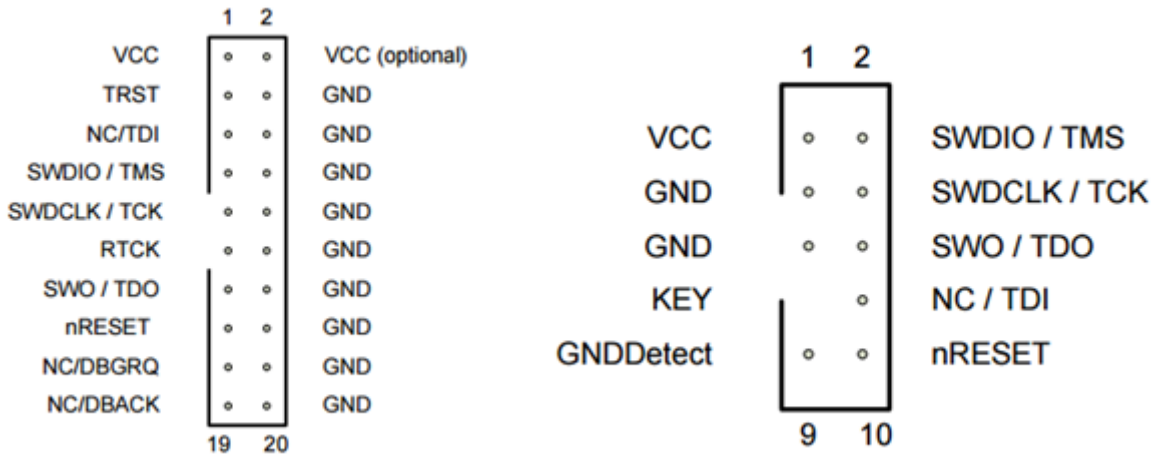


Figure 4. ARM Standard JTAG 20-pin and ARM Cortex Debug Connector pinouts

The MAC57D5xx does not have DBGRQ and DBACK pins, so these pins are left unconnected.

6.2 JTAG+ETM Connectors

The Cortex Debug + ETM Connector (20-pin) is recommended when board space is small and some trace functionality is required. For Multicore and Cortex-A trace debug, the Mictor 38-pin connector has to be used.

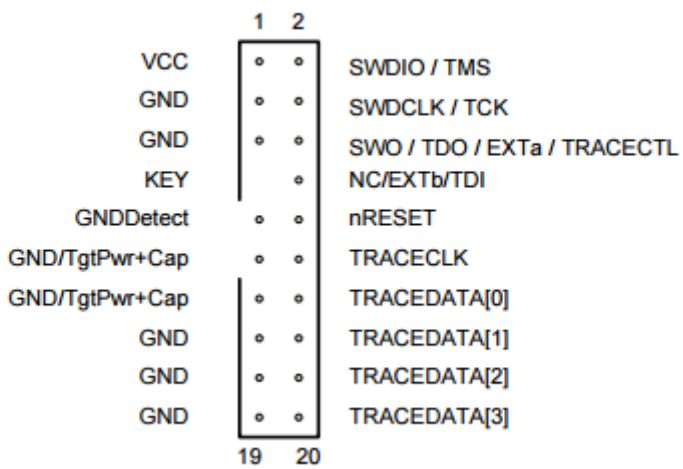


Figure 5. ARM Cortex Debug + ETM 20-pin Connector pinout

For Multicore and Cortex-A trace debugging, the ARM ETM Mictor (38-pin) connector is recommended, since this connector supports the 16bit trace port for maximum bandwidth.

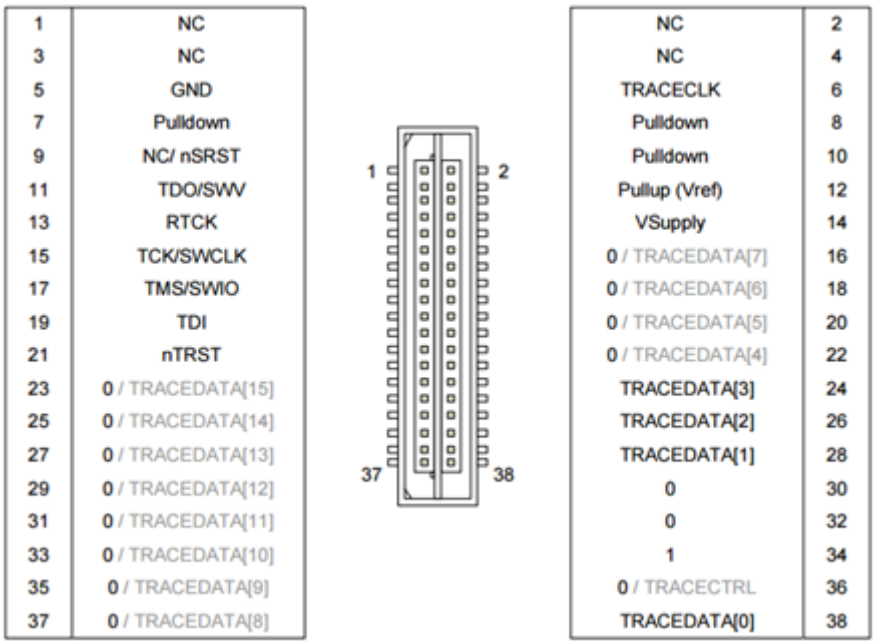


Figure 6. ARM ETM Mictor 38-pin Connector pinout

6.3 Minimum debug external circuitry

6.3.1 Debug pull resistor

In general, other than the connector, no additional circuitry is required for the Nexus/JTAG debug circuitry. The MAC57D5xx devices include internal pull devices that ensure the pins remain in a safe state. However, if there is additional circuitry connected to the JTAG pins, or the signals have long traces, a minimum number of external pull resistors can be added to ensure proper operation under all conditions. Long traces could be affected by other signals, due to crosstalk from high current or high-speed signals. The recommended external resistors are shown in the following table.

Table 10. Optional minimum debug port external resistors

	Resistor direction and value	Description
TRST	10K pullup	Test Reset: is used for an asynchronous reset for the tap controller.
TDI	10K pullup	Test Data In: is the data signal from the debugger to the processor.
TMS	10K pullup	Test Mode Select: is the control signal for the TAP controller
TCK	10K pulldown	Test Clock: is the clock signal from the debugger to the controller

Table continues on the next page...

Table 10. Optional minimum debug port external resistors (continued)

	Resistor direction and value	Description
RTCK	10K pulldown	Return Test Clock: can be used to synchronize the JTAG signals to internal clocks. This signal is optional and typically not required.
TDO	10K pullup	Test Data Out: is the data signal from the controller to the debugger
nRESET	10K pullup	System Reset: this signal fully resets the target. It can be input or output.

6.3.2 Debug buffers

In addition to the pull-up and pull-down resistors, some systems may want to use buffers between the JTAG/ETM connector inputs and the MCU. This will prevent over-voltage conditions from causing damage to the MCU pins. Normal systems should not require this circuitry, but it is helpful in systems that can be exposed to improper connections that provide voltages that are outside the operating conditions of the MCU. A common circuit to use is the Texas Instruments SN74CBTLV38616. This device is a bus switch that implements a bidirectional interface between two terminals with less than 5 Ω of resistance. It should be powered by the same supply that powers the debug port. The device enable should be connected to ground for the interface to be enabled whenever the debug port on the MCU is powered. This circuit provides a high impedance to the tool when the debug port is powered off.

6.4 Debug recommendations

It is recommended that at least the reduced port configuration ETM signals be made available (somewhere) on production boards. This facilitates debugging of new boards and analysis of errors in software, even on boards that have restricted space and normally provide a JTAG-only connection. If the ETM signals are available on the production board, an adapter could be built to provide a Nexus connection on boards that do not have a complete footprint for one of the standard Nexus connectors. Likewise, the JTAG connector does not have to be populated on production boards and could even utilize a smaller connector footprint that could be used with an adapter to the standard debug connections.

6.5 Differences between packages options

MAC57D5xx has different debug capabilities on each of its different packages. The following package specific considerations must be considered when designing the debug interfaces for MAC57D5xx:

Table 11. Debug interface differences between packages

Package	Feature differences due to the package
208 LQFP	• ETM trace pins TRACEDATA0-15, TRACECLK, TRACECTL are multiplexed with the Stepper Motor Control pins, which are commonly connected to low

Table continues on the next page...

Table 11. Debug interface differences between packages (continued)

Package	Feature differences due to the package
	impedance inductors from stepper motors. If the trace debug pins are required, these coils have to be disconnected from the trace signals. • ETM trace pins use the SMD I/O voltage domain, which is typically connected to a 5 V supply when stepper motors are used. JTAG signals are supplied by the VDDE_A voltage domain, which can only be 3.3 V. If the trace debug pins are required, the SMD I/O voltage domain has to be connected to a 3.3 V supply.
516 MAPBGA	• This package has dedicated pins for the Trace debug port. None of the limitations of the 208 LQFP apply to this package.

7 Input/Output pins overview

Since there are many different requirements for the input and output signals of MAC57D5xx, several pin types are used. The table below summarizes the types of pins/pads available on MAC57D5xx. Information on the pad types and signal multiplexing is available in the device Reference Manual and Data Sheet. This section helps interpret this information.

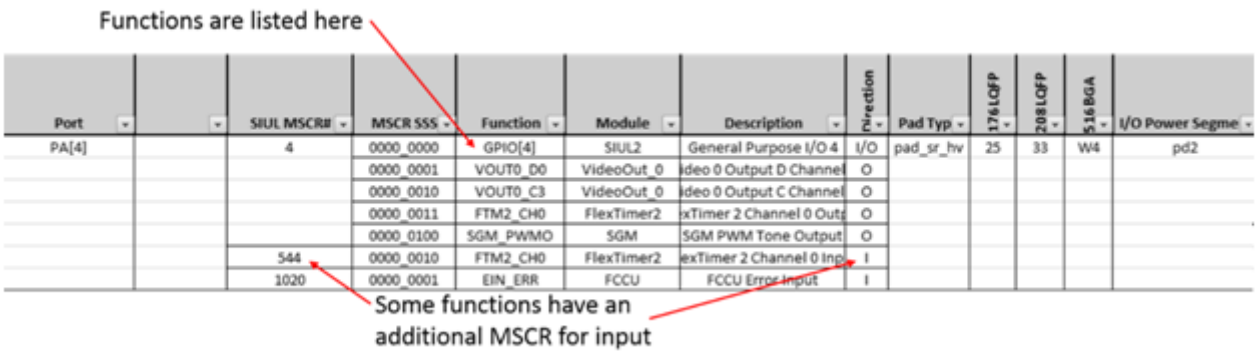
Table 12. MAC57D5xx PAD types

Pad Type	Abbreviation	Description
DDR2 pads	dq, acc_18, clk_18, dq_18	These are especial 1.8 V fast pads used for the DDR2 external interface. This pads are exclusive to the BGA package.
Fast pads	fc_hv	The fast pads are digital pads that allow high speed signals. Generally, these are used for video or memory interfaces.
Analog	isatww_st_hv	These pads are connected to the ADC.
Stepper Motor pads	smc_io_hv	These pads are used to drive the H-bridge for stepper motors and is capable of driving loads with 30 mA. SMC pads are multiplexed with other digital functions.
Slow pads	sr_hv	Most of the peripheral signals are slow speed pads, such as the FlexTimer, and LINFlex. The slow speed pads have slew rate control.
OLDI pads	lvds	These are differential low voltage pads exclusive to the LVDS Video bridge only available in the BGA package.
RSDS pads	rsds	These are differential low voltage pads similar to the lvds interface but these pads are multiplexed with on the video output port with fc_hv and sr_hv pads.

Each of these pad types have programmable features that are controlled in a signal configuration register (MSCR). All pins, except single purpose pins without special properties that need to be controlled, on the device have a MSCR. MSCR controls the function, direction, and other capabilities of the pin.

7.1 Understanding pin multiplexing

A majority of the Input/Output pins on the MCU have multiple functions that are selectable by software. The figure below shows a typical excerpt from the MAC57D5xx IO Signal Multiplexing document (attached to the reference manual). The table in the figure shows the different functions that are available on each pin.



Port		SIUL MSCR#	MSCR SSS	Function	Module	Description	Direction	Pad Typ	176LQFP	208LQFP	516BGA	I/O Power Segme
PA[4]		4	0000_0000	GPIO[4]	SIUL2	General Purpose I/O 4	I/O	pad_sr_hv	25	33	W4	pd2
			0000_0001	VOUT0_D0	VideoOut_0	ideo 0 Output D Channel	O					
			0000_0010	VOUT0_C3	VideoOut_0	ideo 0 Output C Channel	O					
			0000_0011	FTM2_CH0	FlexTimer2	xTimer 2 Channel 0 Outp	O					
			0000_0100	SGM_PWMO	SGM	SGM PWM Tone Output	O					
		544	0000_0010	FTM2_CH0	FlexTimer2	exTimer 2 Channel 0 Inp	I					
		1020	0000_0001	EIN_ERR	FCCU	FCCU Error Input	I					

Figure 7. Typical Device pin multiplexing

The example above shows pin PA[4], that can be used as standard GPIO, Data Enable for Video, FlexTimer and others. By selecting the appropriated SSS value, the pin is configured with the selected function as output. If input functionality is required (FlexTimer), configure the MSCR[544] as shown in the table. Some pins have exclusive function, such as the DDR2 pins, and cannot be configured as GPIO or other function. Still, is required to write to the MSCR register to configure other parameters, like drive strength between others.

Additional information that is important when designing a board is provided in the original spreadsheet. These other fields are:

- Pad Type: This column of the table contains the pad type of the ball/pin. This is required to understand the characteristics of the pin/ball.
- Power Segment: This field will indicate whether this pin will be powered during the different power modes available in the MCU. For example, PD2 pins will be only powered during modes in which the power segment PD2 is enabled.
- Power Domain: This field indicates which power supply is feeding the pin. It is useful to understand what voltage levels the pin can have, in order to pinpoint electrical issues like noise coupling when debugging problems.
- State during Reset and state after reset: The columns for the state of the pin during and after reset could be important in the design of the system. The user needs to ensure that these states do not cause any issues with external circuitry, such as turning on a motor during reset. The table also indicates the state during STANDBY/IOP mode.
- Package Location: These columns show the ball map location of the signal for each of the package types.

7.2 Injection Current

All pins implement protection diodes that protect against electrostatic discharge (ESD). In many cases, both digital and analog pins need to be connected to voltages that are higher than the operating voltage of the device pin. In addition to providing protection from ESD, these diode structures will also clamp the voltage to a diode drop above the supply of that pin segment. This is permissible, as long as the current injection is limited as defined in the device specification. Current can be limited by adding a series resistor on the signal. The input protection diodes will keep the voltage at the pin to a safe level (per the absolute maximum ratings of the device) as long as it is less than the maximum injection current specification.

Additional circuits on the pins can be enabled only by fast ESD transients. In normal operation, these circuits have no effect on the pin characteristics and are triggered by fast high voltage transients. To prevent the turning on of these circuits during normal power-up sequences, the ramp rate of the power supplies (all external supplies) should not exceed 25 V/ms.

Below is an extract from the MAC57D5xx Data Sheet revision 4 dated June 2015. These specifications may change. Consult the latest revision of the data sheet to determine if there have been updates to these specifications.

Table 13. Injection current parameters

Datasheet Table	Parameter	Maximum allowed
Absolute Maximum Ratings	Injected input current on any pin during overload condition	± 5mA
Absolute Maximum Ratings	Absolute sum of all injected input currents during overload condition	± 50mA
Recommended Operating Conditions	Injected input current on any pin during overload condition	± 3mA

The figure below shows a typical digital pin and the protection diodes. Controls for all of the pad options are controlled in the Pad/Pin Configuration Register for the pin.

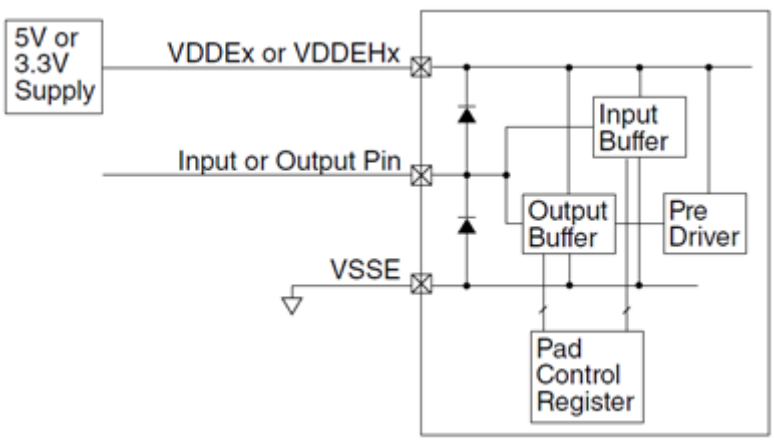


Figure 8. Typical input protection

The value of a series resistor to limit the injected current can be calculated as follows. For a 1 mA injection current limit, a 20 KΩ resistor provides protection for a 20 V DC injection current:

DCmax = 20 kΩ/1 mA = 20 V

This voltage is sufficient for signals that are connected to a typical 12 V battery.

8 SAR ADC

MAC57D5xx contains a single ADC module which supports 12-bit mode as well as 10-bit mode with up to 45 ADC channels. It also supports functions such as multiplexed inputs, normal conversions, injected conversions, and DMA of conversion data to System RAM. The maximum speed of operation of the ADC is 1M Sample/s at 8 0MHz.

The following board schematic and layout guidelines should be followed:

- Isolate the analog power supplies (VDDA) from the digital power supplies
- Isolate analog traces from digital high-frequency traces

- Incorporate robust bypassing of power supplies (analog and digital supplies) to ensure lowest possible voltage ripple on the power supplies
- Use linear power supplies when possible, or minimize or isolate the switching noise when using a switching power supply
- Incorporate low-pass filter on ADC inputs to remove unwanted higher frequency components as shown in the following sections

The ADC requires calibration before it can be used. See the reference manual for more details about the calibration procedure.

For more details about the SAR ADC refer to NXP application notes AN4881, and AN5032 for guidelines on how to handle the ADC circuitry.

NOTE

The aforementioned application notes refer to different NXP devices. These application notes should be used as reference material only. The reference manual and datasheet contain official, specific information on the ADC of MAC57D5xx.

9 Communication Modules

9.1 Example LIN interface for LINFlexD

Local Interconnect Network (LIN) is a commonly used low-speed network interface that consists of a master node communicating with multiple remote slave nodes. Only a single wire is required for communication and is commonly included in the vehicle wiring harness.

On many of the NXP automotive MCUs, the LINFlexD module implements LIN interface. This same module also supports the standard Universal Asynchronous Receiver/Transmitter (UART) functions (with a different physical layer device).

The following figure shows a typical interface implemented using the NXP MC33661 LIN transceiver.

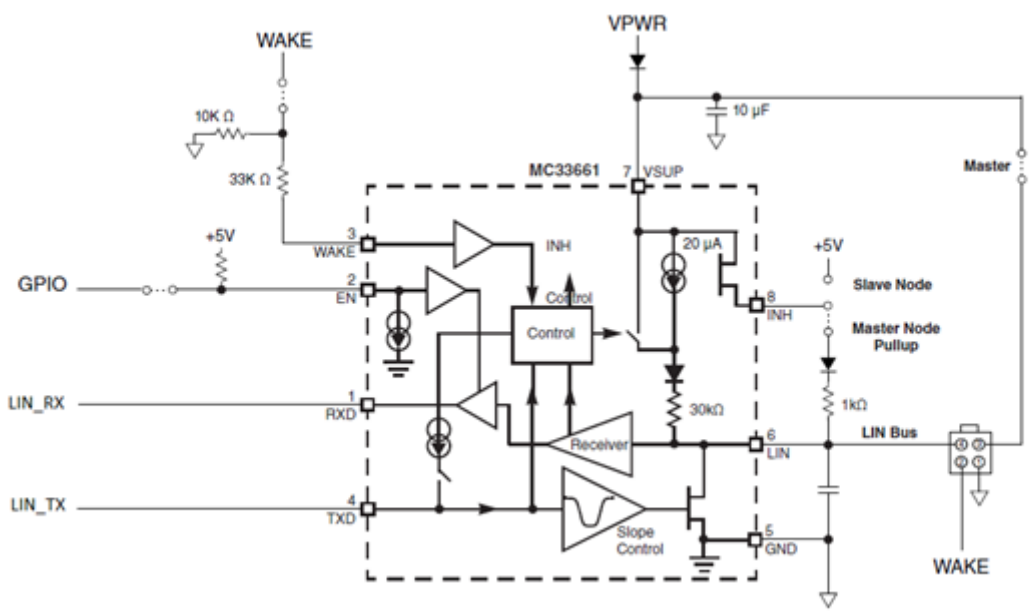


Figure 9. Typical LINFlexD to LIN transceiver connection

There is no standard industry-defined LIN connector. NXP uses a 4-pin Molex connector that includes the LIN bus pin, a power supply source (VPWR), a wakeup signal, and a ground reference. Slave nodes will often implement two connectors to allow a daisy-chain of multiple nodes to be easily implemented. The NXP Molex connector definition is shown in the following table.

Table 14. NXP Molex connector definition

Function	Pin Number	Pin Number	Function
Lin Bus	4	3	VPWR
Wake	2	1	Ground

In a typical system, these pins would be used as follows:

- LIN Bus - This is a single-wire LIN bus that connects the master LIN node and the slave LIN nodes.
- VPWR - This connector input can be used as the power input to a slave node. Care should be taken that sufficient current is available for the total number of LIN slaves that are powered through this connection. In some systems, this may come from the master LIN node.
- Wake - The Wake signal is typically used for each individual slave node to enable the LIN physical interface of that node and enable the power supply (using the INH output) to power up the MCU to perform some action. For example, when the handle on a car door is lifted, turn on the MCU that controls a function inside the vehicle, such as power a smart dome light or enable the controls of a smart seat.
- Ground - Ground reference for the module.

9.2 Example USB to Serial interface for LINFlexD

The RS-232 (TIA/EIA-232-F) standard is a fairly common interface that was once available on nearly all computers. While this interface is disappearing, adapters are available to allow the use of RS-232 peripherals through other interfaces, such as USB. These USB to Serial adapters make it fairly easy to connect to a standard computer for debugging purposes.

On many of the NXP automotive MCUs, the LINFlexD module implements the standard Universal Asynchronous Receiver/ Transmitter (UART) functions. This same module also supports the LIN interface (with a different physical layer device).

The figure below shows the typical connections between the serial port of an MCU and the FT230x USB to Serial transceiver from FTDI Chip (http://www.ftdichip.com/). The transceiver operates from either a 3.3 V or a 5 V supply and includes four configurable I/O pins for different functions, such driving a LED or a SLEEP function. Please check the device manufacturer datasheet for more details.

NOTE

The FT230x device is not rated for the full automotive temperature range of -40 to +105° C and is not intended for automotive applications. This circuit should not be used or populated in a production module intended for automotive use. However, in many cases, the RS-232 interface is intended only as a development interface; therefore the commercial device can be used for prototyping purposes.

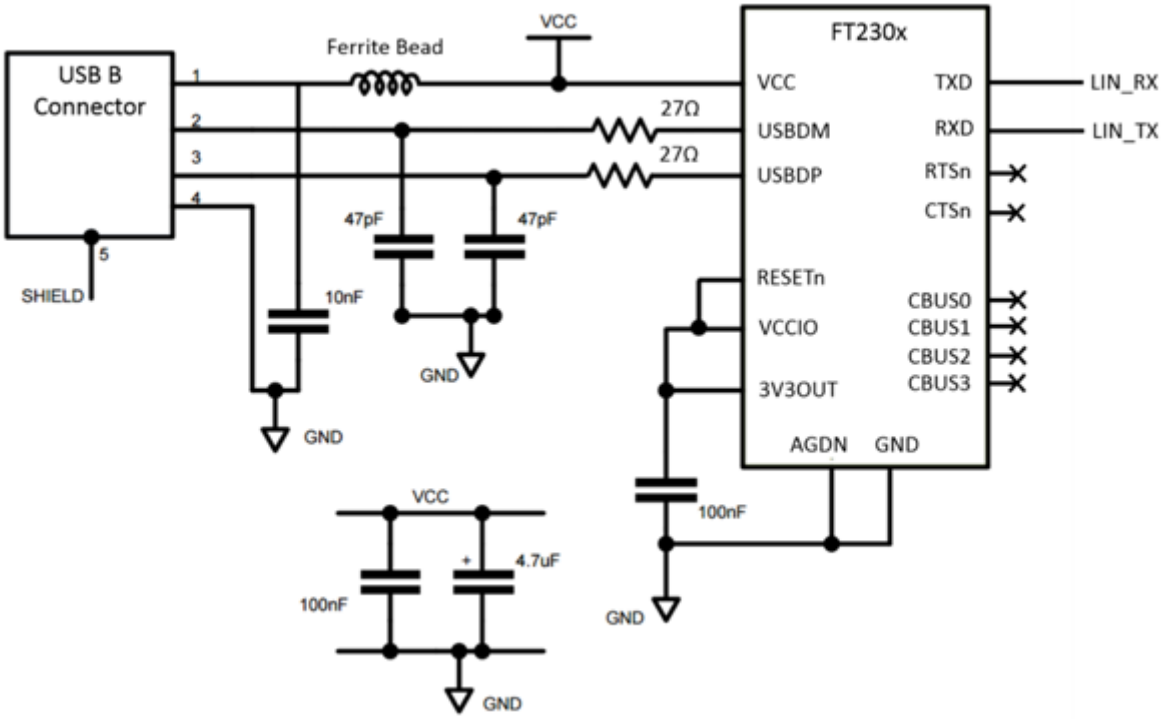


Figure 10. Bus powered USB to Serial configuration connection

9.3 CAN interface circuitry

Controller Area Network (CAN) is commonly used in almost all automotive applications to allow communication between various microchips in the car.

The number of CAN modules on-chip varies from device to device. A separate CAN transceiver is required for each CAN module, although some CAN transceivers may have more than one transceiver on a single chip. It is possible to connect two CAN modules to a single transceiver if the transmit pins are put into open-collector mode with an external pullup resistor. However, the value of this resistor may limit the maximum speed of the CAN module if not sized properly for the speed.

NXP CAN modules conform to CAN protocol specification version 2.0 B, and the transceivers shown in this application note comply with the ISO 11898 physical layer standard.

Typically, CAN is used at either a low speed (5 Kbit/s to 125 Kbit/s) or a high speed (250 Kbit/s to 1 Mbit/s). Powertrain applications typically use a high speed (HS) CAN interface to communicate between the engine control unit and the transmission control unit. Body and chassis applications typically use a low speed (LS) CAN interface. In the dashboard of a vehicle, there is typically a gateway device that interfaces between HS and LS CAN networks.

NXP has a high-speed standalone CAN physical interface device with built-in diagnostic capabilities (MC33902), as well as CAN transceivers integrated with other functions. Other popular CAN transceivers include the NXP devices shown in the following table. Example TJA1050 HS and TJA1054 LS circuits are shown in this application note.

Table 15. Commonly used CAN transceivers

	TJA1050	TJA1054	TJA1040	TJA1041
Bitrate (Kbits/s)	1000	125	1000	1000

Table continues on the next page...

Table 15. Commonly used CAN transceivers (continued)

	TJA1050	TJA1054	TJA1040	TJA1041
Modes of operation	Normal, Listen-only	Normal, Standby, Sleep	Normal, Standby	Normal, Listen-only, Standby, Sleep

9.3.1 High-speed CAN with diagnostics: MC33902 interface

For target systems that require full diagnostics of the CAN interface, NXP MC33902 high-speed CAN transceiver is available. Features of this device are:

- High-speed CAN interface for baud rates of 40 Kbit/s to 1.0 Mbit/s
- Compatible with the ISO 11898 standard
- Single supply from battery
- I/O compatible from 2.75 V to 5.5 V via a dedicated input terminal (3.3 V or 5.0 V logic compatible)
- Low-power mode with remote CAN wakeup and local wake-up recognition and reporting
- CAN bus failure diagnostics and TXD/RXD pin monitoring, cold start detection, and wake-up sources reported through the ERR pin
- Enhanced diagnostics for bus, TXD, RXD, and supply pins available through pseudo-SPI via existing terminals EN, STBY, and ERR
- Split terminal for bus recessive level stabilization
- INH output to control external voltage regulator

The figure below shows an example schematic using the MC33902.

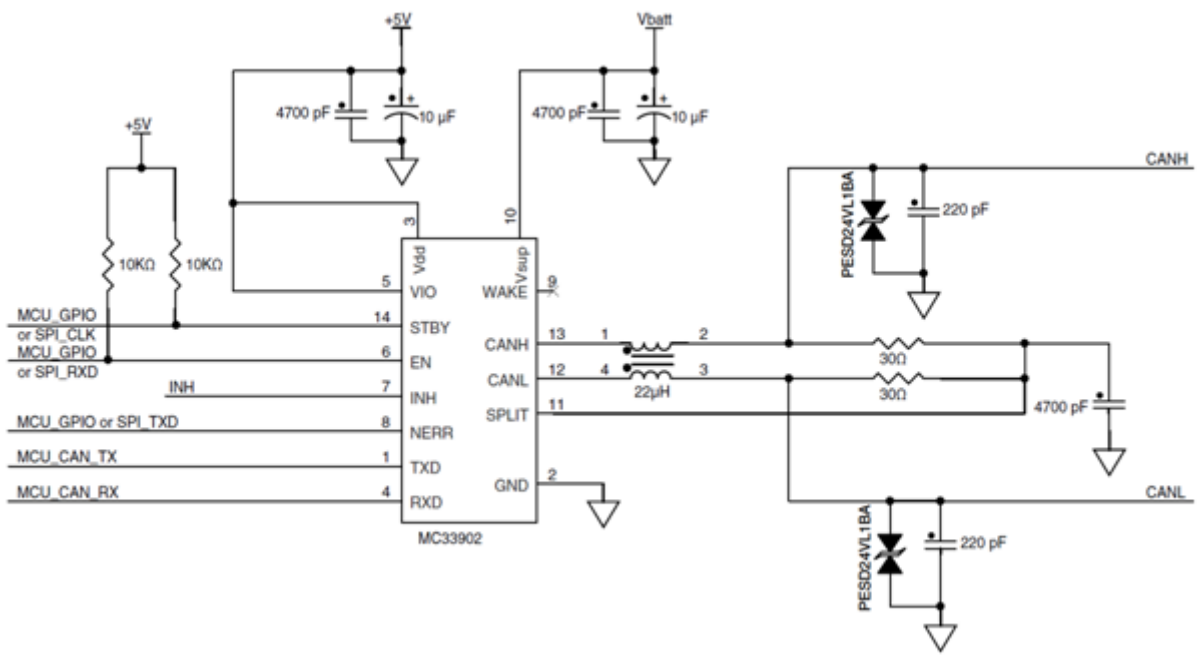


Figure 11. Typical high-speed CAN circuit using the MC33902

The use of the Inhibit pin (INH) is dependent on the selected target system operation. INH can turn an external power supply on and therefore wake up a connected MCU for operation to save power when MCU operation is not required.

9.3.2 High-speed CAN TJA1050 interface

The figure below shows the typical connections for the physical interface between the MCU and the CAN bus for high-speed applications using the NXP TJA1050 HS CAN transceiver.

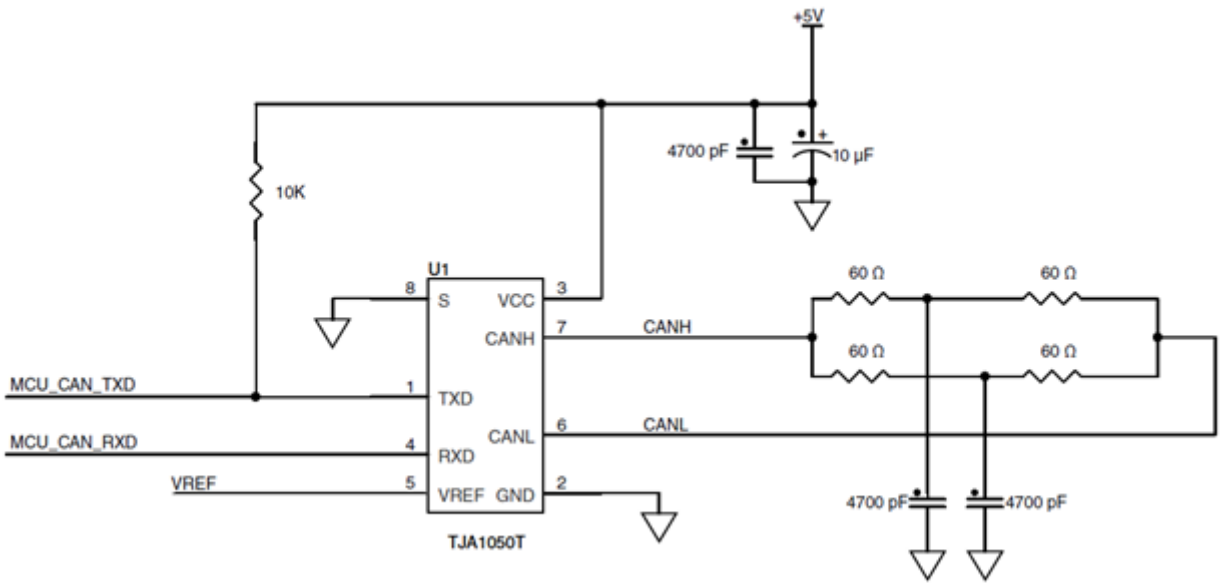


Figure 12. Typical high-speed CAN circuit using TJA1050

NOTE

- Decoupling shown as an example only.
- TXD/RXD pullup/pulldown may be required, depending on device implementation.

9.3.3 Low speed CAN TJA1054 interface

The figure below shows the typical connections for the physical interface between the MCU and the CAN bus for low-speed applications using the NXP TJA1054 LS CAN transceiver. Optionally, the standby and enable pins can be connected to MCU GPIO pins for additional control of the physical interface.

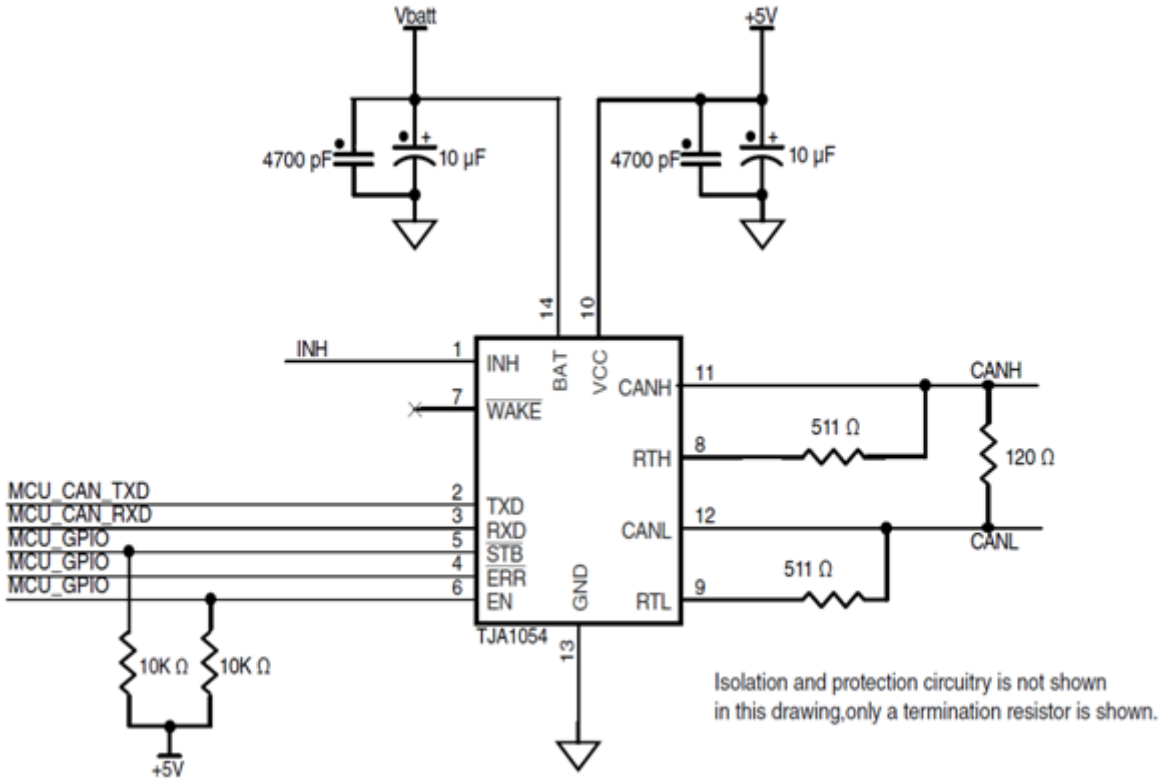


Figure 13. Typical low-speed CAN circuit using TJA1054

NOTE

- Decoupling shown as an example only.
- STB and EN should be pulled high for Normal mode. These signals can optionally be connected to MCU GPIO pins to allow MCU control of the physical interface.

9.3.4 ENET Ethernet interface

The MAC57D5xx ENET (Ethernet) module may provide either MII or RMII connections. MII requires 16 signals and requires a 25 MHz clock, while RMII only requires 8 signals, but requires a faster reference clock of 50 MHz.

There are different options to generate the reference or TX clock when using the ENET module:

- Externally, by an external oscillator providing it to both MAC57D5xx and the Ethernet PHY
- Externally, by an Ethernet PHY providing it to the MAC57D5xx
- Internally, by the MAC57D5xx generating the reference clock

Whether the ENET clock is internal or external is selectable using the General Purpose Register 1, ENET_CLK bit field. For more details please check the device Reference Manual..

Consider the following recommendations when designing the connections between the ENET and the PHY interface:

- Series termination may be required by the transceiver
- Minimize trace length
- Route the clock in isolation away from other traces and noise sources
- Must be routed over a continuous ground plane. It should not be routed across any plane splits or traces on adjacent layers

9.3.4.1 Ethernet TJA1100 Interface example

The NXP TJA1100 is an Ethernet PHY optimized for automotive use cases. The device provides 100 Mbit/s transmit and receive capability over a single Unshielded Twisted Pair (UTP) cable, supporting a cable length of up to 15 m. Optimized for automotive use cases such as IP camera links, driver assistance systems and back-bone networks, the TJA1100 has been designed to minimize power consumption and system costs, while still providing the robustness required for automotive use cases.

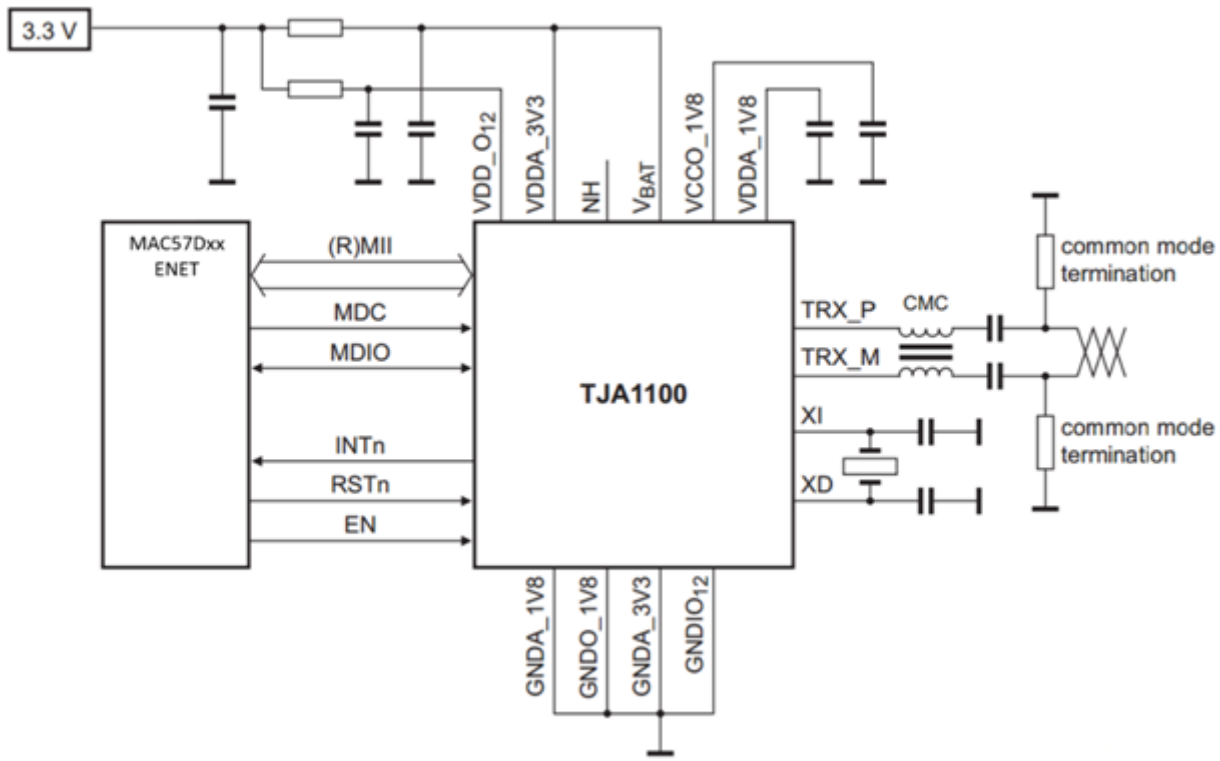


Figure 14. Typical Ethernet circuit using TJA1100

10 External Memories

10.1 SDR DRAM

SDR (Single Data Rate) DRAM is the first generation of synchronous DRAM and is slower than the DDR variants. However, SDR DRAM provides the advantages of system simplicity and cost reduction due to the reduced frequency at which it operates (Max 160MHz) and the 3.3 V supply voltage requirement, which is already required for MAC57D5xx.

All MAC57D5xx packages support SDR DRAM. Only 16 bit SDR DRAM is supported.

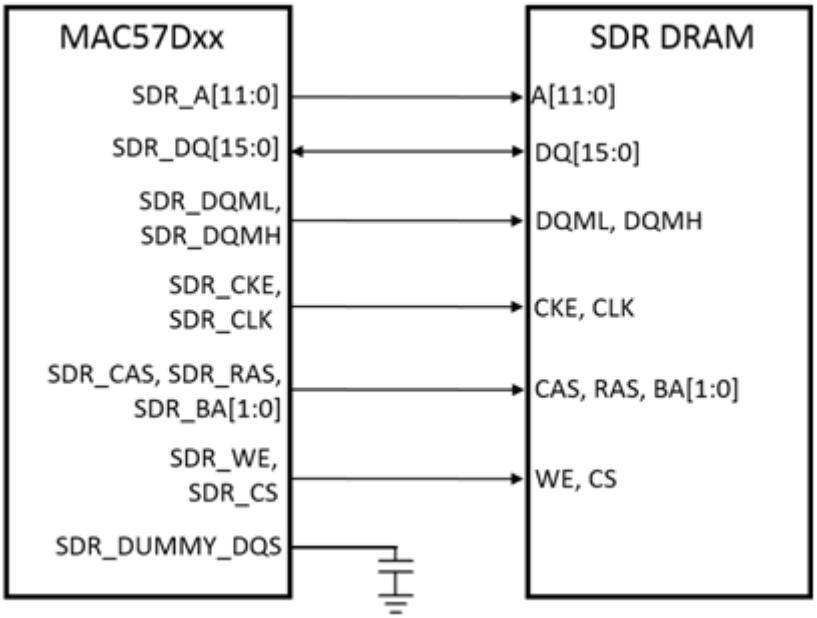


Figure 15. SDR DRAM Connection Diagram

The following considerations must be taken into account when designing with SDR DRAM and MAC57D5xx:

- If the operating frequency is > 80 MHz, use the SDR_DUMMY_DQS to compensate for the round trip delay in the path of the SDR read data. The capacitor selected should reflect the load on the SDR_CLK pin (board load + SDR pin load).
- If Operating at < 80 MHz, SDR_DUMMY_DQS is not necessary and this pin can be used as SDR_A[12]
- It is required to match the impedance of the lines at 50 Ohms
- Series termination of 50 Ohms at the Halo pins is recommended on all SDR lines
- Trace length for Data with respect to CLK signals must be matched within 45 ps
- Trace length for Address/Cmd with respect to CLK signals must be matched within 190 ps
- Round trip trace delay for CLK “out” and Data “in” should not be more than 450 ps

10.2 DDR2 DRAM

DDR2 SDRAM is a double data rate synchronous dynamic random-access memory interface which is only available on the 516 MAPBGA package of MAC57D5xx. The main advantage of using DDR2 over SDR is performance. The double data rate allows the transfer of twice the amount data on a single clock cycle and it is possible to have up to 32 bit data bus and twice the maximum frequency. This gives approximately 8x the maximum performance achievable on the SDR interface.

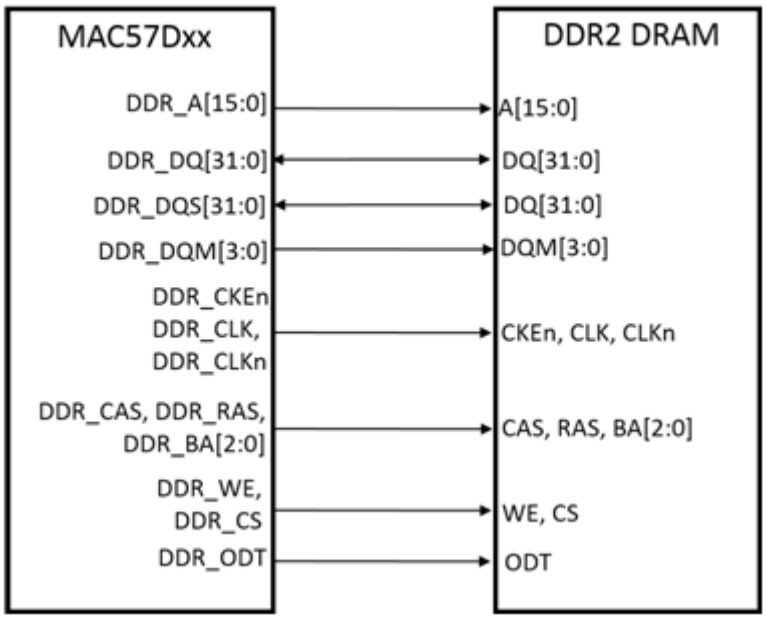


Figure 16. DDR2 DRAM Connection Diagram

The following considerations must be taken into account when designing with DDR2 DRAM and MAC57D5xx:

- CLK/Addess/Commands
  - Route with 50 Ohms controlled impedance and differential pair (CLK) with 100 Ohms controlled impedance.
  - In case of multiple memory components use “Y” topology. Most of the length should be contained in the trunk of the Y, and the length to each device after the split should be as short as possible.
  - Address/Cmd must be terminated to VTT with 50 Ohms.
  - Address/Cmd must be routed within 10ps with respect to CLK and must be matched from controller to memory; memory to memory as well.
  - All traces to be routed in internal layers.
  - Preference is to use only two layers for routing this group.
  - Limit the number of vias to less than three

- Data/Strobe
  - Route with 50 Ohms controlled impedance.
  - Data to be routed within 5 ps with respect to the respective data strobe.
  - All traces must be routed in internal layers.
  - Strictly must be routed in only two layers.
  - Avoid more than two vias.

10.3 Quad Serial Peripheral Interface (QSPI)

The QuadSPI block supports the connection to QuadSPI NOR Flash memories. These memories allow up to four data lines and can be accessed as single data rate (SDR) or double data rate (DDR) devices. Each QuadSPI interface in MAC57D5xx supports up to two external QuadSPI NOR flash memories that can be used in parallel.

The MAC57D5xx QuadSPI interface also supports Octal SPI memories. For more information about supported devices, please check the device Reference Manual.

Figure 17. QuadSPI Connection Diagram

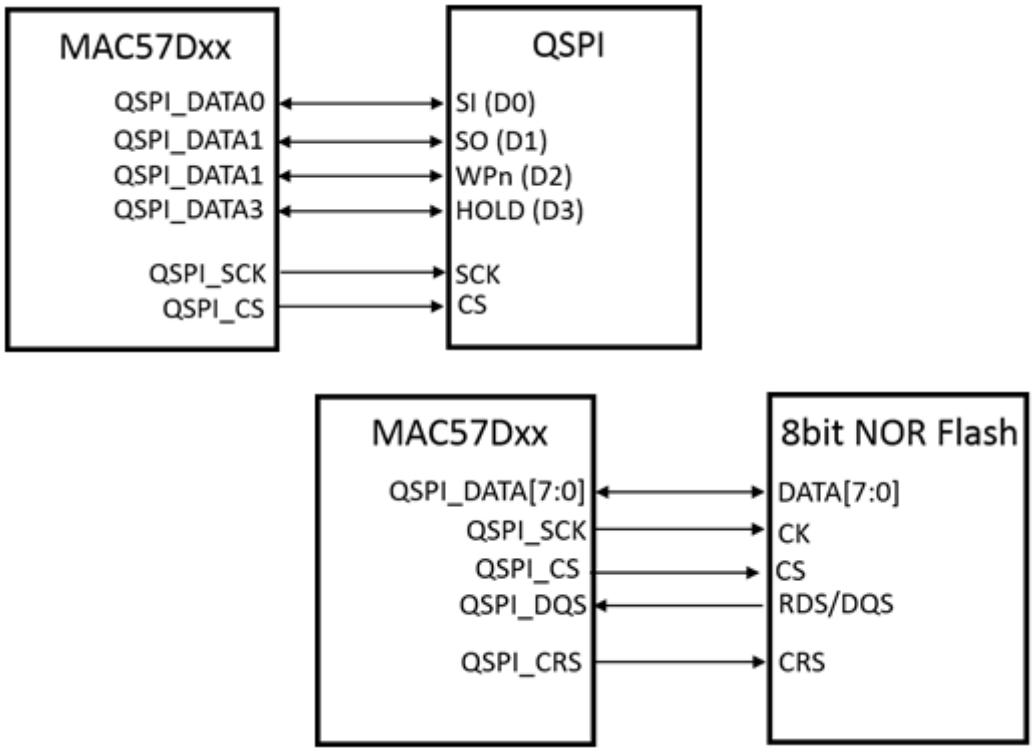


Figure 18. Octal SPI Connection Diagram

Please note that for the Octal SPI, some memory types may not require the Central Read Strobe (CRS) signal, also known as CK2.

The following considerations must be taken into account when designing with QuadSPI and MAC57D5xx:

- Clock signal must be at least 3x away from other signal traces to avoid noise coupling
- Avoid the use of vias since they will create impedance changes and signal reflections
- Avoid using serpentine routing, use straight traces
- Keep a ground plane on the adjacent layer
- Route with 50 Ohms controlled impedance
- Traces should be routed with similar lengths within 3 mm with respect to the clock and the data lines
- If Operating at > 35 MHz in DDR mode, consider the following requirements:
  - Internal or External DQS mode is required
  - Data Learning (software operation) is required at frequencies > 45 MHz when internal DQS is used because temperature and voltage changes move the data valid window
  - External DQS gives the maximum performance and does not requires Data Learning

11 Instrument Cluster Modules

11.1 Sound Generation Module (SGM)

The Sound Generation Module in MAC57D5xx is a 4-channel sound generator which supports the generation of autonomous audio notes, mono linear PCM data playback, and mixing and amplitude control. Output data from the SGM mixer is stereo 16-bit PCM samples that can be fed to the I^2S interface of an external audio DAC or to an internal PWM for output to an external low pass filter.

There are two options available when using the SGM:

- PWM output
- I^2S

The PWM output consists of a single pin which outputs a PWM signal with a duty cycle that varies at the sample rate of the audio data. The I²S option is a 4 pin interface used to send stereo 16-bit sample data to an external sound Digital to Analog converter (DAC). The second option can achieve CD quality sound, while the first can achieve quality levels that are similar to AM radio.

The hardware connections are different for the two solutions. The PWM solution normally looks like the figure below where the PWM output is filtered and has the DC offset removed before amplifying.

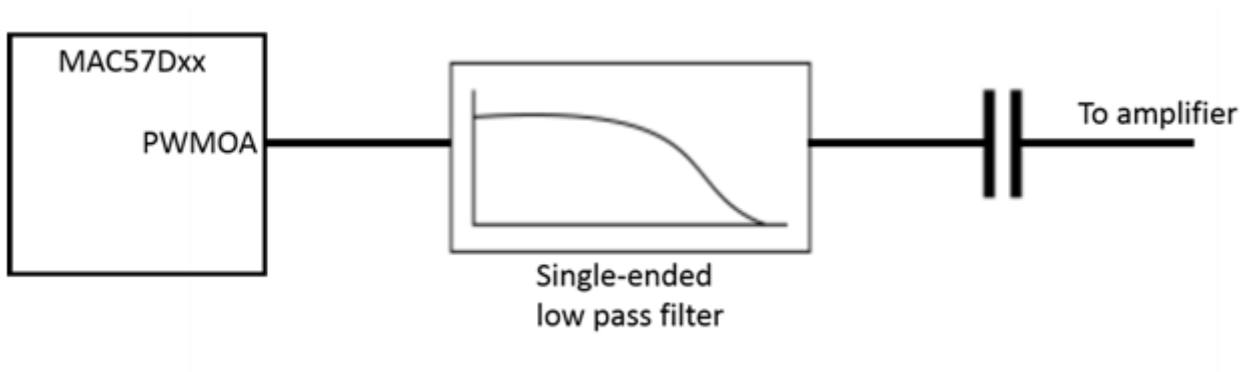


Figure 19. SGM PWM Filtering System

To define the filter, it is necessary to calculate the PWM frequency and sample rates. An example of the filter characteristics consider the following calculation:

$$f_{PWM} = 2^{sample\_depth} * f_{sample\ rate}$$

Equation 1

- fPWM is the (carrier) frequency of the audio signal
- sample_depth is the number of bits in each audio sample
- fsample rate is the audio sample rate

In an ideal case we would produce CD quality output using this approach, but it is not possible because the PWM operating clock will be too large as shown in the equation below:

$$f_{PWM} = 2^{16} * 44100 = 2{,}890{,}137{,}600\ Hz$$

Equation 2

Therefore, a practical output has to sacrifice sample depth or sample rate or both. In practice, the sounds required by typical applications in the vehicle cockpit space are not high bandwidth and therefore it tends to be more satisfactory to reduce the sample rate and keep the sample depth at 10-bit or above. A suggested compromise would be a sample depth of 10 and a sample rate of 11025 kHz, which respects the 44.1 kHz reference point. This requires a PWM frequency as given in the equation below:

$$f_{PWM} = 2^{10} * 11025 = 11{,}289{,}600\ Hz$$

Equation 3

The SGM can operate up to 160 MHz. This is approximately 14 times the calculated clock and so it is possible to achieve by operating the PWM at a higher rate than calculated but keeping the sample rate the same. This will result in more than one sample per PWM duty period.

With this calculation, we can design a filter to remove the unwanted PWM carrier wave. The sample rate is 11 kHz and therefore the maximum frequency usable without aliasing is 5.5 kHz. Depending on the audio content, it may be better to have a filter cut off at a lower frequency and have a less sharp roll-off than a cut off at 5.5 kHz which may require multiple orders of filtering to achieve satisfactory sound quality. In practice, the final sound amplifier will likely have additional filtering so the filter should be designed with this in mind as well.

The I^2S option uses the industry standard 4-pin output-only interface to send digital audio data to a hardware decoder/DAC. These often come with an integrated headphone and line-level amplifier. NXP has such a device (SGTL5000) and the figure below illustrates how this is connected to MAC57D5xx. The MCLK is an over-clocked sample rate clock of 256x or 512x the sample rate and therefore will typically operate at 11.3 MHz. Care must be taken when choosing the port drive strength and layout for this signal. The DO pin is a serial bus which transmits samples at 32 x 44100 = 1.5 MHz.Note that the SGTL5000 also requires an I^2C bus for configuration as shown in the figure.

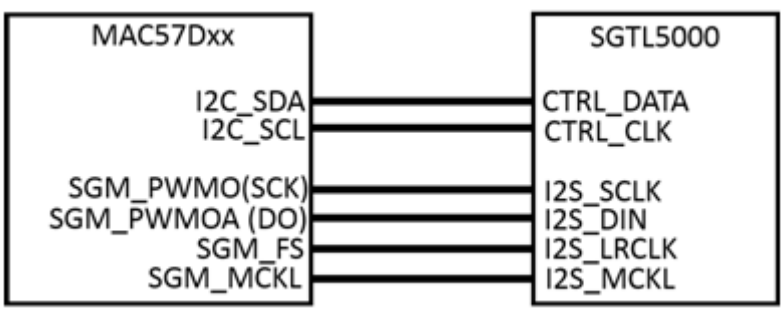


Figure 20. Simplified connection diagram between MAC57D5xx and SGTL5000

11.2 Stepper Motor Controller (SMC) and stall detection

The stepper motor controller shares its functions with the stepper stall detect module on all pins, so no special wiring is required to switch between them. Once again the modules are intended to directly connect the MAC57D5xx to suitable low current stepper motors used to drive small gauges.

The SMC provides 6 x 4 pin interfaces to connect to the coils used on the stepper motor. All of the interfaces are identical and rely on PWMs of an appropriate polarity to drive each of the coils. By appropriately accelerating and decelerating the motor through the use of the PWMs it is possible to minimize system integrity issues. The exact drive approach will vary from motor to motor depending on the coil and gear specifications and the load created by the needle.

The stepper motor functions will typically be supplied at 5 V and since power is being switched across coils there is the potential of spikes being induced back onto this power supply. Therefore it is prudent to take care when routing these signals and when connecting the power supply to avoid undesirable effects on sensitive signals.

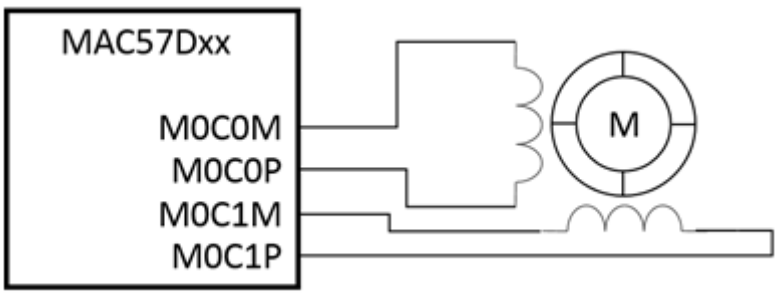


Figure 21. Stepper Motor connection with MAC57D5xx

12 Display modules

The output display module from MAC57D5xx have various electrical interfaces that provide options to connect to an external display:

- TTL mode
- Reduced Swing Differential Signaling (RSDS) mode
- Low Voltage Differential Signaling (LVDS) mode

MAC57D5xx can drive up to 2 displays, one of which can be used in LVDS or RSDS mode. To review the different routing options, please check the Timing Controller chapter from the device Reference Manual.

For video input, the only available electrical interface is TTL signaling.

12.1 Digital RGB Connection

This is the simplest method for connecting to an external display. Usually, the Timing Controller (TCON) module is used to drive the signals to an external display, but when the default pinout fits the system requirements, the TCON module can be bypassed. Therefore, two options are available when connecting to a digital RGB display:

- TCON Bypass mode: The TCON module is bypassed (not used) and the Display Controller (2D-ACE) drives the digital signals
- TCON Enabled: The Display Controller (2D-ACE) will use the TCON to drive the digital signals. This provides more flexibility in pin multiplexing, timing signals and color signal ordering. Typically used when the external display has additional especiall requirements on how the signals need to be delivered or the layout can be simplified by multiplexing the signals on different pins.

The below figure shows a simplified diagram connection between MAC57D5xx and a digital RGB display.

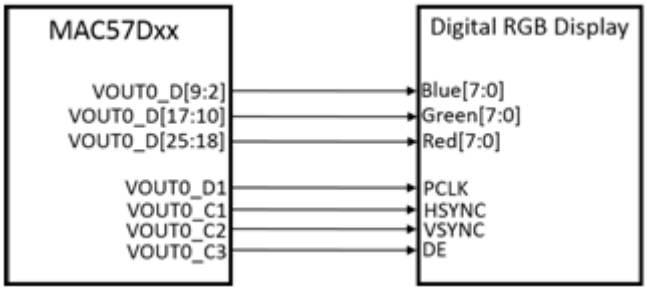


Figure 22. Parallel RGB connection diagram

Using the TCON adds flexibility to the connections on the figure above. For example, is possible to select a different pin (VOUT0_Dn) for the clock signal and also generate additional timing control signals (VOUT0_Cn) using the Timing Signal Generator (TSG) in the TCON timing signal generation unit. It accepts the HSYNC/VSYNC signals from the input parallel display interface, and maintains two counters (hcount, vcount) based on that. All of the timing signals are generated based on these two counters.

Layout requirements depend mainly on pixel clock and display timing requirements, but consider the following recommendations when designing the connection between MAC57D5xx and a digital RGB display:

- Use a trace impedance of 50 Ohms.
- Max skew between data signals <100 ps but the requirement may be relaxed for lower resolutions.
- It is common to have EMC problems with parallel RGB interface due to the flat flex cables, so they should be kept as short as possible.
- Series resistors on the bus lines are recommended to reduce slew rate and control EMC emissions.

12.2 RSDS display connection

The TCON controller allows using RSDS signaling, similar to LVDS, but with reduced power because it is an intra-panel interface, while LVDS is typically an inter module interface (external). Some of the benefits of using RSDS interface are:

- Reduced bus width
- Lower Dynamic power dissipation
- Low EMI generation
- High Noise rejection
- High throughput

The RSDS interface standard only specifies the electrical and protocol characteristics of the protocol. The control signals required by the column and gate drivers are not covered by the specification and depend exclusively on requirements from the display manufacturer.

The figure below implements a display panel without an integrated time controller. The column/row drivers are implemented with external components with the potential of reducing the cost of the system.

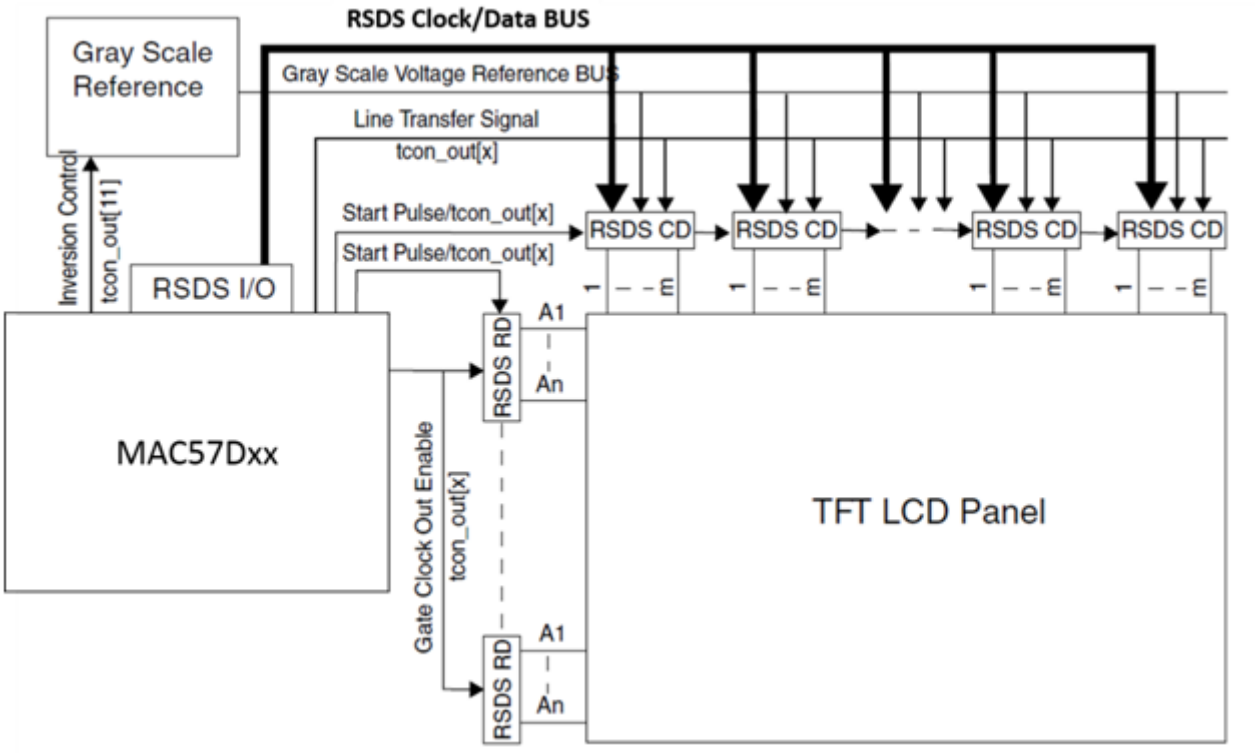


Figure 23. RSDS connection with external row and column drivers

A different use case is shown in the figure below. In this case, the panel includes its own timing controller, therefore a similar connection to RGB parallel is implemented. The only difference is that the DATA and Clock bus is differential (RSDS).

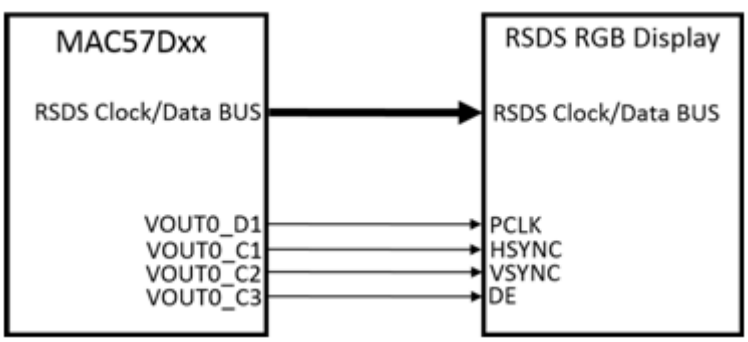


Figure 24. RSDS Connection with a Display Panel with integrated time controller

Since the MAC57D5xx RSDS interface includes a bus of differential signals and a bus of single ended signals, each bus has different routing requirements.

The following requirements are recommended for the RSDS bus:

- Follow standard high-speed differential routing rules for signal integrity
- Minimize the number of vias
- Each differential pair should be length matched to ± 5 mils
- Skew between clock and data pairs should not be more than 20 mils
- Differential pairs should have a differential impedance of 100 Ω

For the timing control signals on the single ended bus, use similar recommendations for the digital RGB sections. Consider that the signals base frequency is typically several times lower than the pixel clock, so the requirements can be relaxed based on the spec of the display used.

12.3 LVDS display bridge connection

LVDS is a signaling method used for high speed, low power transmission of binary data over copper. The LVDS current-mode drivers create a differential voltage of ~350 mV across a 100 Ohm load. The LVDS Display Bridge (LDB) in MAC57D5xx is an effective method for connecting high resolution displays using inexpensive twisted pair copper cables.

There are a total of five differential signals coming out from the LDB module: 4 data signals and 1 clock signal.

The figures below shows a simplified diagram of the connection between the LDB interface on MAC57D5xx and an external LVDS Display.

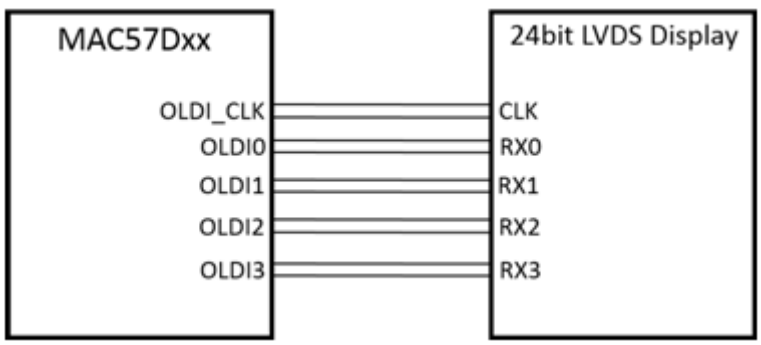


Figure 25. LVDS Connection with 24bit color display

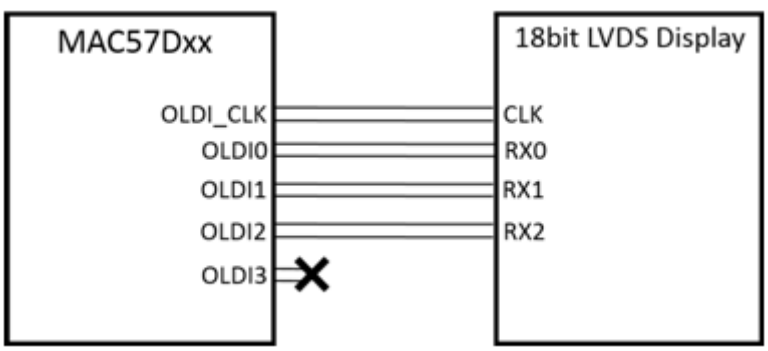


Figure 26. LVDS Connection with 18bit color display

For layout and routing of LVDS signals use the same recommendations as for the RSDS bus signals in RSDS display connection.

12.4 Parallel Video input interface (VIU)

The Video-Input unit in MAC57D5xx receives different format and resolutions of parallel video and stores it in the system memory, converting image data between YUV and RGB color spaces, scaling image size, adjusting the brightness/contrast, and writing image data to memory with many kinds of image data formats.

The following input formats are supported:

- 8-10 bit ITU656 video input
- RGB888/RGB666/RGB565 parallel input
- RGB888 serial input

- 24 bit YUV parallel input
- 8-bit mono video input

The resolution and frame rate ultimately depends on the pixel clock frequency. The maximum pixel clock for MAC57D5xx VIU input is 53 MHz.

The below figure is an example of how to connect a composite video decoder ADV7180 from Analog Devices to the NXP MAC57D5xx.

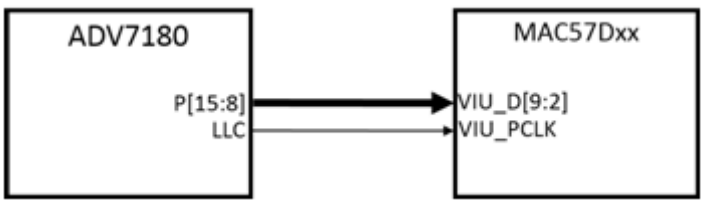


Figure 27. Composite Video Decoder connection with MAC57D5xx VIU port

Since there are several input formats supported, to understand how the pins are mapped to the different formats, please check the device Reference Manual VIU chapter, Video Input Signal Mapping table.

The layout and routing recommendations are the same as shown in Digital RGB Connection section in this document.

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