i.MX 7 Dual/Solo Product Lifetime Usage

1. Introduction

This document describes the estimated product lifetimes for the i.MX 7 Dual/Solo Application Processors based on the criteria used in the qualification process.

The product lifetimes described here are estimates and do not represent guaranteed lifetime for a particular product.

The i.MX 7 Series consists of several processors that deliver a wide range of processing and multimedia capabilities across two qualification levels.

This document is intended to provide users with guidance on how to interpret the different i.MX 7 Dual/Solo qualification levels in terms of target operating frequency of the device, the maximum supported junction temperature ($T_j$) of the processor, and how this relates to the lifetime of the device.
2. Device Qualification Level and Available PoH

Each qualification level supported (Commercial and Industrial) defines a number of power on hours (PoH) available to the processor under a given set of conditions such as:

1. The target voltage for the application (Consumer and Industrial).
   a) The lifetime is limited by the SOC operating voltage.

2. The percentage of active use vs. standby.
   a) Active use means that the processor is running at an active performance mode.
      - For the consumer tier, there are three available performance modes: 800MHz, 1GHz and 1.2GHz. For the Industrial tier, only the 800Mhz and 1Ghz are available.
   b) In standby mode, the VDD_ARM and the VDD_SOC are lowered, reducing power consumption and junction temperature. In this mode, the voltage and temperature are set low enough so that the effect on the lifetime calculation is negligible and treated as if the device were powered off.

3. The junction temperature of the processor (Tj).
   a) The maximum junction temperature of the device is different for a given qualification level, for instance 105 °C for Industrial and 95 °C for the Consumer Tier.
   b) Users must ensure that their device is appropriately thermally managed such that the maximum junction temperature is not exceeded.

All data provided within this document are estimates for PoH that are based on extensive qualification experience and testing with the i.MX 7 Series. These statistically derived estimates should not be viewed as a limit on an individual device’s lifetime, nor should they be construed as a guarantee by NXP as to the actual lifetime of the device.

2.1. Commercial lifetime estimates

Table 1 provides the number of PoH for the typical use condition for a commercial device.

<table>
<thead>
<tr>
<th>ARM® Core Speed (MHz)</th>
<th>Power-on Hours [PoH] (Hrs)</th>
<th>SOC Operating Voltage (V)</th>
<th>ARM® Core Operating Voltage (V)</th>
<th>Junction Temperature [Tj] (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>800</td>
<td>21900</td>
<td>1.0</td>
<td>1.0</td>
<td>95</td>
</tr>
<tr>
<td>1000</td>
<td>21900</td>
<td>1.0</td>
<td>1.1</td>
<td>95</td>
</tr>
<tr>
<td>1200</td>
<td>21900</td>
<td>1.0</td>
<td>1.225</td>
<td>85</td>
</tr>
</tbody>
</table>

Figure 1 establishes guidelines for estimating PoH as a function of the junction temperature. PoH can be read directly from the chart below to determine the necessary trade-offs to be made to CPU.
2.2. Industrial lifetime estimates

Table 2 provides the number of PoH the typical use conditions for an industrial device.

<table>
<thead>
<tr>
<th>ARM® Core Speed (MHz)</th>
<th>Power-on Hours [PoH] (Hrs)</th>
<th>SOC Operating Voltage (V)</th>
<th>Junction Temperature [Tj] (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>800</td>
<td>110000</td>
<td>1.0</td>
<td>105</td>
</tr>
<tr>
<td>1000</td>
<td>110000</td>
<td>1.0</td>
<td>105</td>
</tr>
</tbody>
</table>

Figure 2 establishes guidelines for estimating PoH as a function of junction temperature. PoH can be read directly off of the chart below to determine the necessary trade-off to be made for junction temperature to increase the estimated PoH of the device.
3. Combining Use Cases

In some applications, a constant operating use case cannot deliver the target PoH. In this case, it is advantageous to use multiple operating conditions. This method provides some of the lifetime benefits of running at a lower temperature use case, while keeping the ability of the system to use the highest performance state dictated by the application demands. See Figure 3.
Figure 3. Multiple temperature use case
## 4. Revision History

### Table 3. Revision history

<table>
<thead>
<tr>
<th>Revision number</th>
<th>Date</th>
<th>Substantive changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>09/2016</td>
<td>Initial release</td>
</tr>
<tr>
<td>1</td>
<td>05/2017</td>
<td>Added 1.2 GHz Use Case</td>
</tr>
</tbody>
</table>
Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer’s technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address:

nxp.com/SalesTermsandConditions.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, and Tower, are trademarks of NXP B.V. All other product or service names are the property of their respective owners.

ARM, the ARM Powered logo, and Cortex are registered trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. All rights reserved.

© 2017 NXP B.V.