

i.MX6ULL Power Consumption Application Note

1. Introduction

This application note helps to design power management systems. Through several use cases this application note illustrates the current drain measurements of the i.MX 6ULL Applications Processors taken on the MX6ULL EVK Evaluate Kit Platform. You will be enabled to choose the appropriate power supply domains for the i.MX 6ULL chips and become familiar with the expected chip power in various scenarios.

As the data presented in this application note is based on empirical measurements taken on a small sample size, the presented results are not guaranteed.

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2. Overview of i.MX 6ULL voltage supplies

The i.MX 6ULL processors have several power supply domains (voltage supply rails) and several internal power domains. Figure 1 shows the connectivity of these supply rails and the distribution of the internal power domains.

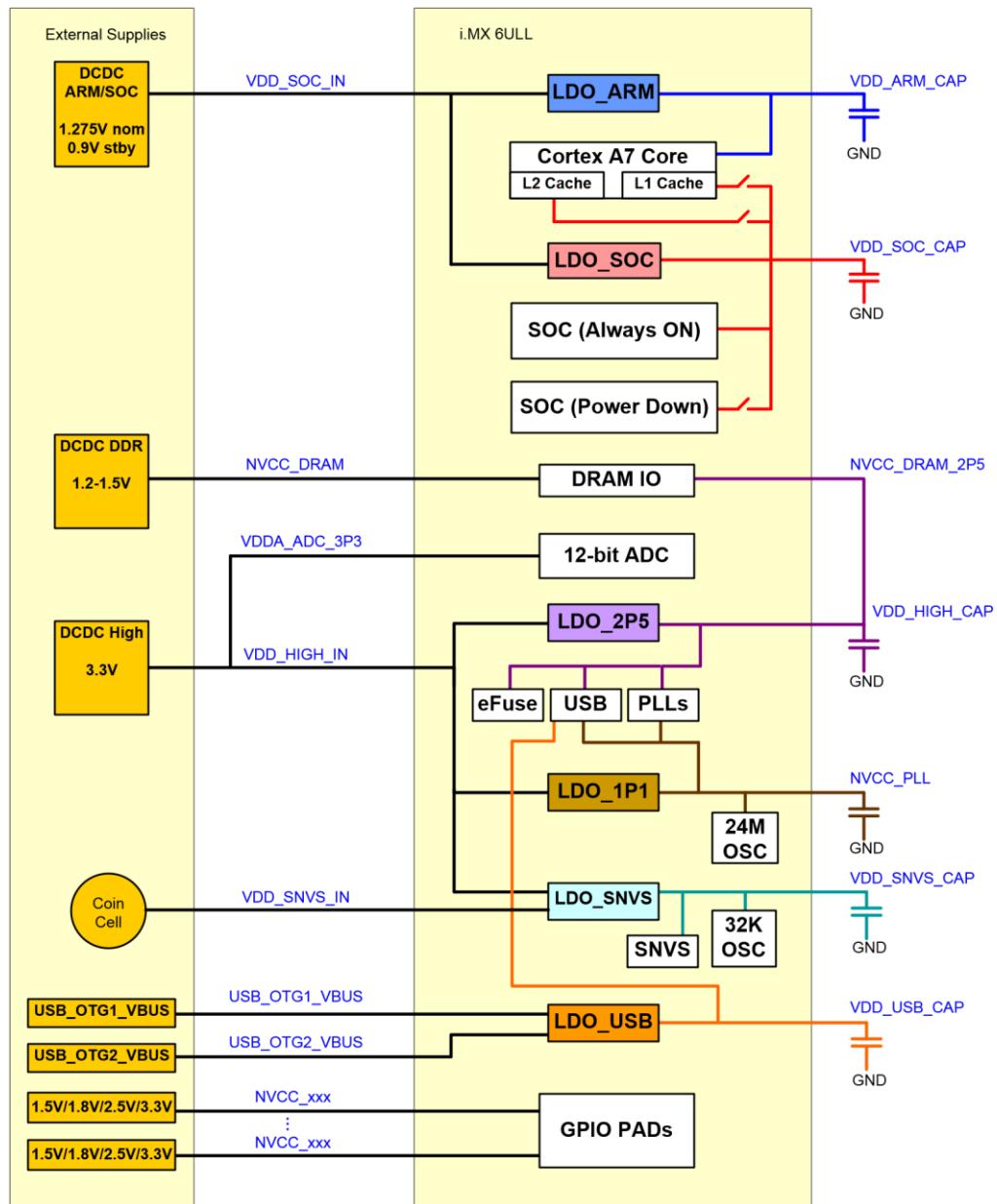


Figure 1. i.MX 6ULL power rails

NOTE

See the i.MX 6ULL datasheet for the recommended operating conditions of each supply rail and for a detailed description of the groups of pins that are powered by each I/O voltage supply.

For more details regarding the i.MX 6ULL power rails see the Power Management Unit (PMU) chapter in the *i.MX 6ULL Applications Processor Reference Manual* (document [IMX6ULLRM](#)).

3. Internal power measurement of the i.MX 6ULL processor

Several use cases (described in [Section 6, Use Case Configuration and Usage Guidelines](#)) are run on the Evaluate Kit platform (Revision C2). The measurements are taken mainly for the following power supply domains:

- VDD_SOC_IN platform's supply
- VDD_HIGH_IN: Source for PLLs, DDR pre-drives, PHYs, and some other circuitry.

These supply domains consume the majority of the internal power of the processor. For the relevant use cases, the power of additional supply domains is added. However, the power of these supply domains does not depend on specific use cases, but whether or not these modules are used. The power consumption of SNVS is comparatively negligible except in Deep-Sleep mode.

The NVCC_* power consumption depends primarily on the board level configuration and the components. Therefore, it is not included in the i.MX6ULL internal power analysis.

The power consumption for these supplies, in different use cases, is provided in Chapter 4.

NOTE

Unless stated otherwise, all measurements were taken on typical process silicon, at room temperature (26 °C approximately).

3.1. VDD_HIGH_CAP power

The voltage VDD_HIGH_CAP domain is generated from the 2.5 V LDO (LDO_2P5). This domain powers the following circuits:

- Bandgap
- eFUSE
- Analog part of the PLLs
- Pre-drivers of the DDR I/Os (NVCC_DRAM_2P5)

3.2. DDR I/O power

The DDR I/O is supplied from the NVCC_DRAM which provides the power for the DDR I/O pads. The target voltage for this supply depends on the DDR interface being used. The target voltages for the different DDR interfaces are as follows:

- 1.5 V for DDR3
- 1.35 V for DDR3L
- 1.2 V for LPDDR2

The power consumption for the NVCC_DRAM supply is affected by various factors, including the following:

- Amount of activity of the DDR interface
- On-die termination (ODT): Enabled/disabled, termination value, which is used for the DDR controller and DDR memories
- Board termination for DDR control and address bus
- Configuration of the DDR pads (such as drive strength)
- Load of the DDR memory devices

NOTE

Due to the factors outlined in the previous paragraph the measurements provided in the following tables will vary from one system to another. The data provided is for guidance only and should not be treated as a specification.

The measured current on the MX6ULL EVK Platform also includes the current of the onboard DDR3L memory devices. This board (on which the measurements were taken) includes one DDR3L device, with a total capacity of 512 MB. The EVK Platform does not require board-level resistor terminations. This further reduces the DDR I/O power usage.

3.2.1. On-die termination (ODT) settings

On-die termination (ODT) is a feature of the DDR3/DDR3L SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, DQS#, and DM signal. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

Using weaker ODT settings can greatly reduce the power consumption of the DDR I/O. The required ODT settings are system dependent and may vary among different board designs. These settings should be carefully selected for power optimization while ensuring that JEDEC requirements for the DDR parameters are still met. The default settings that are used in the Linux OS BSP release may need to be modified by the system designer to fit different systems.

3.3. Voltage levels and DVFS usage in measurement process

The voltage levels of all the supplies, except for VDD_SOC_IN, are set to the typical voltage levels as defined in i.MX 6ULL datasheet.

The VDD_SOC_IN supplies require special explanation. To save power, VDD_SOC_IN voltage is changed using DVFS (dynamic voltage and frequency scaling), during the run time of the use cases. The voltage levels of these supplies can be changed to standby voltage levels in low-power modes.

3.3.1. VDDARM voltage levels

The target voltage levels for VDDARM can vary according to the DVFS setpoint used, which is selected by the DVFS (also named CPUFREQ) driver. There are several factors that contribute to the setpoint decisions, CPU load being the most important. Other factors are CPU latency requirements, thermal restrictions, and peripheral I/O performance requirements.

NOTE

See the operating ranges table in the i.MX 6ULL datasheet for the official operating points.

Most of the measurements are performed using these voltage levels, and the power data that appears in this document is according to these values. If the measurement is done at different voltage levels, the power consumption scales with the voltage change. In real applications when DVFS is applied, the software, in conjunction with the hardware, automatically adjusts the voltage and frequency values based on the use case requirements.

The voltage used for the power calculation is the average voltage between those setpoints. It depends on the amount of time spent at each setpoint.

3.4. Temperature measurements

In some of the use cases the die temperature is measured. The temperature measurements were taken using the on-chip thermal sensor on a thermally calibrated part. While measuring temperature it is recommended to wait until the temperature stabilizes.

NOTE

The measured temperatures are for reference only and will vary on different systems due to differences in board, enclosure, and heat spreading techniques. When using the same board type the measured temperature may vary due to factors such as environment, silicon variations, and measurement error.

3.5. Hardware and tool used

The hardware and tool used for the measurements are as follows:

- The board used for the measurements is the MX6ULL EVK Platform.
- The measurements were performed using an Agilent 34460A 6½ Digit Multimeter.

3.6. Board setup used for power measurements

The power measurements are taken using the default voltages of the supplies. The default input voltages are as follows:

- VDD_SOC_IN at 1.30 V for a maximum of 528 MHz ARM® frequency
- VDD_SOC_IN at 1.40 V for a maximum of 800 MHz ARM® frequency
- VDD_SOC_IN at 1.40 V for a maximum of 900 MHz ARM® frequency
- VDD_HIGH_IN at 3.3 V
- NVCC_DRAM at 1.35 V

By using a different setup such as a configurable and separated DC switcher for ARM, the system power can be further optimized by reducing the VDD_SOC_IN input voltage level to achieve the desired operation point. Such a setup would likely result in a higher system cost, so there is a trade-off between cost and system power.

3.7. Measuring points on the MX6ULL EVK platform

The power data is obtained by measuring the average voltage drop over the measurement points and dividing it by the resistor value to determine the average current. The tolerance of the $0.02\ \Omega$ resistors on the EVK board is 1%. The measuring points for the various supply domains are as follows:

- VDD_SOC_IN: The chip domain current is measured on R729 and the recommended resistance value for this measurement is $0.02\ \Omega$.
- VDD_HIGH_IN: The VDDHIGH domain current is measured on R732 and the recommended resistance value for this measurement is $0.02\ \Omega$.
- VDD_SNVS_IN: The current domain is measured on R519 and the recommended resistance value for this measurement is $100k$
- DDR3L I/O plus Memories: The current in this domain includes the NVCC_DRAM current and the overall current of the onboard DDR3L memory devices. The current in this domain is measured on R728 and the recommended resistance value for this measurement is $0.02\ \Omega$.

4. Use cases and measurement results

The main use cases and subtypes, which form the benchmarks for the i.MX 6ULL internal power measurements on the EVK Platform, can be found in the following sections:

4.1. Low-power mode use cases

4.1.1. Use case 1: Deep-Sleep mode (DSM)

This mode is called either “Dormant mode” or “Suspend-To-RAM” in the Linux BSP. This is the lowest possible power state where external supplies are still on.

The use case is as follows:

- ARM platform is power gated
- L1 Cache periphery is power gated
- SoC is in LDO bypass mode and ARM LDO is power gate automatically
- All PLLs (phase locked loop) and CCM (clock controller module) generated clocks are off
- CKIL (32 kHz) input is on
- All of the modules are disabled
- All analog PHYs are powered down
- External high frequency crystal and on chip oscillator are powered down (by asserting SBYOS bit in CCM)
- VDD_SOC_IN is reduced to 0.925 V. In this mode, no current flow is caused by external resistive loads.

Table 1 shows the measurement results when this use case is applied on the i.MX 6ULL processor.

Table 1. Deep-Sleep Mode (DSM) measurement results

Supply Domain	Voltage (V)	Yocto L4.1.15_2.0.0_6ULL_GA; Linux Kernel Version: 4.1.15-2.0.0+gb63f3f5	
		P (mW)	I (mA)
VDD_SOC_IN	0.92	0.23	0.25
VDD_HIGH_IN	3.3	0.33	0.1
Total Power (without DDR3L I/O + Memories)	—	0.56	—
DDR3L I/O + Memories	1.33	10.108	7.6
Total Power	—	10.668	—

For additional details on this use case and settings, see [Section 6, Use Case Configuration and Usage Guidelines](#).

4.1.2. Use case two: system idle mode

The use case is as follows:

- ARM is power gated if kernel is in the lowest level of idle
- ANATOP will go into low power mode if lowest level of idle is entered and all PLLs are off
- MegaMix power domain is on
- Operating system is on
- LCD is turned off
- Screen is not refreshed. This use cases simulates the situation when the device is left idle for some time and the display is turned off after the timer expires.

[Table 2](#) shows the measurement results when this use case is applied on the i.MX 6ULL processor.

Table 2. System idle mode measurement results

Supply Domain	Yocto L4.1.15_2.0.0_6ULL_GA; Linux Kernel Version: 4.1.15-2.0.0+gb63f3f5		
	Voltage (V)	P (mW)	I (mA)
VDD_SOC_IN	1.396	5.3048	3.8
VDD_HIGH_IN	3.3	4.29	1.3
Total Power (without DDR3L I/O + Memories)	—	9.7598	—
DDR3L I/O + Memories	1.34	10.8272	8.08
Total Power	—	20.587	—

For additional details on this use case and settings, see [Section 6, Use Case Configuration and Usage Guidelines](#).

4.2. Dhystone benchmark

Dhystone is a synthetic benchmark used to measure the integer computational performance of processors and compilers. The small size of the Dhystone benchmark allows it to fit into the L1 cache and minimizes accesses to the L2 cache and DDR.

4.2.1. Use case: Dhystone benchmark on ARM Cortex®-A7

In this use case, the Dhystone test is performed by the ARM Cortex-A7 core.

[Table 3](#) shows the measurement results when this use case is applied on the i.MX 6ULL processor.

Table 3. Dhrystone benchmark measurement results on Cortex-A7 (ARM @ 528 MHz)

Supply Domain	Yocto L4.1.15_2.0.0_6ULL_GA; Linux Kernel Version: 4.1.15-2.0.0+gb63f3f5		
	Voltage (V)	P (mW)	I (mA)
VDD_SOC_IN	1.288	214.452	166.5
VDD_HIGH_IN	3.3	41.25	12.5
Total Power (without DDR3L I/O + Memories)	—	255.702	—
DDR3L I/O + Memories	1.33	13.832	10.4
Total Power	—	269.534	—

Table 4. Dhrystone benchmark measurement results on Cortex-A7 (ARM @ 800 MHz)

Supply Domain	Yocto L4.1.15_2.0.0_6ULL_GA; Linux Kernel Version: 4.1.15-2.0.0+gb63f3f5		
	Voltage (V)	P (mW)	I (mA)
VDD_SOC_IN	1.383	311.175	225
VDD_HIGH_IN	3.3	49.5	15
Total Power (without DDR3L I/O + Memories)	—	360.675	—
DDR3L I/O + Memories	1.33	13.832	10.4
Total Power	—	374.507	—

Table 5. Dhrystone benchmark measurement results on Cortex-A7 (ARM @ 900 MHz)

Supply Domain	Yocto L4.1.15_2.0.0_6ULL_GA; Linux Kernel Version: 4.1.15-2.0.0+gb63f3f5		
	Voltage (V)	P (mW)	I (mA)
VDD_SOC_IN	1.384	342.54	247.5
VDD_HIGH_IN	3.3	51.15	15.5
Total Power (without DDR3L I/O + Memories)	—	393.69	—
DDR3L I/O + Memories	1.33	13.3	10
Total Power	—	406.99	—

4.3. Heavy loading use case: 480P video playback

The purpose of this use case is to provide the power consumption of a video playback use case to show the power consumption in high-loading conditions.

This use case has the following features:

- LCD display ON, 480x272, 60 Hz
- 480p video playback through ethernet
- ARM CPU is heavily loaded
- Maximum frequencies are used for ARM, BUS, and DDR clock.

Table 6. Video Playback power measurement results (ARM @ 528 MHz)

Supply Domain	Yocto L4.1.15_2.0.0_6ULL_GA; Linux Kernel Version: 4.1.15-2.0.0+gb63f3f5		
	Voltage (V)	P (mW)	I (mA)
VDD_SOC_IN	1.28	208	162.5
VDD_HIGH_IN	3.3	66	20
Total Power (without DDR3L I/O + Memories)	—	274	—
DDR3L I/O + Memories	1.33	140.98	106
Total Power	—	414.98	—

Table 7. Video Playback power measurement results (ARM @ 800 MHz)

Supply Domain	Yocto L4.1.15_2.0.0_6ULL_GA; Linux Kernel Version: 4.1.15-2.0.0+gb63f3f5		
	Voltage (V)	P (mW)	I (mA)
VDD_SOC_IN	1.383	262.77	190
VDD_HIGH_IN	3.3	75.9	23
Total Power (without DDR3L I/O + Memories)	—	338.67	—
DDR3L I/O + Memories	1.33	159.6	120
Total Power	—	498.27	—

Table 8. Video Playback power measurement results (ARM @ 900 MHz)

Supply Domain	Yocto L4.1.15_2.0.0_6ULL_GA; Linux Kernel Version: 4.1.15-2.0.0+gb63f3f5

	Voltage (V)	P (mW)	I (mA)
VDD_SOC_IN	1.385	283.925	205
VDD_HIGH_IN	3.3	75.9	23
Total Power (without DDR3L I/O + Memories)	—	359.825	—
DDR3L I/O + Memories	1.33	164.92	124
Total Power	—	524.745	—

4.4. SNVS

In this use case, most of the power rails on the boards are off except from the VDD_SNVS domain. VDD_SNVS is kept on to ensure that RTC and other logic in the SNVS domain remain powered on. Table 9 shows the SNVS measurement results.

Table 9. SNVS measurement results

Supply Domain	Voltage (V)	Under SRTC mode, power consumption does not depend on software	
		P (uW)	I (uA)
VDD_SOC_IN	0	0	0
VDD_HIGH_IN	0	0	0
SNVS_IN	3.34	85.17	25.5
Total Power (without DDR3L I/O + Memories)	—	85.17	—
DDR3L I/O + Memories	0	0	0
Total Power	—	85.17	—

NOTE

The SNVS_IN power consumption in table 6 is measured according to the following conditions:

1. POR_B pin setting: GPBIT[1:0] set to 2b'01;
2. BOOT_MODE[1:0] switch to 2b'00 after system boot up;
3. Remove U2101.

Some recommendations can be considered for SNVS_IN power reduction:

1. "Boot From Fuses" as system BOOT TYPE which can remove the external resistors on BOOT_MODE0/1 PINS;
2. TAMPER0-9 PINS leave floating or only used as TAMPER function (only for MCIMX6G3Cxxxxxx);

3. Add isolation for TAMPER0-9 PINs if those are used as GPIO to prevent the SNVS_IN leakage.

SNVS_IN power design need to consider:

BOOT_MODE0/1, TAMPER0-9, POR_B those PINs connections.

5. Reducing power consumption

The overall system power consumption depends on both software optimization and how the system hardware is implemented. Below is a list of suggestions that may help reduce system power. Some of these are already implemented in Linux BSP. Further optimizations can be done on the individual customer's system.

NOTE

Further power optimizations are planned for future BSP releases. See the NXP website to obtain the latest BSP release.

- Apply clock gating whenever clocks or modules are not used, by configuring CCGR registers in the Clock Controller Module (CCM).
- Reduce the number of operating PLLs: applicable mainly in Audio Playback mode or Idle modes.
- Core DVFS and system bus scaling: applying DVFS for ARM and scaling the frequencies of the AXI, AHB, and IPG bus clocks can significantly reduce the power consumption of the VDDARM and VDDSOC domains. However, due to the reduced operation frequency, the accesses to the DDR take longer, which increases the power consumption of the DDR I/O and memories. This trade-off needs to be taken into account for each mode, to quantify the overall effect on system power.
- Put the i.MX 6ULL into low-power modes (WAIT, STOP) whenever possible. See Chapter “Clock Controller Module (CCM)” of the i.MX 6ULL Applications Processor Reference Manual (document [IMX6ULLRM](#)) for details.
- DDR interface optimization:
 - Use careful board routing of the DDR memories, maintaining PCB trace lengths as short as possible.
 - Use as reduced an ODT (On-Die Termination) setting as possible. The termination used greatly influences the power consumption of the DDR interface pins.
 - Use the proper output driver impedance for DDR interface pins that provide good impedance matching. Select the lowest possible drive strength that provides the required performance, in order to reduce current through DDR I/O pins.
 - Choose onboard resistors so the least amount of current is wasted. For example, when selecting impedance matching resistors between CLK and CLK_B (when using DDR3L memories).
 - When possible, in lower performance use cases, switching to DLL Off mode allows for greatly reducing DDR frequency. This disables or reduces termination, and it reduces the

drive strength. Thus, power consumption of the DDR interface pins could be significantly reduced.

- Float the i.MX 6ULL DDR interface pins (set to high Z) when DDR memory is in Self-Refresh mode, and keep DDR_SDCKE0 and DDR_SDCKE1 at low value. If DDR_SDCKE0 and DDR_SDCKE1 are kept at low value by using external pull-down resistors, make sure there is no onboard termination on these pins during this mode.
- If possible (depending on system stability), configure DDR input pins to CMOS mode, instead of Differential mode. This can be done by clearing the DDR_INPUT bit in the corresponding registers in IOMUXC. This setting is mostly recommended when operating at low frequencies, such as in DLL Off mode.
- Use of LV DDR3L memory devices, operating at low I/O voltage, can further reduce the I/O power by 20%.
- Use of DDR memory offerings in the latest process technology can significantly reduce the power consumption of the DDR devices and the DDR I/O.

The various steps involved in floating the i.MX 6ULL DDR interface pins are shown below.

NOTE

All the programming steps below are performed when the code is running from the internal RAM rather than from the DDR memory. The code is non-cacheable.

5.1. Steps to be performed before entering Suspend (Deep-Sleep mode):

1. Read the power saving status in MMDC in the MAPSR register (automatic power saving is enabled) to make sure that DDR is in Self-Refresh.
2. Do the following:
 - a) If there is no onboard termination for DDR control and the address bus, set the DSE (drive strength selection, in IOMUXC) for all DDR IF I/O to 0 (High Z), except for CKE0 and CKE1.
 - b) If the DDR control and address bus have onboard termination resistors connected to VTT, such as in the case where SODIMM is used:
 - Option 1
As per 2a, keep SDCKE0/1 active, this causes some extra current from the pins sharing the same DSE control in IOMUXC_SW_PAD_CTL_GRP_CTLDS register. The pins are DRAM_CS0, DRAM_CS1, DRAM_SDBA2, DRAM_SDCKE0, DRAM_SDCKE1, and DRAM_SDWE.
 - Option 2 (requires onboard pull down resistors on DRARM_SDCKE0/1 pins)

- Set the supply of the termination resistor to be floated (this can be done through pins with GPIO capability).
 - Set the DSE (drive strength selection, in IOMUXC) for all DDR IF I/O to 0 (High Z).
3. Go into the Suspend mode.

5.2. Steps to be performed after exiting Suspend:

1. Restore all the settings for the DDR I/O to the required values.
2. The system proceeds to Run mode.

NOTE

If the system can ensure there are no masters accessing the DDR, the following may be applied to other scenarios besides Deep-Sleep mode: DDR pins can be floated in the same manner, even when Suspend is not entered, and DDR can be manually put into Self-Refresh to save power. This happens when the CPU is not running, or it is running from the internal RAM.

6. Use case configuration and usage guidelines

6.1. Deep-Sleep mode

In this use case all clocks and PLLs are turned off except the 32 kHz clock which is for system wake up.

1. Boot up Linux OS image.
2. Run below command to let system enter DSM mode:

```
echo mem > /sys/power/state
```

3. Measure the power and record result.

6.2. System Idle mode

6.2.1. System Idle mode: clock configuration

Table 10. System Idle mode clock configuration

Clock Name	Frequency (MHz)
AXI	24
AHB	3
CPU	0

MMDC CH0	1
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6.2.2. System Idle mode: PLL configuration

Table 11. System Idle mode PLL configuration

PLL Name	Frequency (MHz)
PLL1—System PLL	0
PLL2—System Bus PLL	0
pll2 396m pfd	0
pll2 352m pfd	0
pll2 594m pfd	0
pll2 200m pfd	0
PLL3—OTG USB PLL	0
pll3 508m pfd	0
pll3 454m pfd	0
pll3 720m pfd	0
pll3 540m pfd	0
PLL4—Audio PLL	0
PLL5—Video PLL	0
PLL6—ENET PLL	0
PLL7—Host USB PLL	0

6.2.3. System Idle mode: system setup

Disconnect everything except the SD.

1. Boot up Linux image with "x11=false uart_from_osc" in cmdline.
2. Run the following script to let the system enter powersave governor:

```
#!/bin/bash
echo 8 > /proc/sys/kernel/printk
```

```

ifconfig eth0 down
ifconfig eth1 down
echo powersave > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor
echo 1 > /sys/class/graphics/fb0/blank

```

3. Measure the power and record the result.

6.3. Dhystone on Cortex-A7

6.3.1. Dhystone on Cortex-A7: clock configuration

Table 12. Dhystone clock configuration

Clock Name	ARM Frequency @ 528 MHz	ARM Frequency @ 800 MHz	ARM Frequency @ 900 MHz
AXI	264 MHz	264 MHz	264 MHz
AHB	132 MHz	132 MHz	132 MHz
CPU	528 MHz	800 MHz	900 MHz
MMDC CH0	396 MHz	396 MHz	396 MHz

6.3.2. Dhystone on Cortex-A7: PLL configuration

Table 13. Dhystone PLL configuration

PLL Name	ARM Frequency @ 528 MHz	ARM Frequency @ 800 MHz	ARM Frequency @ 900 MHz
PLL1—System PLL	0	800 MHz	900 MHz
PLL2—System Bus PLL	528 MHz	528 MHz	528 MHz
pll2 396m pfd	396 MHz	396 MHz	396 MHz

pll2 352m pfd	0	0	0
pll2 594m pfd	0	0	0
pll2 200m pfd	0	0	0
PLL3—OTG USB PLL	480 MHz	480 MHz	480 MHz
pll3 508m pfd	0	0	0
pll3 454m pfd	454 MHz	454 MHz	454 MHz
pll3 720m pfd	0	0	0
pll3 540m pfd	0	0	0
PLL4—Audio PLL	0	0	0
PLL5—Video PLL	0	0	0
PLL6—ENET PLL	0	0	0
PLL7—Host USB PLL	0	0	0

6.3.3. Dhystone on Cortex-A7: system setup

- SD boot
- Connect LCD panel

6.3.4. Dhystone on Cortex-A7: steps

1. Boot up the Linux image and boot the board to the SD rootfs
2. Run the following script to measure at 528 MHz or 800MHz:

```
#!/bin/sh

ifconfig eth0 down
ifconfig eth1 down
echo 1 > /sys/class/graphics/fb0/blank;
echo userspace > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor;
echo 528000 > /sys/devices/system/cpu/cpu0/cpufreq/scaling_setspeed;
```

Run dry2 and measure:

```
while true; do dry2; done
```

3. Measure the power and record the result.

6.4. Heavy loading use case: video playback

480p video playback on Cortex-A7.

6.4.1. Video playback: clock configuration

Table 14. Maximum power clock configuration

Clock Name	ARM Frequency @ 528 MHz	ARM Frequency @ 800 MHz	ARM Frequency @ 900 MHz
AXI	264 MHz	264 MHz	264 MHz
AHB	132 MHz	132 MHz	132 MHz
CPU	528 MHz	800 MHz	900 MHz
MMDC CH0	396 MHz	396 MHz	396 MHz

6.4.2. Video playback: PLL configuration

Table 15. Maximum power PLL configuration

PLL Name	ARM Frequency @ 528 MHz	ARM Frequency @ 800 MHz	ARM Frequency @ 900 MHz
PLL1—System PLL	0	800 MHz	900 MHz
PLL2—System Bus PLL	528 MHz	528 MHz	528 MHz
pll2 396m pfd	396 MHz	396 MHz	396 MHz
pll2 352m pfd	0	0	0
pll2 594m pfd	0	0	0
pll2 200m pfd	0	0	0
PLL3—OTG USB PLL	480 MHz	480 MHz	480 MHz
pll3 508m pfd	0	0	0
pll3 454m pfd	454 MHz	454 MHz	454 MHz
pll3 720m pfd	720 MHz	720 MHz	720 MHz
pll3 540m pfd	0	0	0
PLL4—Audio PLL	0	0	0
PLL5—Video PLL	649 MHz	649 MHz	649 MHz
PLL6—ENET PLL	500 MHz	500 MHz	500 MHz
PLL7—Host USB PLL	0	0	0

6.4.3. Video playback: system setup

- SD boot
- Connect LCD panel

6.4.4. Video playback: steps

1. Boot up the Linux image and boot the board to the SD rootfs, connect to LCD display
2. Run the following script to measure at 528 MHz or 800MHz:

```
#!/bin/sh
echo userspace > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor;
echo 528000 > /sys/devices/system/cpu/cpu0/cpufreq/scaling_setspeed
echo 0 > /sys/class/graphics/fb0/blank
```

4. Mount server where video stream locates to board:

```
mkdir /mnt/nfsmount -t nfs -o noblock <Server IP>:  
<Server nfs service path> /mnt/nfs
```

5. Run video playback through the ethernet:

```
cd <video stream path>;  
  
gplay-1.0 ./H264_BP13_640x480_15_1507_AAC_44_128_2_vbr.mp4 -video  
-sink="imxv4l2sink sync=false" --audio-sink=fakesink
```

6. Measure the power and record the result.

6.5. SNVS

6.5.1. SNVS: steps

1. Boot up the Linux image and boot the board to the SD rootfs
2. Press the power (on/off) key for about 5 seconds so that the board powers down
3. Measure the power and record the result

6.6. Important commands

In U-Boot Console

- **printenv:** display environment variables
- **setenv:** update environment variables
 - **setenv <name> <value> ...**
 - Set environment variable 'name' to 'value ...'
 - **setenv <name>**
 - Delete environment variable 'name'
- **saveenv:** save updates to environment variables.
- **bootargs:** pass to the kernel, which are called kernel command lines In Linux Console
- **cat /proc/cmdline:** displays command line
- **cat /sys/devices/virtual/thermal/thermal_zone0/temp:** print temperature to screen (chip should be calibrated)
- **cat /sys/kernel/debug/clk/clk_summary:** print all clks to screen

7. Revision history

Table 16. Revision history

Revision number	Date	Substantive changes
0	09/2016	Initial release
1	07/2017	Updated 800MHz and 900MHz data and related description
2	10/2017	Updated Data in Table 1 - 9

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