Using the CodeTEST Probe with Freescale™ MGT5100 Processors

This document describes the requirements for connecting the CodeTEST Probe to the external bus of the MGT5100 processor.

Purpose

This document supplements the *Setup and Installation Guide for the CodeTEST Probe* which provides generic information on setting up, connecting, and configuring the CodeTEST Probe, and describes CodeTEST address and data port requirements, and bus and timing requirements.

Use the information in this document to make the physical connection between the CodeTEST Probe and the MGT5100 processor and to configure the Probe with the CodeTEST Manager.

Hardware Connections

The CodeTEST Probe supports targets with bus clocks up to 100 MHz with no wait states and 100-133 MHz with one wait state.

The Probe supports 16- and 32-bit port sizes. You will need to identify data and address tag ports to be used for data transfers to the Probe.

Connect CodeTEST Probe to MGT5100 using LocalPlus Bus interface in non-multiplexed bus operating mode

For this connection you can use a dedicated chip select or a non-dedicated chip select. All the chip selects (CS0:5) are available on external pins. See the section “MGT5100 Chip Select Initialization” for information about initializing the chip selects.

The following connections are required:

Probe	Processor	Notes
D15:0	EXT_AD_31:16	Data pins
A15:0	EXT_AD_15:0	Address pins – see note 1 below.
X15:0	NC	
C0	NC	VCC – not necessary.
C1	PCI_CLOCK	CLK
C2	NC	DS
C3	LP_CS_x*	AS
C4	NC	RST2

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Version 4

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Probe	Processor	Notes
C5	NC	RST1
C6	NC	CYC
C7	LP_RW*	WS

Notes:

1. If you are using a non-dedicated chip select, then all address pins should be connected to the Probe as shown in the table above. If you are using a dedicated chip select, only the following pins need to be connected:

   Probe A3:1 <-> Processor EXT_AD_3:1

   See the section “Signal Minimization” in the *Setup and Installation Guide for the CodeTEST Probe* for more information.

2. Remember to connect the CodeTEST pod GND (ground) wires to the target board ground.

Connect CodeTEST Probe to MGT5100 using LocalPlus Bus interface in multiplexed bus operating mode

This connection can be used whether or not there is a chip select dedicated to CodeTEST Probe use. All the chip selects (CS0:5) are available on external pins.

The following connections are required:

Probe	Processor	Notes
A31:0	EXT_AD_31:0	Address/Data pins
X15:0	NC	
C0	NC	VCC – not necessary.
C1	PCI_CLOCK	CLK
C2	LP_CS_x*	DS
C3	LP_ALE*	AS
C4	NC	RST2
C5	NC	RST1
C6	NC	CYC
C7	LP_RW*	WS

Note:

Remember to connect the CodeTEST pod GND (ground) wires to the target board ground.

Connect CodeTEST Probe to MGT5100 using the PCI Interface

The CodeTEST Probe cannot be connected directly to a PCI bus because there are many different bus cycles on the PCI bus.

To connect to a PCI bus, a CodeTEST PCI adapter is required. To connect a CodeTEST PCI adapter, a standard PCI slot, PMC, or CompactPCI connector is required. See the CodeTEST PCI adapter connection documentation and PCI v2.2 specifications for more information.

Probe Configuration

This section identifies the settings you should use in the **Probe Config Utility** in the CodeTEST Manager when you configure the Probe.

Connect CodeTEST Probe to MGT5100 using LocalPlus Bus interface in non-multiplexed bus operating mode

Select the **Universal** Probe type and the following settings:

Field	Setting	Notes
Port Address		Enter address of the control port.
Port Address Mask	0xFFFFFFFF 0xFFFF0000	Dedicated chip select. Non-dedicated chip select.
Extended Bus	0x0	
Extended Bus Mask	0xFFFF	
Bus Type	Non-multiplexed	
Port Size	16 bits	
Reset Configuration	Neither	
Strobe Configuration	1 Strobe	
Address Strobe Polarity	Low	
Write Strobe Polarity	Low	
Bus Arbitration Polarity	Disabled	
Endianess	Big	
Word Swap	No	
Frequency Range		Set according to frequency of clock being monitored.
Phase Shift	0	Adjust as necessary to obtain accurate data.
Invert Clock	No	
Trigger In Edge	Rising	
Router Image		Select appropriate router image.

Connect CodeTEST Probe to MGT5100 using LocalPlus Bus interface in multiplexed bus operating mode

Select the **Universal** Probe type and the following settings:

Field	Setting	Notes
Port Address		Enter address of the control port.
Port Address Mask	0xFFFFFFFF 0xFE000000	Dedicated chip select. Non-dedicated chip select.
Extended Bus	0x0	
Extended Bus Mask	0xFFFF	
Bus Type	Multiplexed	
Port Size	16 bits / 32 bits	Set according to the values of bits 22:23 (DS – Data Size) of the CSx Configuration Register. See the section “MGT5100 Chip Select Initialization” for multiplexed bus mode.
Reset Configuration	Neither	
Strobe Configuration	2 Strobe	
Address Strobe Polarity	Low	
Write Strobe Polarity	Low	
Bus Arbitration Polarity	Disabled	
Endianess	Big	
Word Swap	No	
Frequency Range		Set according to frequency of clock being monitored.
Phase Shift	0	Adjust as necessary to obtain accurate data.
Invert Clock	No	
Trigger In Edge	Rising	
Router Image		Select appropriate router image.

MGT5100 Chip Select Initialization

The chip selects are controlled by the Chip Select Configuration registers, the ADREN (Address Space Enable) register, and the Chip Select Control register.

- The CS Configuration registers are located at address *MBAR+0x0300+offset*, where *offset* = 0x04**x* and *x* is the index of the chip select.
- The ADREN register is located at *MBAR+0x0054*.
- The CS Control register is located at *MBAR+0x0318*.

To initialize the chip select CS*x* for CodeTEST Probe use, the following settings must be made.

- For both multiplexed and non-multiplexed bus modes, the chip select CSx must be enabled:

  - In the ADREN register, the bit corresponding to the chip select CSx must be set (bit 10 for CS5 – bit 15 for CS0, where 0 is the MSB).
  - In the CSx Configuration register (bit 0 is the MSB), bit 19 (CE – Chip Enable) must be set.

- For non-multiplexed bus mode, in the CSx Configuration register:
  - Bit 16 (MX - Multiplexed) must be cleared.
  - Bits 20:21 (AS - Address Size) must be set to 01 (16 bits).
  - Bits 22:23 (DS - Data Size) must be set to 01 (2 bytes).
- For multiplexed bus mode, in the CSx Configuration register:
  - Bit 16 (MX - Multiplexed) must be set.
  - Bits 22:23 (DS - Data Size) must be set to 01 (for 16 bits) or 11 (for 32 bytes).
- For both multiplexed and non-multiplexed bus modes, external transactions must be enabled in the CS Control register; bit 7 (ME – Master Enable) must be set.
- If CS0 is used, bit 6 (BootEna) must be cleared (to disable boot for CS0).
- For both multiplexed and non-multiplexed modes CSx Start and Stop Addresses must be set.

See “3.3.1 Memory Map Registers—MBAR + 0x0000” and “9.4.2 Chip Select/LocalPlus Bus Registers—MBAR + 0x0300” in the *MGT5100 User Manual* for more information on configuring the chip selects.

Limitations

Processors with bus frequencies over 100 MHz must use the Mictor-38 connection method and have at least 2 clock cycles per bus cycle.

The Probe does not support the following memory activities:

- Pipelined accesses: Multiple or overlapping address cycles in relation to the data portion of a bus cycle.
- Burst accesses: The tag ports must be located in a non-burst memory region.
- Misaligned accesses: The tag ports must be on 64-bit aligned memory locations.
- Cache: The tag ports must be located in non-cached or cached write-through memory.
- DRAM: The tag ports cannot be located in DRAM on processors with built-in DRAM controllers.
- 8-bit ports: 8-bit ports are not correctly reconstructed into 32-bit tags.