Using the CodeTEST Probe with Freescale™ MGT5200 Processors

This document describes the requirements for connecting the CodeTEST Probe to the external bus of the MGT5200 processor.

Purpose

This document supplements the *Setup and Installation Guide for the CodeTEST Probe*, which provides generic information on setting up, connecting, and configuring the CodeTEST Probe, and describes CodeTEST address and data port requirements, and bus and timing requirements.

Use the information in this document to make the physical connection between the CodeTEST Probe and MGT5200 processor and to configure the Probe with the CodeTEST Manager.

Hardware Connections

The CodeTEST Probe supports targets with bus clocks up to 100 MHz with no wait states and 100-133 MHz with one wait state.

The Probe supports 16- and 32-bit port sizes. You will need to identify data and address tag ports to be used for data transfers to the Probe.

Connect CodeTEST to MGT5200 using LocalPlus Bus interface in Non-Multiplexed – Legacy bus operating mode

For this connection you can use a dedicated chip select or a non-dedicated chip select. The MGT5200 processor has 8 chip selects, but only CS0:5 are available on external pins. See the section “MGT5200 Chip Select Initialization” for information about initializing the chip select.

The following connections are required:

Probe	Processor	Notes
D15:0	EXT_AD_31:16	Data pins
A15:0	EXT_AD_15:0	Address pins – see note 1 below.
X15:0	NC	
C0	NC	VCC – not necessary.
C1	PCI_CLOCK	CLK
C2	NC	DS
C3	LP_CS_x*	AS
C4:6	NC	RST2

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Version 4

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Probe	Processor	Notes
C5	NC	RST1
C6	NC	CYC
C7	LP_RW*	WS

Notes:

1. If you are using a non-dedicated chip select, then all address pins should be connected to the Probe as shown in the table above. If you are using a dedicated chip select, only the following pins need to be connected:

   Probe A3:1 <-> Processor EXT_AD_3:1

   See the section “Signal Minimization” in the *Setup and Installation Guide for the CodeTEST Probe* for more information.

2. Remember to connect the CodeTEST pod GND (ground) wires to the target board ground.

Connect CodeTEST Probe to MGT5200 using LocalPlus Bus interface in non-multiplexed – MOST/Graphic bus operating mode

For this connection you can use a dedicated chip select or a non-dedicated chip select. The MGT5200 processor has 8 chip selects, but only CS0:5 are available on external pins. For this connection, 24 address bits and 32 data bits can be used. See the section “MGT5100 Chip Select Initialization” for information about initializing the chip select.

Non-Dedicated Chip Select

The following connections are required:

Probe	Processor	Notes
D31:0	EXT_AD_31:0	Data pins
A23	LP_ALE	Address pins ATA and PCI not available in this bus mode.
A22	ATA_ISOLATION	
A21	ATA_INTRQ	
A20	ATA_IOCHRDY	
A19	ATA_IOW	
A18	ATA_IOR	
A17	ATA_DACK	
A16	ATA_DRQ	
A15	PCI_RESET	
A14	PCI_GNT	
A13	PCI_REQ	
A12	PCI_IDSEL	
A11	PCI_PERR	

Probe	Processor	Notes
A10	PCI_SERR	
A9	PCI_FRAME	
A8	PCI_DEVSEL	
A7	PCI_STOP	
A6	PCI_IRDY	
A5	PCI_TRDY	
A4:A1	PCI_CBE_3:0	
A0	PCI_PAR	
X15:0	NC	
C0	NC	VCC – not necessary.
C1	PCI_CLOCK	CLK
C2	NC	DS
C3	LP_CS_x*	AS
C4	NC	RST2
C5	NC	RST1
C6	NC	CYC
C7	LP_RW*	WS

Note:

Remember to connect the CodeTEST pod GND (ground) wires to the target board ground.

Dedicated Chip Select

The following connections are required:

Probe	Processor	Notes
D31:0	EXT_AD_31:0	Data pins
A3:A1	PCI_CBE_2:0	Address pins ATA and PCI not available in this bus mode.
X15:0	NC	
C0	NC	VCC – not necessary.
C1	PCI_CLOCK	CLK
C2	NC	DS
C3	LP_CS_x*	AS
C4	NC	RST2
C5	NC	RST1

Probe	Processor	Notes
C6	NC	CYC
C7	LP_RW*	WS

Note:

Remember to connect the CodeTEST pod GND (ground) wires to the target board ground.

Connect CodeTEST Probe to MGT5200 using LocalPlus Bus interface in non-multiplexed – Large Flash bus operating mode

For this connection you can use a dedicated chip select or a non-dedicated chip select. The MGT5200 processor has 8 chip selects, but only CS0:5 are available as pin-outs. For this connection 26 address bits and 16 data bits can be used. See the section “MGT5200 Chip Select Initialization” for information about initializing the chip select.

Non-Dedicated Chip Select

The following connections are required:

Probe	Processor	Notes
D15:0	EXT_AD_31:16	Data pins
A25	PCI_FRAME	
A24	PCI_DEVSEL	
A23	PCI_STOP	
A22	PCI_IRDY	Address pins
A21	PCI_TRDY	PCI not available in this bus mode.
A20:A17	PCI_CBE_3:0	
A16	PCI_PAR	
A15:0	EXT_AD_15:0	
X15:0	NC	
C0	NC	VCC – not necessary.
C1	PCI_CLOCK	CLK
C2	NC	DS
C3	LP_CS_x*	AS
C4	NC	RST2
C5	NC	RST1
C6	NC	CYC
C7	LP_RW*	WS

Note:

Remember to connect the CodeTEST pod GND (ground) wires to the target board ground.

Dedicated Chip Select

The following connections are required:

Probe	Processor	Notes
D15:0	EXT_AD_31:16	Data pins
A3:1	EXT_AD_3:1	PCI not available in this bus mode.
X15:0	NC	
C0	NC	VCC – not necessary.
C1	PCI_CLOCK	CLK
C2	NC	DS
C3	LP_CS_x*	AS
C4	NC	RST2
C5	NC	RST1
C6	NC	CYC
C7	LP_RW*	WS

Note:

Remember to connect the CodeTEST pod GND (ground) wires to the target board ground.

Connect CodeTEST Probe to MGT5200 using LocalPlus Bus interface in multiplexed bus operating mode

This connection can be used whether or not there is a chip select dedicated to CodeTEST Probe use. The chip selects available on external pins are CS0:5.

The following connections are required:

Probe	Processor	Notes
A31:0	EXT_AD_31:0	Address/Data pins
X15:0	NC	
C0	NC	VCC – not necessary
C1	PCI_CLOCK	CLK
C2	LP_CS_x*	DS
C3	LP_ALE*	AS
C4	NC	RST2
C5	NC	RST1
C6	NC	CYC
C7	LP_RW*	WS

Note:

Remember to connect the CodeTEST pod GND (ground) wires to the target board ground.

Connect CodeTEST to MGT5200 using the PCI Interface

The CodeTEST Probe cannot be connected directly to a PCI bus because there are many different bus cycles on the PCI bus.

To connect to a PCI bus, a CodeTEST PCI adapter is required. To connect a CodeTEST PCI adapter a standard PCI slot, PMC, or CompactPCI connector is required. See the CodeTEST PCI adapter connection documentation and PCI v2.2 specifications for more information.

Probe Configuration

This section identifies the settings you should use in the **Probe Config Utility** in the CodeTEST Manager when you configure the Probe.

Connect CodeTEST Probe to MGT5200 using LocalPlus Bus interface in all non-multiplexed bus operating modes

Select the **Universal** Probe type and the following settings:

Field	Setting	Notes
Port Address		Enter address of the control port.
Port Address Mask		Enter appropriate mask for the connection. See Note 1 below.
Extended Bus	0x0	
Extended Bus Mask	0xFFFF	
Bus Type	Non-multiplexed	
Port Size	16 bits / 32 bits	Select appropriately for target hardware. See Note 2 below.
Reset Configuration	Neither	
Strobe Configuration	1 Strobe	
Address Strobe Polarity	Low	
Write Strobe Polarity	Low	
Bus Arbitration Polarity	Disabled	
Endianess	Big	
Word Swap	No	
Frequency Range		Set according to frequency of clock being monitored.
Phase Shift	0	Adjust as necessary to obtain accurate data.

Invert Clock	No	
Trigger In Edge	Rising	
Router Image		Select appropriate router image.

Notes:

1. The Port Address Mask should be 0xFFFFFFFF if you are using a dedicated chip select. If you are using a non-dedicated chip select, the Port Address Mask should be:
   - 0xFFFF0000 for Legacy Non-Multiplexed bus mode (16 address bits)
   - 0xFF000000 for MOST/Graphic Non-Multiplexed bus mode (24 address bits)
   - 0xFC000000 for Large Flash Non-Multiplexed bus mode (26 address bits)
2. The port size is 32 bits for MOST/Graphic bus mode, 16 bits for Large Flash bus modes. For the Legacy bus modes, the port size can be 16 or 32 bits and must be set according to the values of bits 22:23 (DS – Data Size) of the CSx Configuration Register (see the section “MGT5200 Chip Select Initialization” for non-multiplexed bus mode).

Connect CodeTEST Probe to MGT5200 using LocalPlus Bus interface in multiplexed bus operating mode

Select the **Universal** Probe type and the following settings:

Field	Setting	Notes
Port Address		Enter address of the control port.
Port Address Mask	0xFFF00000	
Extended Bus	0x0	
Extended Bus Mask	0xFFFF	
Bus Type	Multiplexed	
Port Size	16 bits / 32 bits	Select appropriately for target hardware. See Note below.
Reset Configuration	Neither	
Strobe Configuration	2 Strobe	
Address Strobe Polarity	Low	
Write Strobe Polarity	Low	
Bus Arbitration Polarity	Disabled	
Endianess	Big	
Word Swap	No	
Frequency Range		Set according to frequency of clock being monitored.
Phase Shift	0	Adjust as necessary to obtain accurate data.
Invert Clock	No	

Trigger In Edge	Rising	
Router Image		Select appropriate router image.

Note:

The port size can be 16 or 32 bits and must be set according to the values of bits 22:23 (DS – Data Size) of the CSx Configuration register (see the section “MGT5200 Chip Select Initialization” for multiplexed bus mode).

MGT5200 Chip Select Initialization

The chip selects are controlled by the Chip Select Configuration registers, the IPBI Control Register and the Chip Select Control register.

- The CS Configuration registers are located at address *MBAR+0x0300+offset*, where *offset* = 0x04**x* and *x* is the index of the chip select.
- The IPBI Control register is located at *MBAR+0x0054*.
- The CS Control register is located at *MBAR+0x0318*.

For **all bus modes**:

- To initialize chip select CS*x* for the CodeTEST Probe, the following settings must be made:
  - The chip select CSx must be enabled.
  - In the IPB Configuration Register, the bit corresponding to chip select CSx must be set (bit 10 for CS5 – bit 15 for CS0, where 0 is the MSB).
  - In the CSx Configuration Register (bit 0 is the MSB), bit 19 (CE – Chip Enable) must be set.
- External transactions must be enabled:
  - In the CS Control Register, bit 7 (ME – Master Enable) must be set.
- If CS0 is used, bit 6 (BootEna) must be cleared (to disable boot for CS0).
- CSx start and stop addresses must be set (in the registers CSx Start Address and CSx Stop Address).

Below are the settings specific to specific bus modes:

For **Non-Multiplexed Legacy bus mode**, in the CSx Configuration register:

- Bit 16 (MX - Multiplexed) must be cleared.
- Bits 20:21 (AS - Address Size) must be set to 01 (16 bits).
- Bits 22:23 (DS - Data Size) must be set to 01 (2 bytes).

For **Multiplexed bus mode**, in the CSx Configuration register:

- Bit 16 (MX - Multiplexed) must be set.
- Bits 22:23 (DS - Data Size) must be set to 01 (for 16 bits) or 11 (for 32 bytes).

For **Non-Multiplexed MOST/Graphics bus mode**, there is only one configuration (24 bits address, 32 bits data), which is selected by default.

For **Non-Multiplexed Large Flash bus mode**, the only configuration that can be used for the CodeTEST Probe is 26 bits address, 16 bits data.

See sections “3.3.3.2 Boot and Chip Select Addresses” and “9.7.2 Chip Select/LPC Registers—MBAR + 0x0300” of the *MGT5200 User Manual* for more information on configuring the chip select.

Non-Multiplexed Bus Mode Configuration

The Non-Multiplexed bus modes (Legacy, MOST/Graphics, Large Flash) are selectable via the reset configuration word. See the section, “4.6 Reset Configuration” in the *MGT5200 User Manual* for information on how to configure the reset configuration word.

Limitations

Processors with bus frequencies over 100 MHz must use the Mictor-38 connection method and have at least 2 clock cycles per bus cycle.

The Probe does not support the following memory activities:

- Pipelined accesses: Multiple or overlapping address cycles in relation to the data portion of a bus cycle.
- Burst accesses: The tag ports must be located in a non-burst memory region.
- Misaligned accesses: The tag ports must be on 64-bit aligned memory locations.
- Cache: The tag ports must be located in non-cached or cached write-through memory.
- DRAM: The tag ports cannot be located in DRAM on processors with built-in DRAM controllers.
- 8-bit ports: 8-bit ports are not correctly reconstructed into 32-bit tags.