Using the CodeTEST Probe with Freescale™ MSC8101 Processors

This document describes the requirements for connecting the CodeTEST Probe to MSC8101 processors.

Purpose

This document supplements the "*Setup and Installation Guide for the CodeTEST Probe"*, which provides generic information on setting up, connecting, and configuring the CodeTEST Probe, and describes CodeTEST address and data port requirements, and bus and timing requirements.

Use the information in this document to make the physical connection between the CodeTEST Probe and MSC8101 processors and to configure the Probe with the CodeTEST Manager.

Hardware Connections

The CodeTEST Probe supports targets with bus clocks up to 100 MHz with no wait states and 100-133 MHz with one wait state.

The Probe supports 32- and 64-bit port sizes. You will need to identify data and address tag ports to be used for data transfers to the Probe.

MSC8101 processors support 32- and 64-bit port sizes. While the Probe will support a 32-bit port (i.e., tag ports on 32 bit aligned memory locations), it is advisable to always use a 64-bit port (i.e., tag ports on 64-bit aligned memory locations). This way the Probe will naturally support 64-bit ports, and can also support 32-bit ports by locating the ports on 64-bit boundaries.

Connect CodeTEST Probe to MSC8101 running in Single Master Bus mode

Use this connection if the target is set up in single-master bus mode. The chip select used for the Probe must be configured so that it meets the requirements of the Probe AS signal. See "Probe Specifications" in the "*Setup and Installation Guide for the CodeTEST Probe"*.

The following connections are required:

Probe	Processor	Notes
D31:0	D0:31	Note the bit-wise inversion of the bus.
A31:0	A0:31	Note the bit-wise inversion of the bus.
X15:0	NC	
C0	NC	VCC – not necessary.
C1	CLKOUT	CLK
C2	NC	DS

CodeTEST Development Team

Version 3

freescale semiconductor

Probe	Processor	Notes
C3	$\overline{\text{CSx}}$	AS
C4	$\overline{\text{HRESET}}$	RST2
C5	$\overline{\text{SRESET}}$	RST1
C6	NC	CYC
C7	$\overline{\text{BCTL0}}$	WS

Connect CodeTEST Probe to MSC8101 running in Multiple Master Bus mode

Use this connection if the target is set up in multiple-master bus mode. It takes advantage of all the signals available in this bus mode. For information on connecting to the 60x bus, see the application note on connecting the Probe to the 60x bus, the "*MSC8101 Reference Manual*," and "*PowerPC™ Microprocessor Family: The Bus Interface for 32-Bit Microprocessors*."

Probe Configuration

This section identifies the settings you should use in the **Probe Config Utility** in the CodeTEST Manager when you configure the Probe.

Connect CodeTEST Probe to MSC8101 running in Single Master Bus mode

Select the **Universal** Probe type and the following settings:

Field	Setting	Notes
Port Address		Enter address of the Probe tag port.
Port Address Mask	0x0	
Extended Bus	0x0	
Extended Bus Mask	0xFFFF	
Bus Type	Non-multiplexed	
Port Size		Select appropriately for target hardware.
Reset Configuration	Both	
Strobe Configuration	1 Strobe	
Address Strobe Polarity	Low	
Write Strobe Polarity	Disabled	
Bus Arbitration Polarity	Disabled	
Endianess	Big	
Word Swap	No	
Frequency Range		Set according to frequency of target clock.
Phase Shift		Adjust as necessary to obtain accurate data.

Invert Clock	No	
Router Image		Select appropriate routing image.

MSC8101 Chip Select Initialization

The chip select must be associated with a memory bank which is assigned to a GPCM or UPM; a synchronous SDRAM Machine cannot be used for the CodeTEST Probe. The memory bank is configured by a Base Register (BRx), an Options Register (ORx), and other interface-specific registers. For information on how to configure the memory bank, see *"10. Memory Controller*" in the "*MSC8101 Reference Manual"*.

Limitations

Processors with bus frequencies over 100 MHz must use the Mictor-38 connection method and have at least 2 clock cycles per bus cycle.

The Probe does not support the following memory activities:

- Pipelined accesses: Multiple or overlapping address cycles in relation to the data portion of a bus cycle.
- Burst accesses: The tag ports must be located in a non-burst memory region.
- Misaligned accesses: The tag ports must be on 64-bit aligned memory locations.
- Cache: The tag ports must be located in non-cached or cached write-through memory.
- DRAM: The tag ports cannot be located in DRAM on processors with built-in DRAM controllers.
- 8-bit ports: 8-bit ports are not correctly reconstructed into 32-bit tags.