Using the CodeTEST Probe with Freescale™ PPC60x Family Processors

This document describes the requirements for connecting the CodeTEST Probe to the PPC60x family processors

Purpose

This document supplements the *Setup and Installation Guide for the CodeTEST Probe*, which provides generic information on setting up, connecting, and configuring the CodeTEST Probe, and describes CodeTEST address and data port requirements, and bus and timing requirements.

Use the information in this document to make the physical connection between the CodeTEST Probe and PPC603, PPC604, PPC740, PPC750, or PPC8260 processors and to configure the Probe with the CodeTEST Manager. Other PPC60x busses are supported as long as ABB* and DBB* are available for CodeTEST use.

Hardware Connections

The CodeTEST Probe supports targets with bus clocks up to 100 MHz with no wait states and 100-133 MHz with one wait state.

The Probe supports 32- and 64-bit port sizes. PPC processors support port sizes of 32 and 64 bits. While the Probe will support a 32-bit port (tag ports on 32 bit aligned memory locations) it is advisable to always use a 64-bit port (tag ports on 64-bit aligned memory locations). This way, the Probe will naturally support 64-bit ports, and can also support 32-bit ports by locating the ports on 64-bit boundaries.

You will need to identify data and address tag ports to be used for data transfers to the Probe.

The following connections are required:

Probe	Processor	Notes
D31:0	DH0:31	Note the bit-wise inversion of the bus.
A31:0	A0:31	Note the bit-wise inversion of the bus.
X15:6	NC	
X5	AACK*	
X4:3	NC	
X2	TT3	
X1:0	NC	
C0	VCC	VCC – not necessary
C1	SYSCLK	CLK

CodeTEST Development Team

Version 3

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Probe	Processor	Notes
C2	DBB*	DS
C3	ABB*	AS
C4	HRESET*	RST2
C5	SRESET*	RST1
C6	ARTRY*	CYC
C7	TT1	WS

Probe Configuration

This section identifies the settings you should use in the **Probe Config Utility** in the CodeTEST Manager when you configure the Probe.

You can use the PPCxxx or the Universal Probe type and select the following settings. The fields that do not appear for the PPCxxx Probe type are set to the values shown below:

Field	Setting	Notes
Port Address		Enter address of the Probe tag port.
Port Address Mask	0x0	
Extended Bus	0x0	
Extended Bus Mask	0xFFFF	
Bus Type	PPC60x bus	
Port Size		Select appropriately for target hardware.
Reset Configuration	Both	
Strobe Configuration	Both	
Address Strobe Polarity	Low	
Write Strobe Polarity	Low	
Bus Arbitration Polarity	Low	Do not set to Disabled.
Endianess	Big	
Word Swap	No	
Frequency Range		Set according to frequency of target clock.
Phase Shift	-4	Adjust as necessary to obtain accurate data.
Invert Clock	No	
Routing Image		Select appropriate routing image.

Startup Requirements

You must start the system in the following order in order for the CodeTEST Probe to properly collect tags will connecting in 60x mode. This ensures that address and data cycles will be correctly correlated when pipelining is present.

1. Power up the CodeTEST Probe.
2. Connect the CodeTEST Manager to the Probe.
3. Power up the target.

When connecting the Probe to a target that is already running, a hard reset (HRESET asserted) is required after the connection is made and Probe configuration is complete. A hard reset is also required each time the Probe configuration is downloaded to the CodeTEST Probe. This reset is required to synchronize the Probe's internal 60x bus monitoring logic with the processor's bus.

Limitations

60x busses on PPC750Cx and PPC74xx processors are not supported.

Processors with bus frequencies over 100 MHz must use the Mictor-38 connection method and have at least 2 clock cycles per bus cycle.

The Probe does not support the following memory activities:

- Pipelined accesses: Multiple or overlapping address cycles in relation to the data portion of a bus cycle.
- Burst accesses: The tag ports must be located in a non-burst memory region.
- Misaligned accesses: The tag ports must be on 64-bit aligned memory locations.
- Cache: The tag ports must be located in non-cached or cached write-through memory.
- DRAM: The tag ports cannot be located in DRAM on processors with built-in DRAM controllers.
- 8-bit ports: 8-bit ports are not correctly reconstructed into 32-bit tags.