Using the CodeTEST Probe with the Freescale™ Patriot Processor

This document describes the requirements for connecting the CodeTEST Probe to the Patriot processor.

Purpose

This document supplements the *Setup and Installation Guide for the CodeTEST Probe*, which provides generic information on setting up, connecting, and configuring the CodeTEST Probe, and describes CodeTEST address and data port requirements, and bus and timing requirements.

Use the information in this document to make the physical connection between the CodeTEST Probe and the Patriot processor and to configure the Probe with the CodeTEST Manager.

Hardware Connections

The CodeTEST Probe supports targets with 100 MHz bus clocks with no wait states and 100-133 MHz clocks with one wait state.

The Probe supports a 16-bit port size when connected to the Patriot processor. You will need to identify data and address tag ports to be used for data transfers to the Probe.

EBx* used as CodeTEST Address Strobe

This method of connecting the CodeTEST Probe to the external memory interface of the Patriot processor uses one of the enable byte signals as the AS to the Probe. The enable byte signal used as the strobe must be configured to act as a write strobe (EBM=1).

To further qualify the bus cycles, the chip selects should be connected to the Probe extended bus.

Probe	Processor	Notes
D31:16	NC	
D15:0	DATA15:0	
A31:24	ADDR31:24	Not available externally.
A23:0	A23:0	
X15:6	NC	
X5	CS5	
X4:0	CS4:0*	
C0	VCC or NC	VCC – not required

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C1	BCLK_OUT	CLK
C2	NC	DS
C3	EBx*	AS
C4	RESET_OUT*	RST2
C5	NC	RST1
C6	NC	CYC
C7	NC	WS

Probe Configuration

This section identifies the settings you should use in the **Probe Config Utility** in the CodeTEST Manager when you configure the Probe.

Use the Universal Probe type and select the following settings:

Field	Setting	Notes
Port Address		Enter address of the Probe tag port.
Port Address Mask	0xFF000000	
Extended Bus	0x0020	
Extended Bus Mask	0xFFFF	See Note below.
Bus Type	Non-multiplexed	
Port Size	16 bit	
Reset Configuration		Set according to available resets.
Strobe Configuration	1 Strobe	
Address Strobe Polarity	Low	
Write Strobe Polarity	Disabled	
Bus Arbitration Polarity	Disabled	
Endianess	Big	
Word Swap	No	
Frequency Range		Set according to frequency of clock being monitored.
Phase Shift		Adjust as necessary to obtain accurate data.
Invert Clock	No	
Router Image		Select appropriate routing image.

Note: The extended bus mask must be set to allow qualification of the cycle with the appropriate chip select. For example, if the Probe ports reside in a region of memory controlled

by chip select ‘0’ (CS0*), then the mask must be set to 0xFFFE; if the ports reside in a region of memory controlled by chip select ‘1’ (CS1*), then the mask must be set to 0xFFFD; if the ports reside in a region of memory controlled by chip select ‘2’ (CS2*), then the mask must be set to 0xFFFB, and so on.

Limitations

Processors with bus frequencies over 100 MHz must use the Mictor-38 connection method and have at least 2 clock cycles per bus cycle.

The Probe does not support the following memory activities:

- Pipelined accesses: Multiple or overlapping address cycles in relation to the data portion of a bus cycle.
- Burst accesses: The tag ports must be located in a non-burst memory region.
- Misaligned accesses: The tag ports must be on 64-bit aligned memory locations.
- Cache: The tag ports must be located in non-cached or cached write-through memory.
- DRAM: The tag ports cannot be located in DRAM on processors with built-in DRAM controllers.
- 8-bit ports: 8-bit ports are not correctly reconstructed into 32-bit tags.