CodeTEST Probe Interface Guide

This document describes the interface requirements for the CodeTEST Probe. It contains the following sections:

Overview

CodeTEST Tools monitor code performance, code coverage, memory usage, and trace code execution on an embedded target. In order to do this, the CodeTEST Instrumenter inserts tags (typically assignment statements) into C and C++ source code. When tags are reached during code execution, they are written out on a bus that is monitored by the CodeTEST Probe.

Target Interface

The CodeTEST Probe is a synchronous, 64 bit (128 bit if using 64-bit ports), write-only memory device that expects the instrumentation in the target code to be the only thing that accesses its location in the target memory space. The Probe is designed to monitor the target bus – not necessarily the target processor itself. The Probe can be connected to a processor, processor support chip, RAM or ROM memory bank, backplane, I/O port, or any non-cached bus that is physically accessible.

Many high-speed processors require support chips to convert the processor bus to the actual system bus. These chips may step down the bus speed, reorganize signals, and generate the appropriate signals to access physical memory.

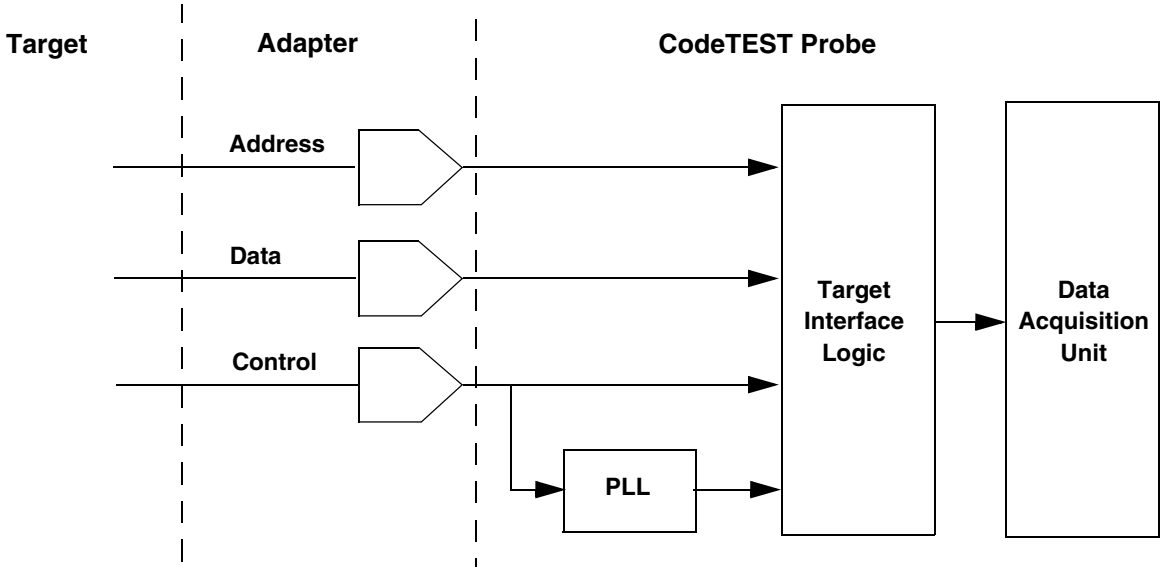
Systems in which a logic analyzer is used to monitor bus activity typically have the appropriate signals readily available for the Probe to monitor bus cycles. For most processors, logic analyzer preprocessors are available for breaking out the signals for easier access to the processor pins. These preprocessors often provide the ideal solution for connecting the Probe to a target.

Block diagram

A target adapter provides the connection between the CodeTEST Probe and the target system. The Probe uses a phase lock loop (PLL) to adjust the timing relationship between the signals and the clock. The data acquisition unit is responsible for filtering instrumentation tags collected from the target bus and passing the data to the data processor.

Revised October 2005

Figure 1.1 Target interface



Special Features

The Probe has a number of special features that provide the flexibility necessary to handle the ever-increasing variations in processor bus cycles. It is no longer as simple as grabbing the address when the address strobe asserts and data when the data strobe asserts. Most buses are quite generic in the way they do accesses, but there are some that do non-standard operations that the Probe needs to know about.

The following features give the Probe great flexibility and should cover most standard bus cycles:

- Target clock control
- 64-bit port support
- Word swapping
- Internal DS (data strobe)
- Single strobe mode
- Multiplexed bus
- Large/small address buses
- Router image

All of the special features are controlled by the CodeTEST Manager Probe Configuration Utility.

Physical Connection

There are several target adapters available for the CodeTEST Probe. Each provides two functions:

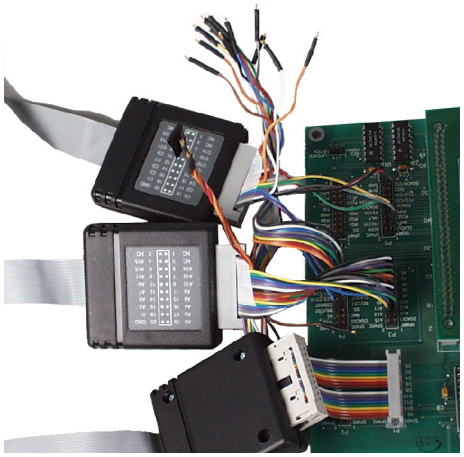
- Connection to the target system.
- Signal buffering. The buffers are located as close to the target as possible to minimize loading of the target by the CodeTEST Probe.

CodeTEST 16-Channel Pod Adapter

The 16-channel pods interface with 2x10 0.1” header logic analyzer connector, and are supplied with extension cables and flying leads. The flying leads allow you to connect to 0.05” posts. The flying leads provide signal routing, if necessary.

This adapter lets you easily connect the Probe to logic analyzer connectors that may be on the your target or to breakout adapters that are available from a number of sources.

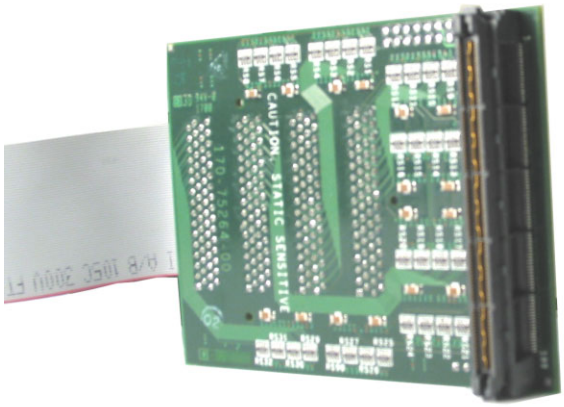
Figure 1.2 16-channel Pod Adapter



CodeTEST Mictor-190 Adapter

This adapter connects a CodeTEST Probe to a Mictor-190 connector with a Freescale 60x bus pinout. The signals cannot be routed.

Figure 1.3 Mictor-190 Adapter

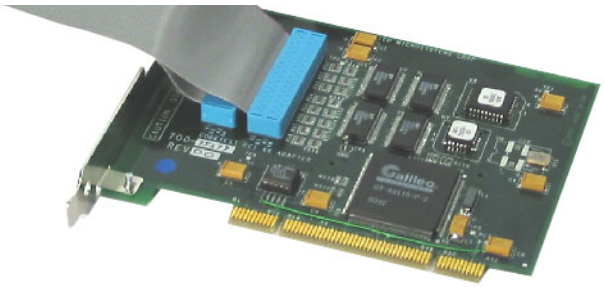


CodeTEST PCI Bus Adapter

These adapters connect a CodeTEST Probe to one of the following PCI configurations:

- Standard PCI slot
- PMC (PCI Mezzanine card)
- Stackable PMC
- cPCI (Compact PCI)

Figure 1.4 PCI Bus Adapter

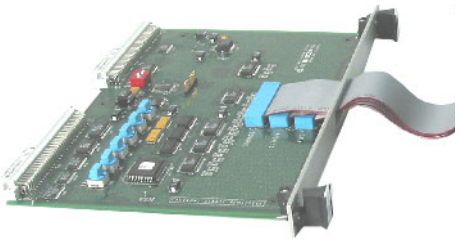


CodeTEST VME Bus Adapter

This adapter connects a CodeTEST Probe to a VME bus. The VME Adapter provides:

- A single slot 6U, 160mm form factor.
- VMEbus slave support for D32 and D16 data transfers using A16, A24, and A32 addressing modes.
- The ability to shadow an existing VME card.

Figure 1.5 VME Bus Adapter



Dedicated Processor Adapter

These adapters connect a CodeTEST Probe to one of several processor sockets. Adapters are available for the following processors:

- PPC 860
- PPC 750

Figure 1.6 Dedicated Processor Adapter

CodeTEST Mictor-38 Adapter

This adapter connects a CodeTEST Probe to Mictor-38 connectors on your target. The adapter includes four cables with Mictor-38 connectors. These cables provide connection to control, address, and data signals.

The four cables do not have permanent designated pin assignments. Instead, the pin assignments are set in a router image that you load into the Probe flash memory.

Before using a Mictor-38 Adapter, you'll need to consult with your Sales Representative to provide requirements for a router image to Support. The Sales Representative will work with Support Engineers to obtain a custom router image for your system.

Figure 1.7 Mictor-38 Adapter

CodeTEST Interface Port

The CodeTEST Interface Port allows a minimized connection to be achieved with a single target Mictor-38 connector. You can either conform to the specified pin-out, or design your own and use a custom router image. For more information, see the *CodeTEST Interface Port Design Guide*.

Signal Descriptions

The Probe has three distinct signal groups: address, control, and data. Each group serves a specific purpose in capturing the correct information from the target system.

Address

The Address signal group contains the A31:0 (address) and X15:0 (extended) buses. These buses are used to determine if the memory location where the tag control and data ports are located has been accessed.

The decoding of these buses is identical. The extended bus can be used for other signals needed to track bus accesses (chip select, function codes, etc.). Both buses can be configured to monitor or ignore any of their signals with the Probe Configuration Utility's mask fields.

The only requirement for these buses is that A1 and A2 be connected (A3 if using 64-bit ports). A2 (or A3) identifies which of the two ports is being accessed. A1 distinguishes which half of the 32-bit tag is currently on the bus when using a 16-bit port. This information can help in minimizing the number of signals necessary.

If using a multiplexed bus structure, connect the target's address/data bus to A31:0, where A0 is the least significant address signal.

Data

The Probe has a dedicated 32-bit data bus. This is verified using the address, extended, and control signal groups and latched according to its port size definition. Systems using 16-bit ports require only the lower bits (D15:0). For 64-bit ports, the 32-bit data bus is connected to the lower half of the target's bus.

NOTE In a multiplexed environment, the target's address/data bus should be connected to A31:0 instead of the dedicated data bus.

Control

The Control signals (C7:C0) are used to validate the address, extended, and data buses, as well as to identify the state of the target system. The signal connections described in this section are generic signals that are typically found on many bus interfaces.

Table 1.1 describes the signals used for decoding most other bus types. Currently the signals are tied to specific signal lines in the control pod. The "signal names" are used in a generic sense – different processors might use different names for similar functions. For example, Address Strobe (AS) might also be called Transfer Start (TS), Address Latch Enable (ALE), Chip Select (CS), etc.

Table 1.1 Signals Used to Decode Bus Interfaces

Pod Signal	CodeTEST Signal Name	Description
C1	CLK (Clock)	The CodeTEST Probe uses the target's synchronous bus clock to monitor the target bus. This clock must be free running at all times to keep data moving through the Probe's internal data pipeline. All signals, address, data, control, and extended bus are continuously sampled by this clock.
C2	DS (Data Strobe)	The data strobe is used to validate the data bus and indicate when the bus cycle has completed. This signal must be asserted when valid data is on the data bus, and it must de-assert after each bus transaction. The Probe waits for the state-change (from asserted to de-asserted) of this signal before passing the tag data to the rest of the Probe. The data is latched on the last rising edge of the clock before the de-assertion of the data strobe. This means the strobe can be asserted before data is valid, but must be de-asserted before the data bus changes state. NOTE: This signal is active *low* asserted. When using single strobe mode, the Probe uses the address strobe to validate data, and the polarity is user selectable.
C3	AS (Address Strobe)	The address strobe is used to validate the address and extended buses, CYC, and WR signals. This signal can only be asserted when valid address information is on the address and extended buses. In single strobe mode, this signal acts as the address and data strobe and must also meet the requirements for DS. NOTE: The polarity of this signal is defined in the Probe Configuration Utility.
C4 C5	RS2* (Reset 2) RS1* (Reset 1)	Target reset signals. These lines are normally connected to the target's RESET signals, and are used to indicate to the Probe's data processing software that the target has gone through a major change in program execution. Both lines are treated the same, and neither has priority over the other. Both resets are active low.
C6	CYC (Cycle Ownership)	When asserted, the cycle ownership signal indicates that the current bus cycle is being run by the target software. It is used as a bus arbitration signal. NOTE: The polarity of this signal is defined in the Probe Configuration Utility. If this signal is not connected, it must be disabled in the Probe Configuration Utility.
C7	WR (Write Strobe)	Target write strobe. This signal is used to identify if the current bus cycle is a write access. NOTE: The polarity of this signal is defined in the Probe Configuration Utility. If this signal is not connected it must be disabled in the Probe Configuration Utility.
C0	PWR	(Optional) Target VCC. This signal is used to detect if the target has been deactivated. It is NOT used to power the Probe. The Probe supports both 5 and 3.3 volt systems. When using the Mictor-38 Adapter, 2.5 volt systems are also supported.

Signal Minimization

In total, up to 88 signals are used by the Probe. There are ways to minimize what needs to be connected by making some assumptions about the target system and possibly making some changes to the target:

- Assuming that no other bus master will be accessing the tag ports and that the system will never perform a read from that region, disable the CYC and WR signals using the Probe Configuration Utility.
- If the target is not going to be power-cycled or reset while running the tool, the $\overline{\text{RST1}}$ and $\overline{\text{RST2}}$ signals can be left disconnected.
- The Probe needs to monitor only the address lines that are required to decode the entire memory space that the target will use. All unnecessary lines can be disconnected and ignored in the Probe Configuration Utility. If the target can be modified to assert a signal (i.e., chip select) only when accessing the tag ports, then the entire address bus can be left disconnected, with the exception of A3 for 64-bit ports, A2 for 32 bit ports, and A2 and A1 for 16-bit ports.)

- If the target can use a 16-bit port, only the lower 16-bits of the data bus are necessary to connect to the target. In a multiplexed situation, no data bits are required.
- PWR never needs to be connected.

Interface Port

To minimize the number of target hardware connectors required, the CodeTEST Interface Port allows a minimized connection to be achieved with a single target Mictor-38 connector. For more information, see the *CodeTEST Interface Port Design Guide*.

Bus Interface

The CodeTEST Probe supports five basic bus cycles and the PPC603 bus. The timing diagrams for the basic bus cycles are shown below.

In each of the timing diagrams, data is latched into the Probe on the rising clock edge (user-configurable). The Address Strobe (AS) is shown as an active low signal, and the Write Strobe (WS) and the Bus Arbitration (CYC) signals are shown as active high signals. The WS and CYC signals must be valid whenever AS is valid.

The Probe requires an access time of 10 nS. Systems running up to 100 MHz require a 1 clock cycle bus cycle. Systems running over 100 MHz will need to add a wait state to ensure correct operation of Probe. The timing diagrams are all shown without wait states.

Figure 1.8 Non-Multiplexed 2-Strobe Bus Cycle

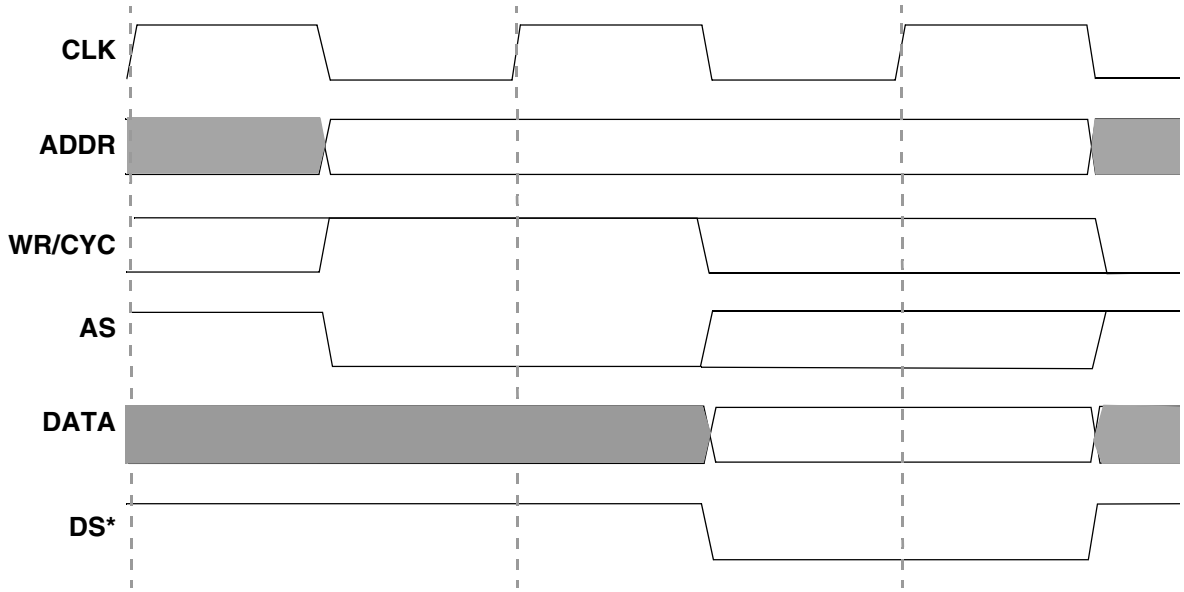
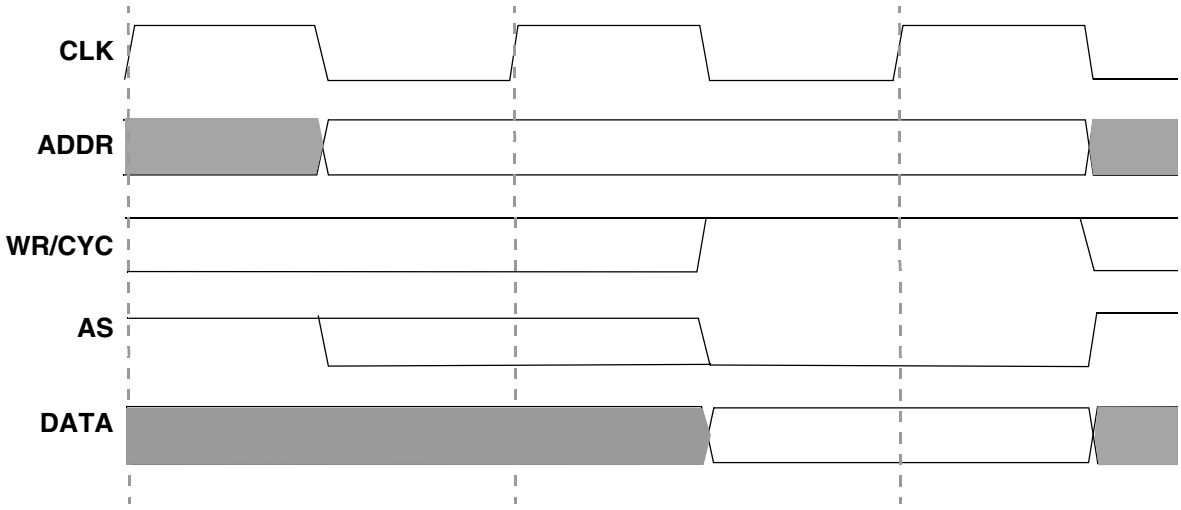
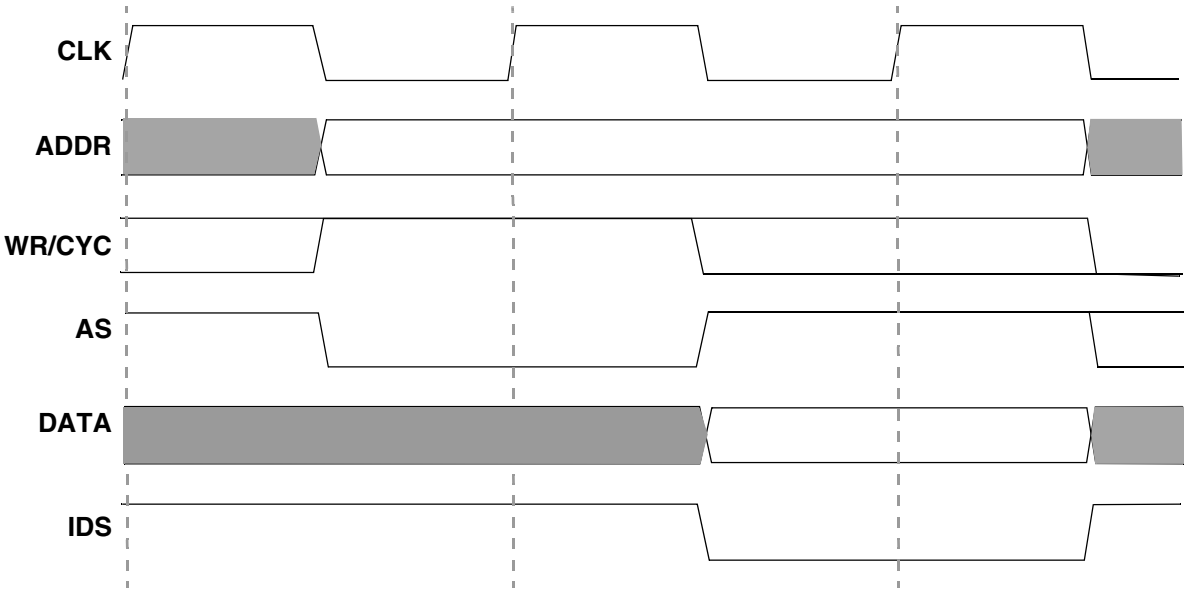


Figure 1.9 Non-Multiplexed 1-Strobe Bus Cycle



The AS may be asserted before the data is valid. The data on the bus during the last rising edge of the clock before AS is de-asserted is used as the tag.

Figure 1.10 Non-Multiplexed Internal Data Strobe Bus Cycle



The internal data strobe (IDS) is generated by the target interface logic and is used only by the Probe. The IDS is a single clock cycle in length and is asserted when AS is de-asserted.

Figure 1.11 Multiplexed 2-Strobe Bus Cycle

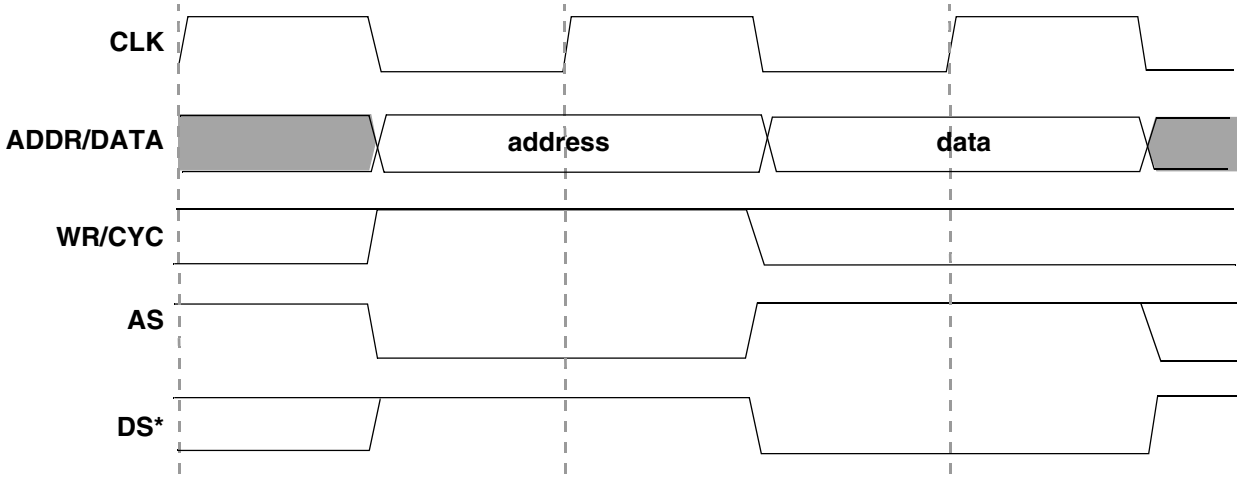
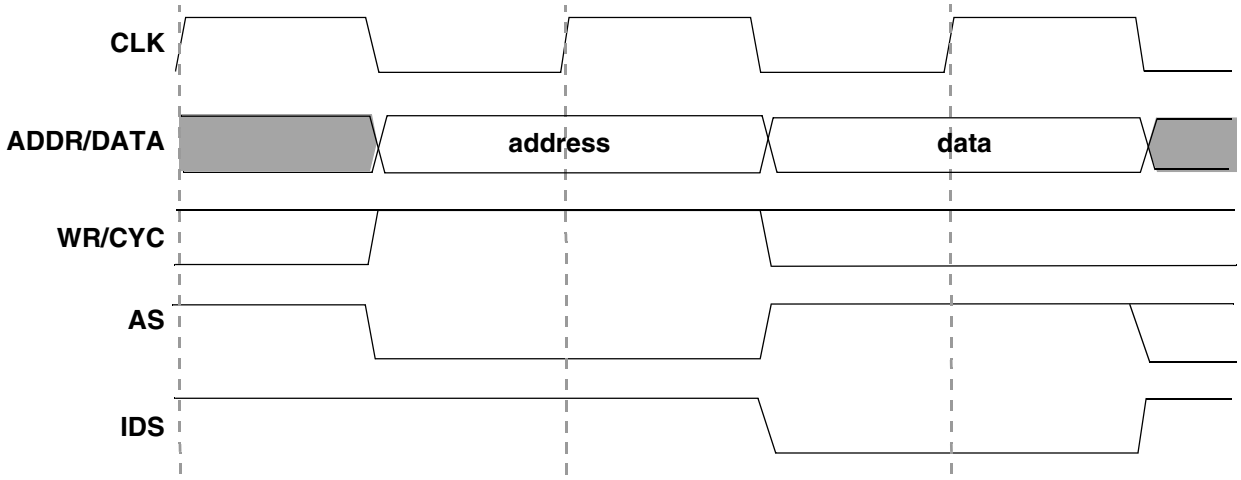


Figure 1.12 Multiplexed Internal Strobe Bus Cycle



PPC 603 bus cycles

In addition to the above bus cycles, the Probe is capable of supporting the PPC603 bus cycle. This bus cycle allows the Probe to support the PPC603, PPC604, PPC740, PPC750, and the 603 bus on the MPC8260. For information on using the Probe with these processors see the PPC60x bus application note.

R30xx bus cycles

This is a special feature to support R3000 bus cycles. Address bits A3:0 are not driven on the Address/Data bus. Instead they are driven on dedicated address pins Addr(3:0). Connect Addr(3:0) to X3:0 on the Probe.

Timing and Loading Specifications

Figure 1.13 System Timing Requirements

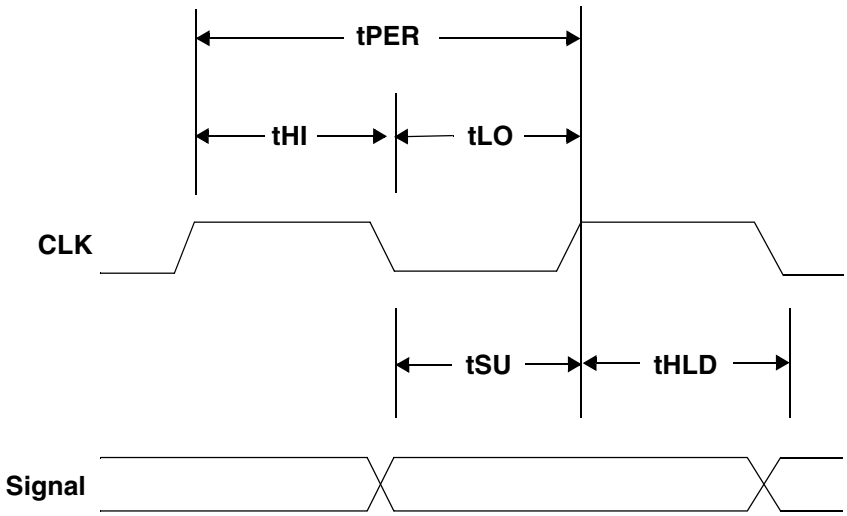
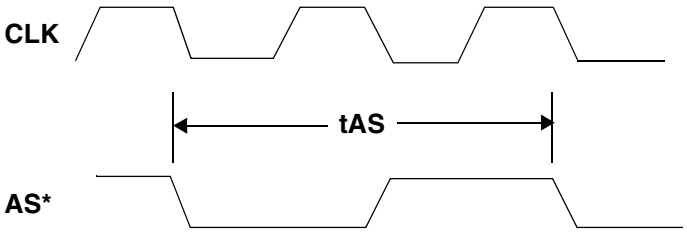


Figure 1.14 Address Strobe Timing Requirements



The following timing and loading specifications apply to all the bus types shown in "Bus Interface" on page 7

Table 1.2 Timing and Loading Specifications

Parameter	Description	Adapter Voltage[2]	Min	Typ	Max	Note
tPER	Period of clock cycle	all	7.5 ns		41.67 ns	1
tHI	Time clock is high	all	3 ns			1
tLO	Time clock is low	all	3 ns			1
tSU	Setup time	all	2 ns			
tHLD	Hold time	all	1 ns			
tAS	Time between assertions	all	20 ns			
V_{IH}	Input high voltage	5 V/3.3 V	2 V		5.25 V	
		2.5 V	1.7 V		5.25 V	2
V_{IL}	Input low voltage	5 V/3.3 V	-0.3 V		0.8 V	
		2.5 V	-0.3 V		0.7 V	2

Table 1.2 Timing and Loading Specifications

Parameter	Description	Adapter Voltage[2]	Min	Typ	Max	Note
I_{IH}	Input current high	all			1 µA	
I_{IL}	Input current low	all			1 µA	
C_{IN}	Input capacitance	all		3.5 pF	6 pF	
Notes: 1. Applies only when using frequency range settings other than 1-25 MHz. 2. Only the Mictor-38 Adapter can be set to 2.5V.						

Configuration

You will need to specify your target configuration in the CodeTEST Manager Probe Configuration Utility. The following features are supported or required.

Bus Cycle

Two fields determine bus cycle configuration in the Probe Configuration Utility. The table below shows the required settings:

Bus Cycle	Bus Type	Strobe Configuration
Non-multiplexed 2 strobe	Non-multiplexed	2 strobe
Non-multiplexed 1 strobe	Non-multiplexed or Interface Port	1 strobe
Non-multiplexed internal data strobe	Non-multiplexed	1 strobe + internal data strobe
Multiplexed 2 strobe	Multiplexed	2 strobe
Multiplexed internal data strobe	Multiplexed or R30xx bus	1 strobe + internal data strobe
PPC603 bus	PPC6XX	N/A

Port Size

CodeTEST Probes support 16, 32, and 64 bit port sizes. Port size refers to the size of the *memory region* where the tag ports are located, not the size of the data bus. The port size options in the CodeTEST Probe Utility are 16+6, 16, 32, and 64.

The port size used depends on the target hardware:

- (versions higher than 4.0.1) 16+6-bit ports are a special case, intended and required for target hardware with a 16-bit processor core and a 16-bit data bus. Compressed 16-bit instrumentation must be used for such systems. A tag write is accomplished through a 16-bit write from the processor. Multiple tag ports are used due to the compression decoding requirements, and cause the Probe to consume 128 bytes of contiguous memory space, beginning at 0x*XXXXXX*00.
- 16-bit ports are intended for target hardware with a 32-bit processor core, where the Probe is connected to a 16-bit data bus. A tag write is accomplished through a 32-bit write from the processor. On a 16-bit bus, this will appear as two 16-bit write cycles. The second write will be located 2 bytes later, thus completing the 32-bit write.
- 32-bit ports are intended for target hardware with a 32-bit data bus. A tag write is accomplished through a 32-bit write from the processor. This will appear on the bus as a 32-bit write.

- 64-bit ports are intended for target hardware with a 32- or 64-bit data bus. In this case, the actual tag must be written to the lower 32 bits of the 64-bit port. The upper 32 bits are ignored by the Probe.

Endianness

By default, the Probe expects data to be in big endian format. This can be changed by setting Endianness to Little in the Probe Configuration Utility.

Endianness refers to the byte (1 byte = 8-bits) ordering relative to the address of a multi-byte word. Big-endian targets store the most significant byte of a word aligned to the lowest address. Little-endian targets store the most-significant byte aligned to the highest address.

The figures below illustrate the difference between big-endian formatting and little- endian formatting. In the figures, A is the least significant byte and H is the most-significant byte.

Table 1.3 8-Byte Word in Big-Endian Format

Data Bit	7 0	15 8	23 16	31 24	39 32	47 40	55 48	63 56
	A	B	C	D	E	F	G	H
Byte Address [2:0]	111	110	101	100	011	010	001	000

Table 1.4 8-Byte Word in Little-Endian Format

Data Bit	63 56	55 48	47 40	39 32	31 24	23 16	15 8	7 0
	H	G	F	E	D	C	B	A
Byte Address [2:0]	111	110	101	100	011	010	001	000

As you can see, it is possible to achieve big-endian style data from little- endian style data by swapping the bytes relative to the address. This is what the Endianness feature accomplishes.

Word-swap

Word-swap is intended only for 16-bit port size. Word-swap is similar to the Endianness feature except it reorders the tag on a word (16-bit) basis.

Target Clock Control

The Probe uses a phase lock loop (PLL) circuit to control the timing relationship between the clock and the rest of the signals it monitors. This allows you to change the setup time on the system to ensure that CodeTEST Probe timing requirements are met. It also allows you to select which clock edge to sample target signals on. The PLL does not affect the clock on the target.

The PLL supports frequency ranges of 24-50 MHz, 48-10 0 MHz, and 96-133 MHz. For operation at low frequencies the 1-25 MHz frequency range is provided. This bypasses the PLL and as a result the clock inversion and phase shift features discussed below are not available.

You can configure the system to sample data on either the rising edge or the falling edge of the target's clock. Setting the invert clock option to 'yes' results in Probe sampling on the falling edge of the target's clock. Likewise setting the invert clock option to 'no' results in Probe sampling on the rising edge.

The PLL also includes a delay line, which allows the Probe to change the timing relationship between the clock and the other signals being monitored. Increasing the phase shift will increase tSU while at the same time reducing tHLD. The clock can be shifted by up to 6 time units in either direction, or it can be inverted and shifted 6 time units in either direction, in increments of 2 time units.

To calculate the actual time shift in the target clock signal, based on the frequency range selected, see the table below, where:

`t` is the time in nanoseconds
`Fnom` is the frequency in MHz of the target's bus clock

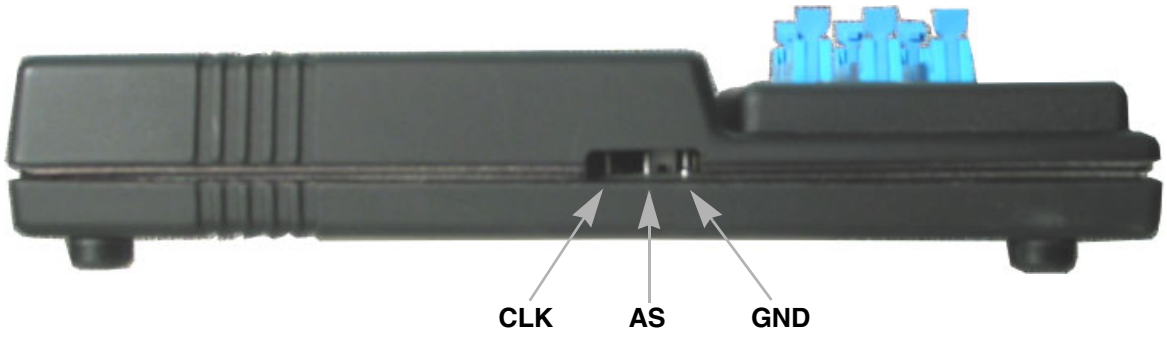
Frequency Range	Time Shift
24–50 MHz	`t = 1000/(32*Fnom)`
48–100 MHz	`t = 1000/(16*Fnom)`
96–133 MHz	`t = 1000/(8*Fnom)`

Adjusting the clock using an oscilloscope

Correct adjustment of the PLL is essential for the operation of the CodeTEST Probe. This may be necessary due to a noisy or overloaded clock signal, or a high-speed application where timing is critical. Using an oscilloscope with a bandwidth of at least five times the bus clock frequency is essential.

Connect the scope to the CLK and AS test points on the Probe, trigger the scope on the AS signal, and view the timing between the rising edge of the clock and the assertion/de-assertion of the strobe. The timing should meet the appropriate setup and hold times as specified in Table 1.2, and shown in Figure 1.13 and Figure 1.14.

Figure 1.15 Test Points



NOTE The CLK test point is taken from a point beyond the output of the PLL. All flip-flops in the target interface logic use the rising edge to latch data.

Limitations

The Probe tag ports cannot support:

- Address pipelines (except for supported PPC603 buses)
- Misaligned accesses
- Cache accesses
- DRAM controllers
- 8-bit port sizes
- Asynchronous probing
- Burst cycles

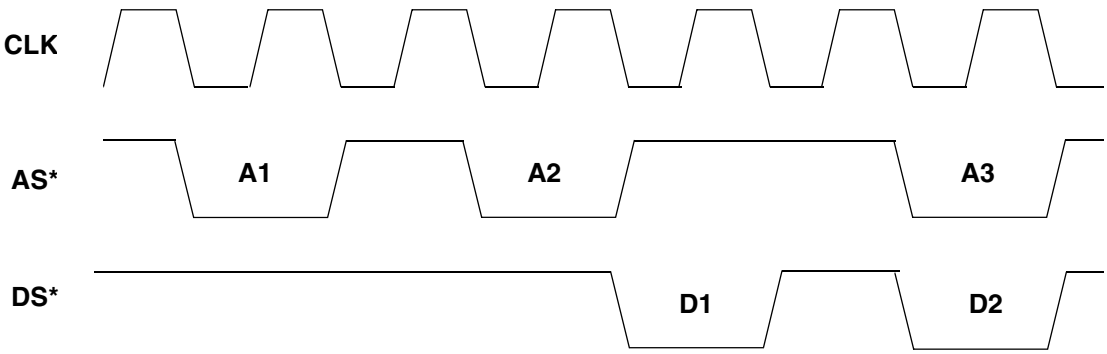
Address Pipelines

An address pipeline refers to a processor’s ability to have multiple or overlapping address cycles in relation to the data being placed on the bus. This feature prevents the Probe from being able to track which piece of data goes with which address, thereby causing data acquisition errors.

Address pipelining support for most PPC60x bus implementations is built into CodeTEST.

The timing diagram in Figure 1.16 shows an example of an address pipeline situation using the address and data strobes to indicate valid cycle activity.

Figure 1.16 Address Pipelining Example



A1 is the first address placed on the bus, A2 is the second, and A3 the third. D1 is the data that corresponds to the address A1 and D2 goes with A2. It can be seen that without specific decoding circuitry, the probe should assume that data D1 goes with address A2. The Probe will also assume that data D2 goes with address A3.

In both cases the Probe will inaccurately capture data. If A2 is a valid tag access, the Probe will capture D1 instead of D2 as the actual tag value.

Misaligned accesses

The tag ports as defined in the instrumentation process must be located on 32-bit boundaries when using 32-bit or smaller port sizes. If using a 64-bit port, they must be located on a 64-bit boundary.

Cache

The tag ports as defined in the instrumentation process must be located in non-cached or write-though cached memory. If the tags are not written to the external bus, the Probe will not see the tag.

DRAM Controllers

The Probe cannot decode access to DRAM memory. DRAM memory uses a multiple address cycle depending on the row and column address used to access a memory location. If the tag ports are located in a non-DRAM area, and the target has a DRAM controller, the Probe will work correctly. If there is an external DRAM controller taking standard bus cycles from the probed device to convert them to DRAM cycles, the Probe will also work correctly. There is a difficulty only when the tag ports are located in a DRAM memory space when the probed device controls the memory access directly.

8-bit Port Sizes

8-bit ports are not correctly reconstructed into 32-bit tags. Some applications where dynamic bus sizing is used may be supported. To do this, the appropriate signals to distinguish between the first, larger access and the following byte access must be connected to the probe via the extended bus. These signals could be SIZE bits, BYTE ENABLEs, or port control bits.

Asynchronous Probing

A clock that is synchronous with the target's bus interface is required to correctly sample the data from the target's bus.

Burst Cycles

The Probe does not fully decode burst cycles. For 32-bit accesses, bursting is generally not a problem due to the way tags are written. Some 32-bit processors with 16-bit data buses will burst the two halves of the tag, resulting in the Probe not being able to collect tags correctly.